**Freescale Semiconductor**
**Technical Data**

Document Number: MPC8572EEC
Rev. 6, 06/2014

# MPC8572E PowerQUICC III Integrated Processor Hardware Specifications

## 1 Overview

This section provides a high-level overview of the features of the MPC8572E processor. Figure 1 shows the major functional units within the MPC8572E.

### 1.1 Key Features

The following list provides an overview of the MPC8572E feature set:

- Two high-performance, 32-bit, Book E-enhanced cores that implement the Power Architecture® technology:
  - Each core is identical to the core within the MPC8572E processor.
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
  - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both

Contents

1. Overview . . . . . 1
2. Electrical Characteristics . . . . . 10
3. Power Characteristics . . . . . 15
4. Input Clocks . . . . . 16
5. RESET Initialization . . . . . 18
6. DDR2 and DDR3 SDRAM Controller . . . . . 19
7. DUART . . . . . 27
8. Ethernet: Enhanced Three-Speed Ethernet (eTSEC) 28
9. Ethernet Management Interface Electrical Characteristics . . . . . 50
10. Local Bus Controller (eLBC) . . . . . 53
11. Programmable Interrupt Controller . . . . . 65
12. JTAG . . . . . 65
13. $I^2C$ . . . . . 67
14. GPIO . . . . . 69
15. High-Speed Serial Interfaces (HSSI) . . . . . 71
16. PCI Express . . . . . 81
17. Serial RapidIO . . . . . 89
18. Package Description . . . . . 99
19. Clocking . . . . . 117
20. Thermal . . . . . 121
21. System Design Information . . . . . 123
22. Ordering Information . . . . . 134
23. Document Revision History . . . . . 136

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the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

— Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.

— Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.

— 36-bit real addressing

— Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.

— Enhanced hardware and software debug support

— Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
  — Shared by both cores.
  — Flexible configuration and individually configurable per core.
  — Full ECC support on 64-bit boundary in both cache and SRAM modes
  — Cache mode supports instruction caching, data caching, or both.
  — External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    – 1, 2, or 4 ways can be configured for stashing only.
  — Eight-way set-associative cache organization (32-byte cache lines)
  — Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  — Global locking and Flash clearing done through writes to L2 configuration registers
  — Instruction and data locks can be Flash cleared separately.
  — Per-way allocation of cache region to a given processor.
  — SRAM features include the following:
    – 1, 2, 4, or 8 ways can be configured as SRAM.
    – I/O devices access SRAM regions by marking transactions as snoopable (global).
    – Regions can reside at any aligned location in the memory map.
    – Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
  — Twelve local access windows define mapping within local 36-bit address space.
  — Inbound and outbound ATMUs map to larger external address spaces.
    – Three inbound windows plus a configuration window on PCI Express

  - Four inbound windows plus a default window on Serial RapidIO®
  - Four outbound windows plus default translation for PCI Express
  - Eight outbound windows plus default translation for Serial RapidIO with segmentation and sub-segmentation support
- Two 64-bit DDR2/DDR3 memory controllers
  - Programmable timing supporting DDR2 and DDR3 SDRAM
  - 64-bit data interface per controller
  - Four banks of memory supported, each up to 4 Gbytes, for a maximum of 16 Gbytes per controller
  - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
  - Full ECC support
  - Page mode support
    - Up to 32 simultaneous open pages for DDR2 or DDR3
  - Contiguous or discontiguous memory mapping
  - Cache line, page, bank, and super-bank interleaving between memory controllers
  - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
  - Sleep mode support for self-refresh SDRAM
  - On-die termination support when using DDR2 or DDR3
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access through JTAG port
  - 1.8-V SSTL_1.8 compatible I/O
  - Support 1.5-V operation for DDR3. The detail is TBD pending on official release of appropriate industry specifications.
  - Support for battery-backed main memory
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts per processor with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters per processor that can generate interrupts
  - Supports a variety of other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing.

  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
  - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, SSL/TLS, SRTP, 802.16e, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units through an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 4096 bits
    - Elliptic curve cryptography with $F_2m$ and F(p) modes and programmable field size up to 1023 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB, CBC and OFB-64 modes for both DES and 3DES
  - AESU—Advanced Encryption Standard unit
    - Implements the Rijndael symmetric key cipher
    - ECB, CBC, CTR, CCM, GCM, CMAC, OFB-128, CFB-128, and LRW modes
    - 128-, 192-, and 256-bit key lengths
  - AFEU—ARC four execution unit
    - Implements a stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - MDEU—message digest execution unit
    - SHA-1 with 160-bit message digest
    - SHA-2 (SHA-256, SHA-384, SHA-512)
    - MD5 with 128-bit message digest
    - HMAC with all algorithms
  - KEU—Kasumi execution unit
    - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
    - Also supports A5/3 and GEA-3 algorithms
  - RNG—random number generator
  - XOR engine for parity checking in RAID storage applications
  - CRC execution unit
    - CRC-32 and CRC-32C
- Pattern Matching Engine with DEFLATE decompression
  - Regular expression (regex) pattern matching
    - Built-in case insensitivity, wildcard support, no pattern explosion
    - Cross-packet pattern detection

  - Fast pattern database compilation and fast incremental updates
  - 16000 patterns, each up to 128 bytes in length
  - Patterns can be split into 256 sets, each of which can contain 16 subsets
- Stateful rule engine enables hardware execution of state-aware logic when a pattern is found
  - Useful for contextual searches, multi-pattern signatures, or for performing additional checks after a pattern is found
  - Capable of capturing and utilizing data from the data stream (such as LENGTH field) and using that information in subsequent pattern searches (for example, positive match only if pattern is detected within the number of bytes specified in the LENGTH field)
  - 8192 stateful rules
- Deflate engine
  - Supports decompression of DEFLATE compression format including zlib and gzip
  - Can work independently or in conjunction with the Pattern Matching Engine (that is decompressed data can be passed directly to the Pattern Matching Engine without further software involvement or memory copying)

- Two Table Lookup Units (TLU)
  - Hardware-based lookup engine offloads table searches from e500 cores
  - Longest prefix match, exact match, chained hash, and flat data table formats
  - Up to 32 tables, with each table up to 16M entries
  - 32-, 64-, 96-, or 128-bit keys
- Two $I^2C$ controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset the $I^2C$ interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended $I^2C$ addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Enhanced local bus controller (eLBC)
  - Multiplexed 32-bit address and data bus operating at up to 150 MHz
  - Eight chip selects support eight external slaves
  - Up to 8-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.

  - Three protocol engines available on a per-chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - NAND Flash control machine (FCM)
  - Parity support
  - Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over

  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- 10/100 Fast Ethernet controller (FEC) management interface
  - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
  - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
  - Four DMA channels per controller
  - All channels accessible by the local masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
  - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins ($\overline{\text{DMA2_DREQ}}$[2]) is made available
  - Ability to launch DMA from single write transaction
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification, Revision 1.2*
  - Both 1x and 4x LP-serial link interfaces
  - Long- and short-haul electricals with selectable pre-compensation
  - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane

  - Auto-detection of 1x- and 4x-mode operation during port initialization
  - Link initialization and synchronization
  - Large and small size transport information field support selectable at initialization time
  - 34-bit addressing
  - Up to 256 bytes data payload
  - All transaction flows and priorities
  - Atomic set/clr/inc/dec for read-modify-write operations
  - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
  - Receiver-controlled flow control
  - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
  - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
  - Hardware recovery only
  - Register support is not required for software-mediated error recovery.
  - Accept-all mode of operation for fail-over support
  - Support for RapidIO error injection
  - Internal LP-serial and application interface-level loopback modes
  - Memory and PHY BIST for at-speed production test
- RapidIO–compliant message unit
  - 4 Kbytes of payload per message
  - Up to sixteen 256-byte segments per message
  - Two inbound data message structures within the inbox
  - Capable of receiving three letters at any mailbox
  - Two outbound data message structures within the outbox
  - Capable of sending three letters simultaneously
  - Single segment multicast to up to 32 devIDs
  - Chaining and direct modes in the outbox
  - Single inbound doorbell message structure
  - Facility to accept port-write messages
- Three PCI Express controllers
  - PCI Express 1.0a compatible
  - Supports x8, x4, x2, and x1 link widths (see following bullet for specific width configuration options)
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing

  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Full 64-bit decode with 36-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
  - Single x8/x4/x2/x1 PCI Express
  - Dual x4/x2/x1 PCI Express
  - Single x4/x2/x1 PCI Express and dual x2/x1 PCI Express
  - Single 1x/4x Serial RapidIO and single x4/x2/x1 PCI Express
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, that automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the eight counters
  - Supports duration and quantity threshold counting
  - Permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™ compatible, JTAG boundary scan
- 1023 FC-PBGA package

Figure 1 shows the MPC8572E block diagram.

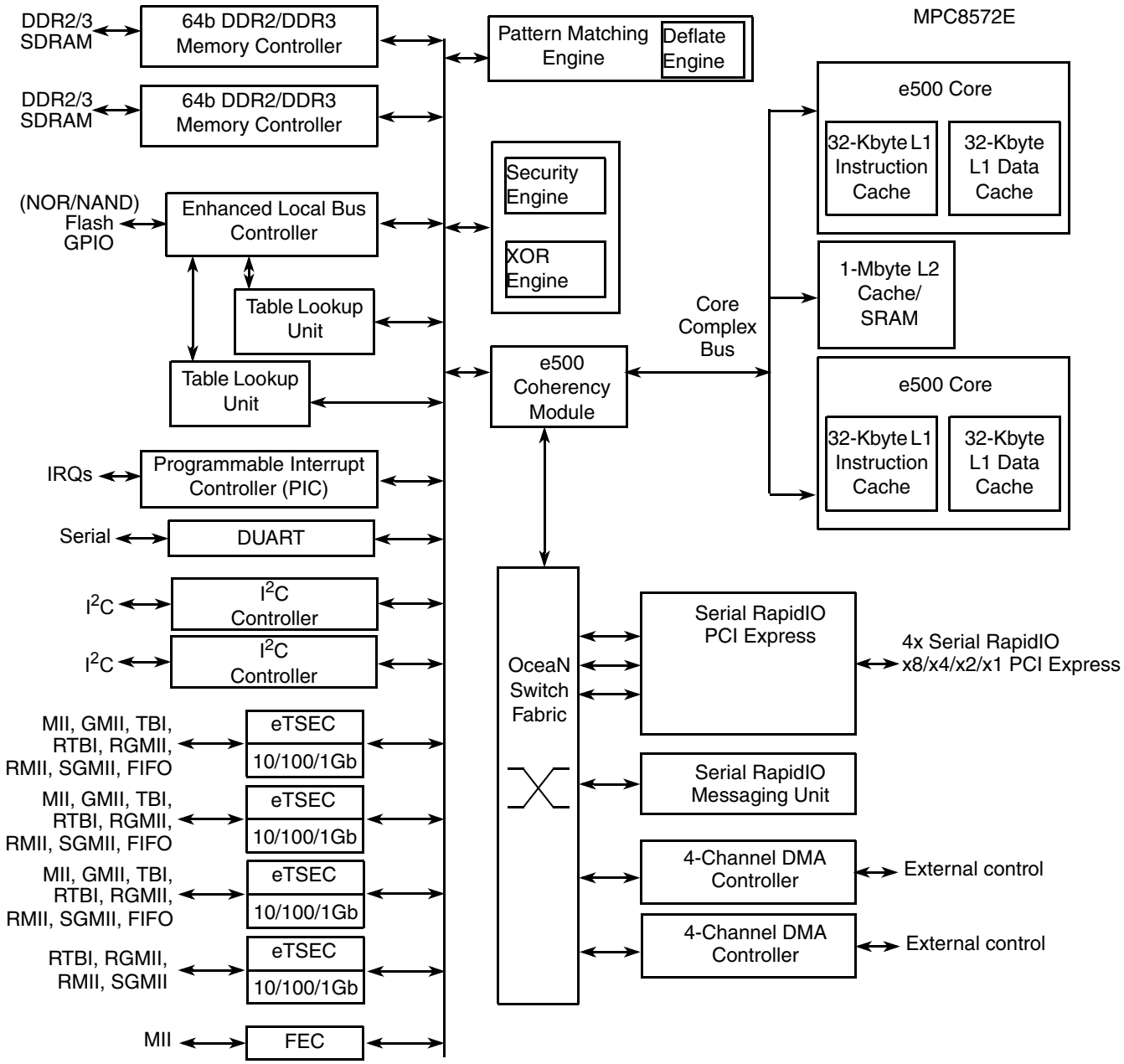



**Figure 1. MPC8572E Block Diagram**

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8572E. The MPC8572E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Range | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 1.21 | V | — |
| PLL supply voltage | | $AV_{DD}$ | –0.3 to 1.21 | V | — |
| Core power supply for SerDes transceivers | | $SV_{DD}$ | –0.3 to 1.21 | V | — |
| Pad power supply for SerDes transceivers | | $XV_{DD}$ | –0.3 to 1.21 | V | — |
| DDR SDRAM Controller I/O supply voltage | DDR2 SDRAM Interface | $GV_{DD}$ | –0.3 to 1.98 | V | — |
| | DDR3 SDRAM Interface | — | –0.3 to 1.65 | | — |
| Three-speed Ethernet I/O, FEC management interface, MII management voltage | | $LV_{DD}$ (for eTSEC1 and eTSEC2)<br>$TV_{DD}$ (for eTSEC3 and eTSEC4, FEC) | –0.3 to 3.63<br>–0.3 to 2.75<br>–0.3 to 3.63<br>–0.3 to 2.75 | V<br>—<br>— | 2<br>2 |
| DUART, system control and power management, $I^2C$, and JTAG I/O voltage | | $OV_{DD}$ | –0.3 to 3.63 | V | — |
| Local bus and GPIO I/O voltage | | $BV_{DD}$ | –0.3 to 3.63<br>–0.3 to 2.75<br>–0.3 to 1.98 | V | — |
| Input voltage | DDR2 and DDR3 SDRAM interface signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 3 |
| | DDR2 and DDR3 SDRAM interface reference | $MV_{REF}n$ | –0.3 to ($GV_{DD}$/2 + 0.3) | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3)<br>–0.3 to ($TV_{DD}$ + 0.3) | V | 3 |
| | Local bus and GPIO signals | $BV_{IN}$ | –0.3 to ($BV_{DD}$ + 0.3) | — | — |
| | DUART, SYSCLK, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 3 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
3. (M,L,O)$V_{IN}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

## 2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values shown are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

**Table 2. Recommended Operating Conditions**

| Characteristic | | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | 1.1 V ± 55 mV | V | — |
| PLL supply voltage | | $AV_{DD}$ | 1.1 V ± 55 mV | V | 1 |
| Core power supply for SerDes transceivers | | $SV_{DD}$ | 1.1 V ± 55 mV | V | — |
| Pad power supply for SerDes transceivers | | $XV_{DD}$ | 1.1 V ± 55 mV | V | — |
| DDR SDRAM Controller I/O supply voltage | DDR2 SDRAM Interface | $GV_{DD}$ | 1.8 V ± 90 mV | V | — |
| | DDR3 SDRAM Interface | | 1.5 V ± 75 mV | | — |
| Three-speed Ethernet I/O voltage | | $LV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV | V | 4 |
| | | $TV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV | | 4 |
| DUART, system control and power management, $I^2C$, and JTAG I/O voltage | | $OV_{DD}$ | 3.3 V ± 165 mV | V | 3 |
| Local bus and GPIO I/O voltage | | $BV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | — |
| Input voltage | DDR2 and DDR3 SDRAM Interface signals | $MV_{IN}$ | GND to $GV_{DD}$ | V | 2 |
| | DDR2 and DDR3 SDRAM Interface reference | $MV_{REF}n$ | $GV_{DD}/2$ ± 1% | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | GND to $LV_{DD}$<br>GND to $TV_{DD}$ | V | 4 |
| | Local bus and GPIO signals | $BV_{IN}$ | GND to $BV_{DD}$ | V | — |
| | Local bus, DUART, SYSCLK, Serial RapidIO, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | GND to $OV_{DD}$ | V | 3 |
| Junction temperature range | | $T_J$ | 0 to 105 | °C | — |

**Notes:**
1. This voltage is the input to the filter discussed in Section 21.2.1, "PLL Power Supply Filtering," and not necessarily the voltage at the $AV_{DD}$ pin, that may be reduced from $V_{DD}$ by the filter.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $L/TV_{IN}$ must not exceed $L/TV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8572E.

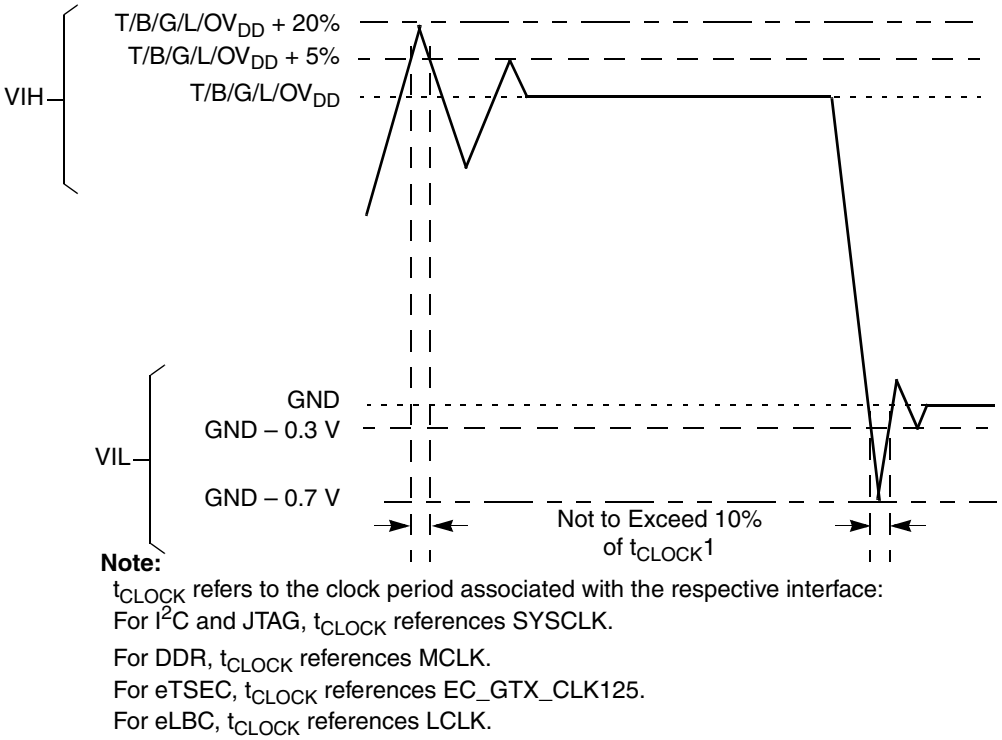



**Figure 2. Overshoot/Undershoot Voltage for $TV_{DD}/BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$**

The core voltage must always be provided at nominal 1.1 V. (See Table 2 for actual recommended core voltage.) Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, and $LV_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied $MV_{REF}n$ signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

### 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

**Table 3. Output Drive Capability**

| Driver Type | Programmable Output Impedance (Ω) | Supply Voltage | Notes |
|---|---|---|---|
| Local bus interface utilities signals | 25<br>35 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V | 1 |
| | 45(default)<br>45(default)<br>125 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V<br>$BV_{DD}$ = 1.8 V | |
| DDR2 signal | 18<br>36 (half strength mode) | $GV_{DD}$ = 1.8 V | 2 |
| DDR3 signal | 20<br>40 (half strength mode) | $GV_{DD}$ = 1.5 V | 2 |
| eTSEC/10/100 signals | 45 | $L/TV_{DD}$ = 2.5/3.3 V | — |
| DUART, system control, JTAG | 45 | $OV_{DD}$ = 3.3 V | — |
| I2C | 150 | $OV_{DD}$ = 3.3 V | — |

**Notes:**
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at $T_j$ = 105°C and at $GV_{DD}$ (min).

## 2.2 Power Sequencing

The MPC8572E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. $V_{DD}$, $AV_{DD}_n$, $BV_{DD}$, $LV_{DD}$, $OV_{DD}$, $SV_{DD_SRDS1}$ and $SV_{DD_SRDS2}$, $TV_{DD}$, $XV_{DD_SRDS1}$ and $XV_{DD_SRDS2}$
2. $GV_{DD}$

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

To guarantee MCKE low during power-on reset, the above sequencing for $GV_{DD}$ is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-on reset, then the sequencing for $GV_{DD}$ is not required.

**NOTE**

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-on reset, and extra current may be drawn by the device.

# 3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with out the L in its part ordering is shown in Table 4.

**Table 4. MPC8572E Power Dissipation [1]**

| CCB Frequency | Core Frequency | Typical-65[2] | Typical-105[3] | Maximum[4] | Unit |
|---|---|---|---|---|---|
| 533 | 1067 | 12.3 | 17.8 | 18.5 | W |
| 533 | 1200 | 12.3 | 17.8 | 18.5 | W |
| 533 | 1333 | 16.3 | 22.8 | 24.5 | W |
| 600 | 1500 | 17.3 | 23.9 | 25.9 | W |

**Notes:**

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/$XV_{DD}$ rails.
2. Typical-65 is based on $V_{DD}$ = 1.1 V, $T_j$ = 65 °C, running Dhrystone.
3. Typical-105 is based on $V_{DD}$ = 1.1 V, $T_j$ = 105 °C, running Dhrystone.
4. Maximum is based on $V_{DD}$ = 1.1 V, $T_j$ = 105 °C, running a smoke test.

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with the L in its port ordering is shown in Table 5.

**Table 5. MPC8572EL Power Dissipation [1]**

| CCB Frequency | Core Frequency | Typical-65[2] | Typical-105[3] | Maximum[4] | Unit |
|---|---|---|---|---|---|
| 533 | 1067 | 12 | 15 | 15.8 | W |
| 533 | 1200 | 12 | 15.5 | 16.3 | W |
| 533 | 1333 | 12 | 15.9 | 16.9 | W |
| 600 | 1500 | 13 | 18.7 | 20.0 | W |

**Notes:**

1. This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/$XV_{DD}$ rails.
2. Typical-65 is based on $V_{DD}$ = 1.1 V, $T_j$ = 65 °C, running Dhrystone.
3. Typical-105 is based on $V_{DD}$ = 1.1 V, $T_j$ = 105 °C, running Dhrystone.
4. Maximum is based on $V_{DD}$ = 1.1 V, $T_j$ = 105 °C, running a smoke test.

# 4 Input Clocks

## 4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

**Table 6. SYSCLK AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3V ± 5%.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | 33 | — | 133 | MHz | 1 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 7.5 | — | 30.3 | ns | — |
| SYSCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 1.2 | ns | 2 |
| SYSCLK duty cycle | $t_{KHK}/t_{SYSCLK}$ | 40 | — | 60 | % | 3 |
| SYSCLK jitter | — | — | — | +/– 150 | ps | 4, 5, 6 |

**Notes:**

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

## 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

## 4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8572E.

**Table 7. EC_GTX_CLK125 AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3V ± 5% or 2.5V ± 5%

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 frequency | $f_{G125}$ | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |

**Table 7. EC_GTX_CLK125 AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3V ± 5% or 2.5V ± 5% (continued)

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 rise and fall time<br>$L/TV_{DD}$=2.5V<br>$L/TV_{DD}$=3.3V | $t_{G125R}$, $t_{G125F}$ | — | — | <br>0.75<br>1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle<br>GMII, TBI<br>1000Base-T for RGMII, RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 2, 3 |

**Notes:**

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for $L/TV_{DD}$=2.5V, and from 0.6V and 2.7V for $L/TV_{DD}$=3.3V.
2. Timing is guaranteed by design and characterization.
3. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*_GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

## 4.4 DDR Clock Timing

Table 8 provides the DDR clock (DDRCLK) AC timing specifications for the MPC8572E.

**Table 8. DDRCLK AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3V ± 5%.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| DDRCLK frequency | $f_{DDRCLK}$ | 66 | — | 100 | MHz | 1 |
| DDRCLK cycle time | $t_{DDRCLK}$ | 10.0 | — | 15.15 | ns | — |
| DDRCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 1.2 | ns | 2 |
| DDRCLK duty cycle | $t_{KHK}/t_{DDRCLK}$ | 40 | — | 60 | % | 3 |
| DDRCLK jitter | — | — | — | +/– 150 | ps | 4, 5, 6 |

**Notes:**

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to Section 19.4, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The DDRCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
6. For spread spectrum clocking, guidelines are +0% to –1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

## 4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/4.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

FIFO TX/RX clock frequency <= platform clock (CCB) frequency/3.2

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

## 4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

# 5 RESET Initialization

Table 9 describes the AC electrical specifications for the RESET initialization timing.

**Table 9. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ | 100 | — | μs | 2 |
| Minimum assertion time for $\overline{\text{SRESET}}$ | 3 | — | SYSCLKs | 1 |
| PLL config input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation | 100 | — | μs | — |
| Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 4 | — | SYSCLKs | 1 |
| Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 2 | — | SYSCLKs | 1 |
| Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$ | — | 5 | SYSCLKs | 1 |

**Notes:**

1. SYSCLK is the primary clock input for the MPC8572E.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.

Table 10 provides the PLL lock times.

**Table 10. PLL Lock Times**

| Parameter/Condition | Symbol | Min | Typical | Max |
|---|---|---|---|---|
| PLL lock times | — | 100 | μs | — |
| Local bus PLL | — | 50 | μs | — |

# 6 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E. Note that the required $GV_{DD}$(typ) voltage is 1.8Vor 1.5 V when interfacing to DDR2 or DDR3 SDRAM, respectively.

## 6.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR2 SDRAM.

**Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.71 | 1.89 | V | 1 |
| I/O reference voltage | $MV_{REF}n$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF}n$ – 0.04 | $MV_{REF}n$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF}n$ + 0.125 | $GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF}n$ – 0.125 | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.420 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**
1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to $MV_{REF}n$. This rail should track variations in the DC level of $MV_{REF}n$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

**Table 12. DDR3 SDRAM Interface DC Electrical Characteristics for $GV_{DD}$(typ) = 1.5 V**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.425 | 1.575 | V | 1 |
| I/O reference voltage | $MV_{REF}n$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| Input high voltage | $V_{IH}$ | $MV_{REF}n$ + 0.100 | $GV_{DD}$ | V | — |
| Input low voltage | $V_{IL}$ | GND | $MV_{REF}n$ – 0.100 | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | μA | 3 |

**Notes:**
1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.
3. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

**Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for $GV_{DD}$(typ)=1.8 V and 1.5 V**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{IO}$ | 6 | 8 | pF | 1, 2 |
| Delta input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{DIO}$ | — | 0.5 | pF | 1, 2 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.
2. This parameter is sampled. $GV_{DD}$ = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.175 V.

Table 14 provides the current draw characteristics for $MV_{REF}n$.

**Table 14. Current Draw Characteristics for $MV_{REF}$ *n***

| Parameter / Condition | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Current draw for $MV_{REF}n$ | DDR2 SDRAM | $I_{MVREF}n$ | — | 1500 | μA | 1 |
| | DDR3 SDRAM | | | 1250 | | |

1. The voltage regulator for $MV_{REF}n$ must be able to supply up to 1500 μA or 1250 uA current for DDR2 or DDR3, respectively.

## 6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in

this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

### 6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

**Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5%

| Parameter | | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| AC input low voltage | >=667 MHz | $V_{ILAC}$ | — | $MV_{REF}n - 0.20$ | V | — |
| | <= 533 MHz | | — | $MV_{REF}n - 0.25$ | | |
| AC input high voltage | >=667 MHz | $V_{IHAC}$ | $MV_{REF}n + 0.20$ | — | V | — |
| — | <= 533 MHz | | $MV_{REF}n + 0.25$ | — | | |

**Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.5 V ± 5%. DDR3 data rate is between 606 MHz and 800 MHz.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{ILAC}$ | — | $MV_{REF}n - 0.175$ | V | — |
| AC input high voltage | $V_{IHAC}$ | $MV_{REF}n + 0.175$ | — | V | — |

**Table 17. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Controller Skew for MDQS—MDQ/MECC | $t_{CISKEW}$ | — | — | ps | 1, 2 |
| 800 MHz | — | –200 | 200 | — | — |
| 667 MHz | — | –240 | 240 | — | — |
| 533 MHz | — | –300 | 300 | — | — |
| 400 MHz | — | –365 | 365 | — | — |

**Note:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called tDISKEW.This can be determined by the following equation: tDISKEW =+/–(T/4 – abs(tCISKEW)) where T is the clock period and abs(tCISKEW) is the absolute value of tCISKEW.

Figure 3 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

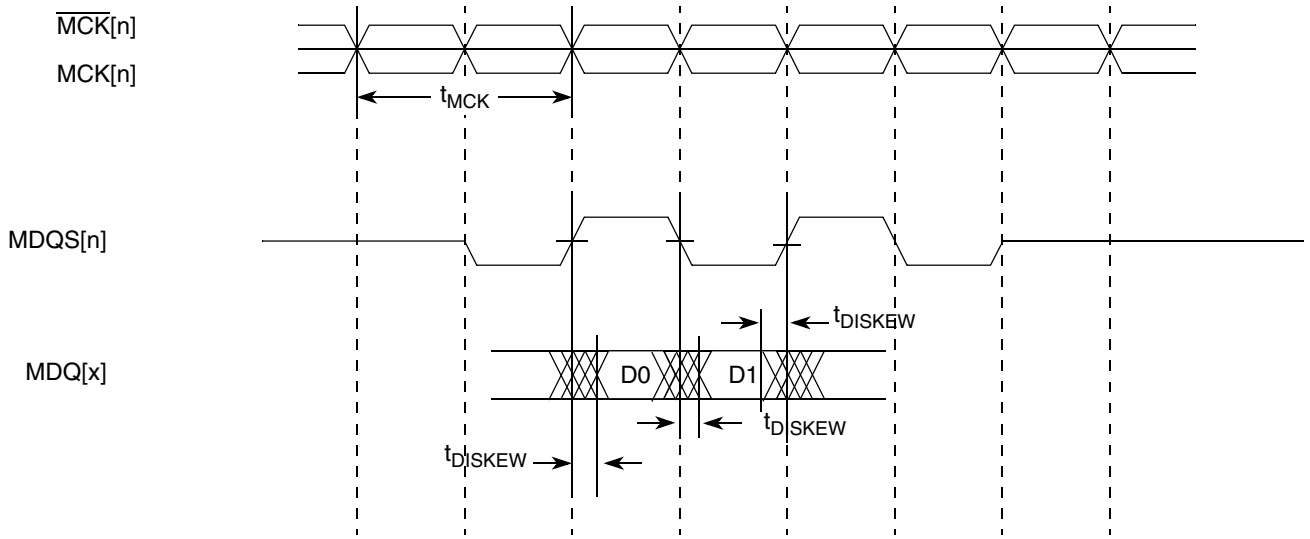



**Figure 3. DDR2 and DDR3 SDRAM Interface Input Timing Diagram**

## 6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 18 contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

**Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time | $t_{MCK}$ | 2.5 | 5 | ns | 2 |
| ADDR/CMD output setup with respect to MCK | $t_{DDKHAS}$ | | | ns | 3 |
| 800 MHz | | 0.917 | — | | |
| 667 MHz | | 1.10 | — | | |
| 533 MHz | | 1.48 | — | | |
| 400 MHz | | 1.95 | — | | |
| ADDR/CMD output hold with respect to MCK | $t_{DDKHAX}$ | | | ns | 3 |
| 800 MHz | | 0.917 | — | | |
| 667 MHz | | 1.10 | — | | |
| 533 MHz | | 1.48 | — | | |
| 400 MHz | | 1.95 | — | | |
| $\overline{MCS}$[n] output setup with respect to MCK | $t_{DDKHCS}$ | | | ns | 3 |
| 800 MHz | | 0.917 | — | | |
| 667 MHz | | 1.10 | — | | |
| 533 MHz | | 1.48 | — | | |

**Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 400 MHz | $t_{DDKHCS}$ | 1.95 | — | ns | 3 |
| $\overline{MCS}$[n] output hold with respect to MCK | $t_{DDKHCX}$ | | | ns | 3 |
| 800 MHz | | 0.917 | — | | |
| 667 MHz | | 1.10 | — | | |
| 533 MHz | | 1.48 | — | | |
| 400 MHz | | 1.95 | — | | |
| MCK to MDQS Skew | $t_{DDKHMH}$ | | | ns | 4 |
| 800 MHz | | –0.375 | 0.375 | | |
| <= 667 MHz | | –0.6 | 0.6 | | |
| MDQ/MECC/MDM output setup with respect to MDQS | $t_{DDKHDS}$, $t_{DDKLDS}$ | | | ps | 5 |
| 800 MHz | | 375 | — | | |
| 667 MHz | | 450 | — | | |
| 533 MHz | | 538 | — | | |
| 400 MHz | | 700 | — | | |
| MDQ/MECC/MDM output hold with respect to MDQS | $t_{DDKHDX}$, $t_{DDKLDX}$ | | | ps | 5 |
| 800 MHz | | 375 | — | | |
| 667 MHz | | 450 | — | | |
| 533 MHz | | 538 | — | | |
| 400 MHz | | 700 | — | | |
| MDQS preamble start | $t_{DDKHMP}$ | | | ns | 6 |
| 800 MHz | | $-0.5 \times t_{MCK} - 0.375$ | $-0.5 \times t_{MCK} + 0.375$ | | |
| <= 667 MHz | | $-0.5 \times t_{MCK} - 0.6$ | $-0.5 \times t_{MCK} + 0.6$ | | |
| MDQS epilogue end | $t_{DDKHME}$ | | | ns | 6 |
| 800 MHz | | –0.375 | 0.375 | | |

**Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| <= 667 MHz | $t_{DDKHME}$ | –0.6 | 0.6 | ns | 6 |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.

**NOTE**

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 4 shows the DDR2 and DDR3 SDRAM Interface output timing for the MCK to MDQS skew measurement (tDDKHMH).

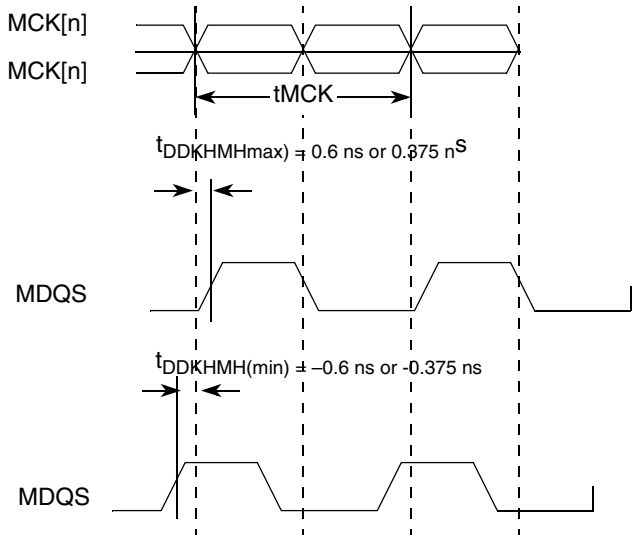



**Figure 4. Timing Diagram for tDDKHMH**

Figure 5 shows the DDR2 and DDR3 SDRAM Interface output timing diagram.

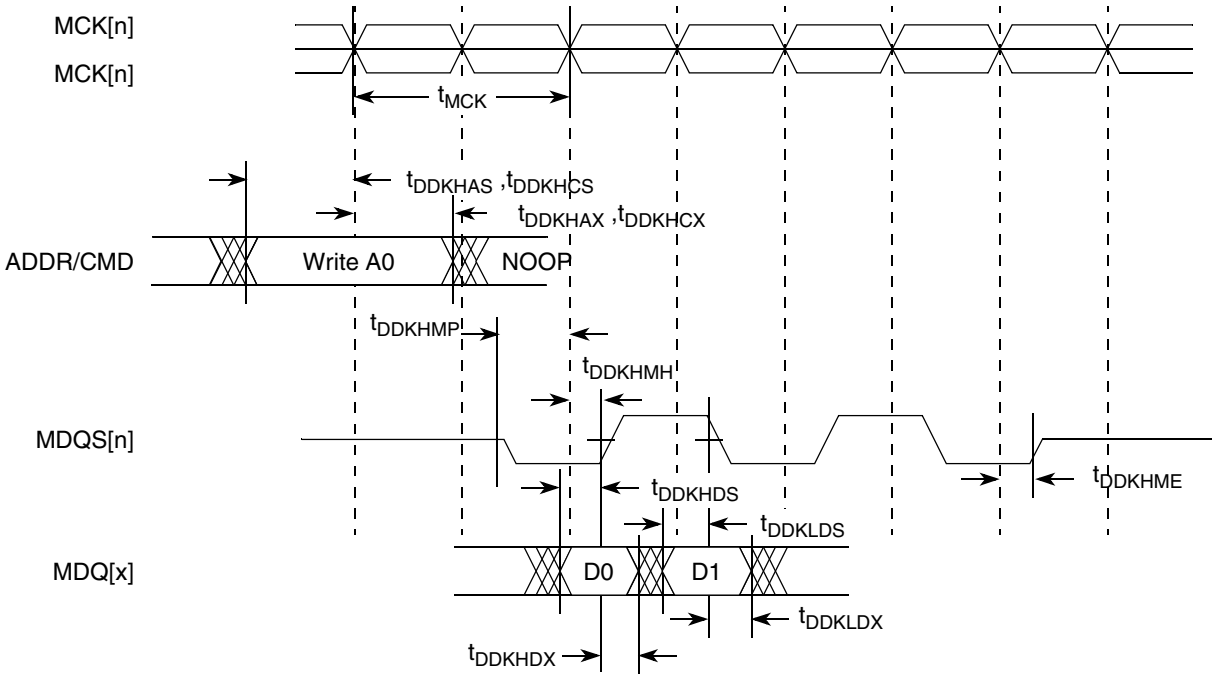



**Figure 5. DDR2 and DDR3 SDRAM Interface Output Timing Diagram**

Figure 6 provides the AC test load for the DDR2 and DDR3 Controller bus.

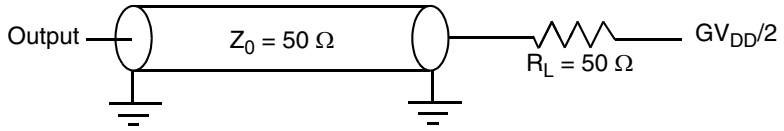
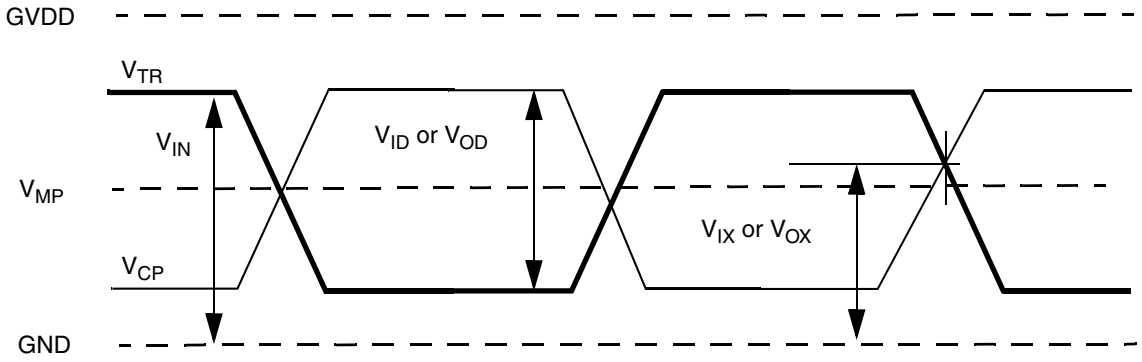



**Figure 6. DDR2 and DDR3 Controller bus AC Test Load**

## 6.2.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E.




**NOTE**

VID specifies the input differential voltage |VTR -VCP| required for switching, where VTR is the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 19 provides the differential specifications for the MPC8572E differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ when in DDR2 mode.

**Table 19. DDR2 SDRAM Differential Electrical Characteristics**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| DC Input Signal Voltage | $V_{IN}$ | –0.3 | $GV_{DD}$ + 0.3 | V | — |
| DC Differential Input Voltage | $V_{ID}$ | — | — | mV | — |
| AC Differential Input Voltage | $V_{IDAC}$ | — | — | mV | — |
| DC Differential Output Voltage | $V_{OH}$ | — | — | mV | — |
| AC Differential Output Voltage | $V_{OHAC}$ | JEDEC: 0.5 | JEDEC: $GV_{DD}$ + 0.6 | V | — |
| AC Differential Cross-point Voltage | $V_{IXAC}$ | — | — | mV | — |
| Input Midpoint Voltage | $V_{MP}$ | — | — | mV | — |

Table 20 provides the differential specifications for the MPC8572E differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ when in DDR3 mode.

**Table 20. DDR3 SDRAM Differential Electrical Characteristics**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| DC Input Signal Voltage | $V_{IN}$ | — | — | mV | — |
| DC Differential Input Voltage | $V_{ID}$ | — | — | mV | — |
| AC Differential Input Voltage | $V_{IDAC}$ | — | — | mV | — |
| DC Differential Output Voltage | $V_{OH}$ | — | — | mV | — |
| AC Differential Output Voltage | $V_{OHAC}$ | — | — | mV | — |
| AC Differential Cross-point Voltage | $V_{IXAC}$ | — | — | mV | — |
| Input Midpoint Voltage | $V_{MP}$ | — | — | mV | — |

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8572E.

## 7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

**Table 21. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | 3.13 | 3.47 | V |
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1.

## 7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

**Table 22. DUART AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3V ± 5%.

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | $f_{CCB}$/1,048,576 | baud | 1, 2 |
| Maximum baud rate | $f_{CCB}$/16 | baud | 1, 2, 3 |
| Oversample rate | 16 | — | 1, 4 |

**Notes:**
1. Guaranteed by design
2. $f_{CCB}$ refers to the internal platform clock frequency.
3. Actual attainable baud rate is limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the $8^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each $16^{th}$ sample.

# 8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

## 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all FIFO mode, gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC), and serial gigabit media independent interface (SGMII). The RGMII, RTBI and FIFO mode interfaces are defined for 2.5 V, while the GMII, MII, RMII, and TBI interfaces can operate at both 2.5 V and 3.3V .

The GMII, MII, or TBI interface timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998).

The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical Characteristics.”

The electrical characteristics for SGMII is specified in Section 8.3, “SGMII Interface Electrical Characteristics.” The SGMII interface conforms (with exceptions) to the Serial-GMII Specification Version 1.8.

The Fast Ethernet Controller (FEC) operates in MII mode only, and complies with the AC and DC electrical characteristics specified in this chapter for MII. Note that if FEC is used, eTSEC 3 and 4 are only available in SGMII mode.

### 8.1.1 eTSEC DC Electrical Characteristics

All MII, GMII, RMII, and TBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. All RGMII, RTBI and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 24. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$<br>$TV_{DD}$ | 3.13 | 3.47 | V | 1, 2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, IOH = –4.0 mA) | VOH | 2.40 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = Min, IOL = 4.0 mA) | VOL | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 2.0 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.90 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 40 | μA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –600 | — | μA | 3 |

**Notes:**

1 $LV_{DD}$ supports eTSECs 1 and 2.
2 $TV_{DD}$ supports eTSECs 3 and 4 or FEC.
3 The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1.

**Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics**

| Parameters | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}/TV_{DD}$ | 2.37 | 2.63 | V | 1,2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, IOH = –1.0 mA) | $V_{OH}$ | 2.00 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND – 0.3 | 0.40 | V | — |
| Input high voltage | $V_{IH}$ | 1.70 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.70 | V | — |

**Table 24. MII, GMII, RMII, RGMII, TBI, RTBI, and FIFO DC Electrical Characteristics (continued)**

| Parameters | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 10 | μA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | μA | 3 |

**Note:**

1 $LV_{DD}$ supports eTSECs 1 and 2.
2 $TV_{DD}$ supports eTSECs 3 and 4 or FEC.
3 Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1.

## 8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

### 8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, because they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back on the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, because the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is a relationship between the maximum FIFO speed and the platform (CCB) frequency. For more information see Section 4.5, "Platform to eTSEC FIFO Restrictions."

Table 25 and Table 26 summarize the FIFO AC specifications.

**Table 25. FIFO Mode Transmit AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period[1] | $t_{FIT}$ | 5.3 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}/t_{FIT}$ | 45 | 50 | 55 | % |
| TX_CLK, GTX_CLK peak-to-peak jitter | $t_{FITJ}$ | — | — | 250 | ps |

**Table 25. FIFO Mode Transmit AC Timing Specification (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Rise time TX_CLK (20%–80%) | $t_{FITR}$ | — | — | 0.75 | ns |
| Fall time TX_CLK (80%–20%) | $t_{FITF}$ | — | — | 0.75 | ns |
| FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK | $t_{FITDV}$ | 2.0 | — | — | ns |
| GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time | $t_{FITDX}$ | 0.5 | — | 3.0 | ns |

**Notes:**

1. The minimum cycle period (or maximum frequency) of the TX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to Section 4.5, "Platform to eTSEC FIFO Restrictions," for more detailed description.

**Table 26. FIFO Mode Receive AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period[1] | $t_{FIR}$ | 5.3 | 8.0 | 100 | ns |
| RX_CLK duty cycle | $t_{FIRH}/t_{FIR}$ | 45 | 50 | 55 | % |
| RX_CLK peak-to-peak jitter | $t_{FIRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{FIRR}$ | — | — | 0.75 | ns |
| Fall time RX_CLK (80%–20%) | $t_{FIRF}$ | — | — | 0.75 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{FIRDV}$ | 1.5 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{FIRDX}$ | 0.5 | — | — | ns |

1. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to Section 4.5, "Platform to eTSEC FIFO Restrictions," for more detailed description.

Figure 7 and Figure 8 show the FIFO timing diagrams.

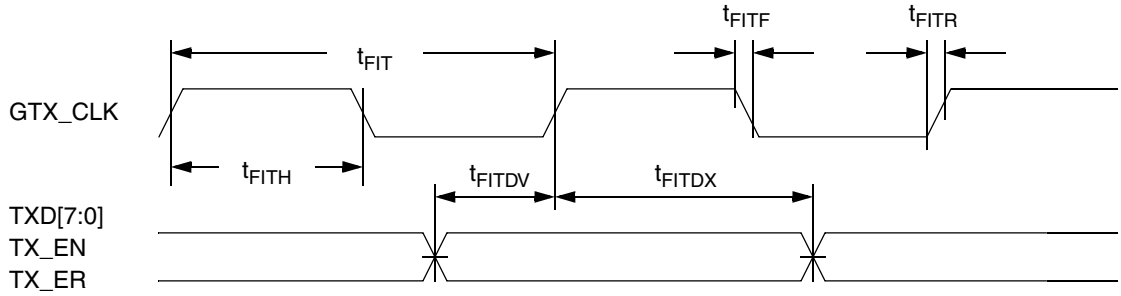



**Figure 7. FIFO Transmit AC Timing Diagram**

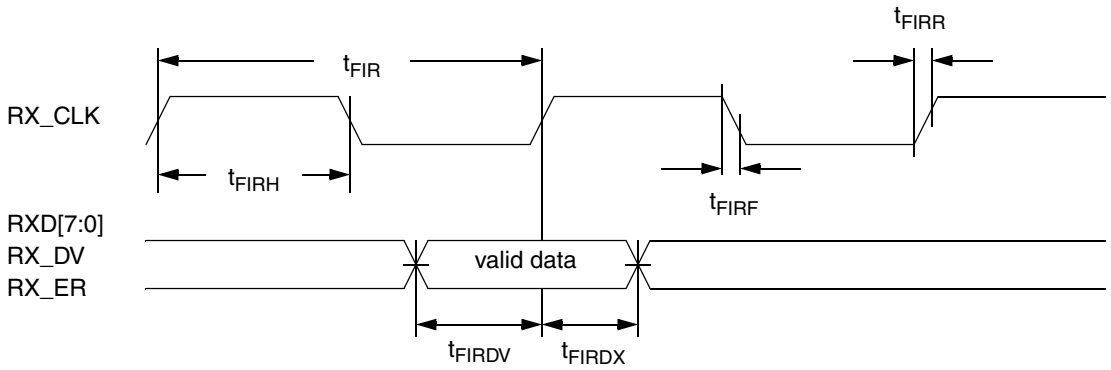



**Figure 8. FIFO Receive AC Timing Diagram**

## 8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### 8.2.2.1 GMII Transmit AC Timing Specifications

Table 27 provides the GMII transmit AC timing specifications.

**Table 27. GMII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GMII data TXD[7:0], TX_ER, TX_EN setup time | $t_{GTKHDV}$ | 2.5 | — | — | ns |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$ | 0.5 | — | 5.0 | ns |
| GTX_CLK data clock rise time (20%-80%) | $t_{GTXR}$[2] | — | — | 1.0 | ns |
| GTX_CLK data clock fall time (80%-20%) | $t_{GTXF}$[2] | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GTKHDV}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, $t_{GTKHDX}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GTX}$ represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 9 shows the GMII transmit AC timing diagram.

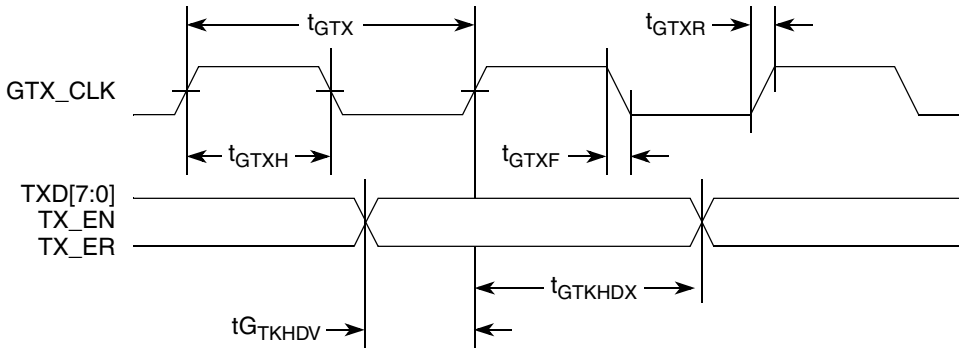



**Figure 9. GMII Transmit AC Timing Diagram**

### 8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

**Table 28. GMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$ | — | 8.0 | — | ns |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 40 | — | 60 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{GRDXKH}$ | 0 | — | — | ns |
| RX_CLK clock rise (20%-80%) | $t_{GRXR}$[2] | — | — | 1.0 | ns |
| RX_CLK clock fall time (80%-20%) | $t_{GRXF}$[2] | — | — | 1.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, $t_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{GRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 10 provides the AC test load for eTSEC.

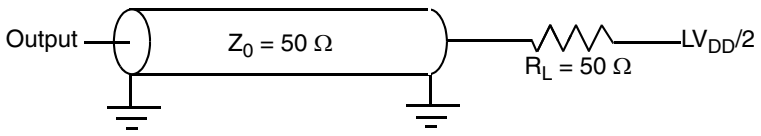



**Figure 10. eTSEC AC Test Load**

Figure 11 shows the GMII receive AC timing diagram.

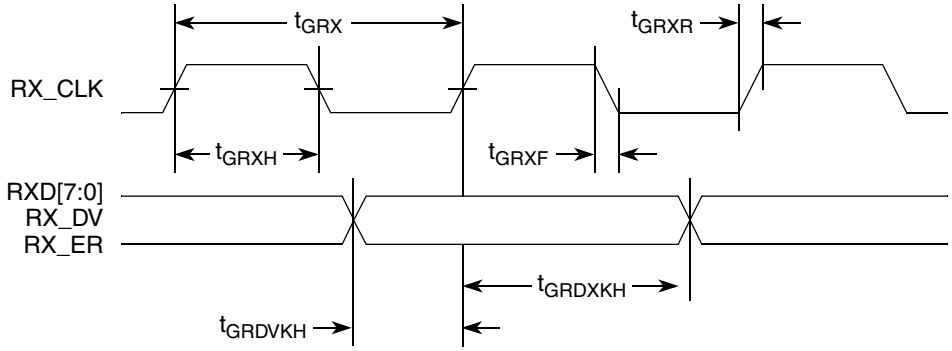



**Figure 11. GMII Receive AC Timing Diagram**

## 8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

**Table 29. MII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$[2] | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 1 | 5 | 15 | ns |
| TX_CLK data clock rise (20%-80%) | $t_{MTXR}$[2] | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall (80%-20%) | $t_{MTXF}$[2] | 1.0 | — | 4.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 shows the MII transmit AC timing diagram.

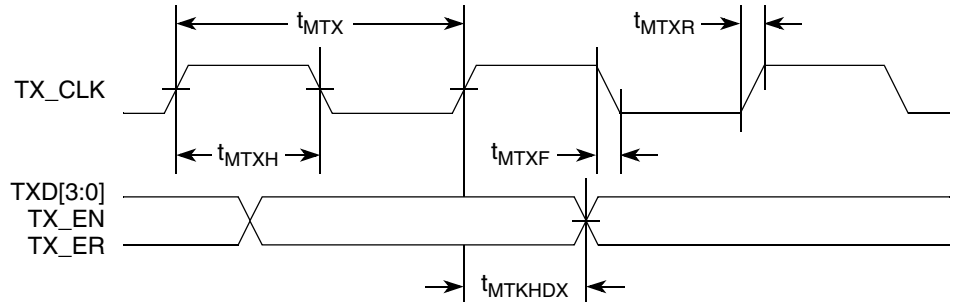



**Figure 12. MII Transmit AC Timing Diagram**

### 8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

**Table 30. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$[2] | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise (20%-80%) | $t_{MRXR}$[2] | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%-20%) | $t_{MRXF}$[2] | 1.0 | — | 4.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

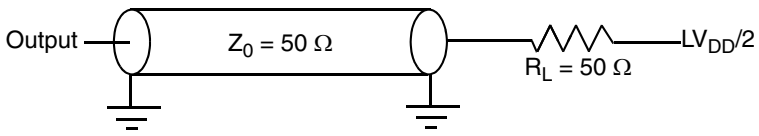



**Figure 13. eTSEC AC Test Load**

Figure 14 shows the MII receive AC timing diagram.

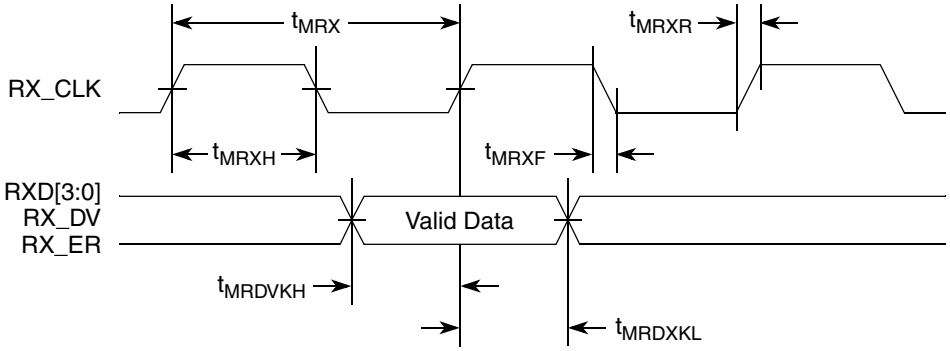



**Figure 14. MII Receive AC Timing Diagram**

## 8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 8.2.4.1 TBI Transmit AC Timing Specifications

Table 31 provides the TBI transmit AC timing specifications.

**Table 31. TBI Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TCG[9:0] setup time GTX_CLK going high | $t_{TTKHDV}$ | 2.0 | — | — | ns |
| TCG[9:0] hold time from GTX_CLK going high | $t_{TTKHDX}$ | 1.0 | — | — | ns |
| GTX_CLK rise (20%–80%) | $t_{TTXR}$[2] | — | — | 1.0 | ns |
| GTX_CLK fall time (80%–20%) | $t_{TTXF}$[2] | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TTKHDV}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, $t_{TTKHDX}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TTX}$ represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 15 shows the TBI transmit AC timing diagram.

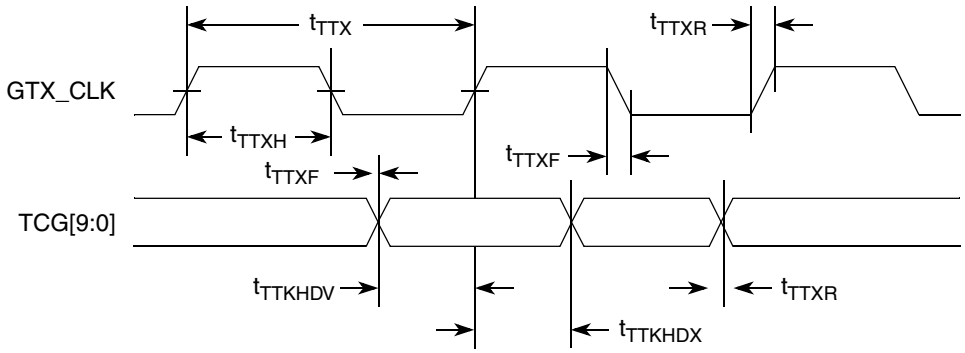



**Figure 15. TBI Transmit AC Timing Diagram**

### 8.2.4.2 TBI Receive AC Timing Specifications

Table 32 provides the TBI receive AC timing specifications.

**Table 32. TBI Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition [3] | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock period for TBI Receive Clock 0, 1 | $t_{TRX}$ | — | 16.0 | — | ns |
| Skew for TBI Receive Clock 0, 1 | $t_{SKTRX}$ | 7.5 | — | 8.5 | ns |
| Duty cycle for TBI Receive Clock 0, 1 | $t_{TRXH}/t_{TRX}$ | 40 | — | 60 | % |
| RCG[9:0] setup time to rising edge of TBI Receive Clock 0, 1 | $t_{TRDVKH}$ | 2.5 | — | — | ns |
| RCG[9:0] hold time to rising edge of TBI Receive Clock 0, 1 | $t_{TRDXKH}$ | 1.5 | — | — | ns |
| Clock rise time (20%-80%) for TBI Receive Clock 0, 1 | $t_{TRXR}$[2] | 0.7 | — | 2.4 | ns |
| Clock fall time (80%-20%) for TBI Receive Clock 0, 1 | $t_{TRXF}$[2] | 0.7 | — | 2.4 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TRDVKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{TRDXKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TRX}$ represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. The signals “TBI Receive Clock 0” and “TBI Receive Clock 1” refer to TSECn_RX_CLK and TSECn_TX_CLK pins respectively. These two clock signals are also referred as PMA_RX_CLK[0:1].

Figure 16 shows the TBI receive AC timing diagram.

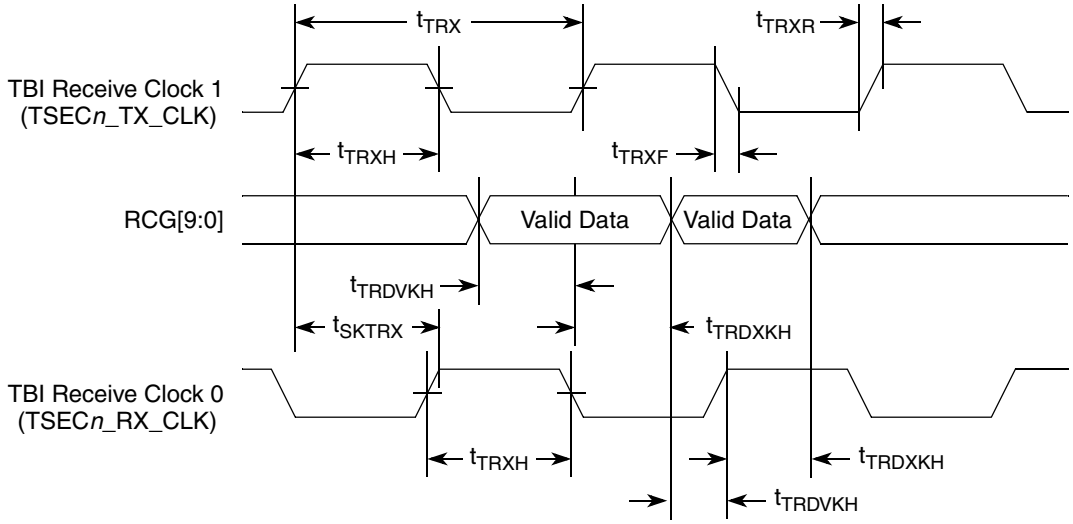



**Figure 16. TBI Receive AC Timing Diagram**

## 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

**Table 33. TBI single-clock Mode Receive AC Timing Specification**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRRX}$ | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRRH}/t_{TRRX}$ | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDVKH}$ | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDXKH}$ | 1.0 | — | — | ns |

Figure 17 shows the TBI receive the timing diagram.

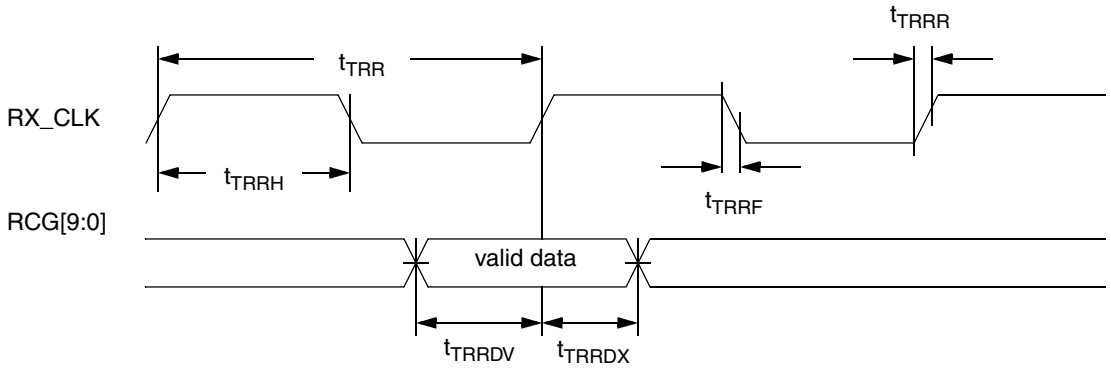



**Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram**

## 8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

**Table 34. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$ | –500 | 0 | 500 | ps |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.8 | ns |
| Clock period [3] | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 10BASE-T and 100BASE-TX [3, 4] | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns |

**Notes:**

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

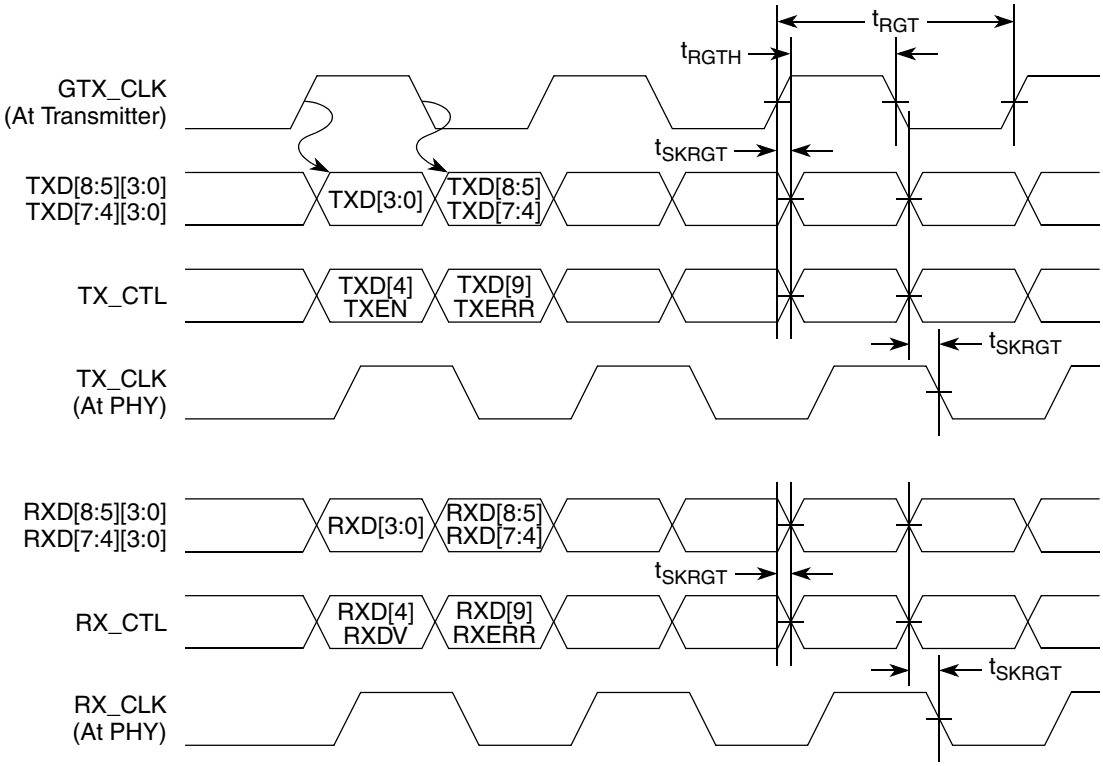



**Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams**

## 8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

### 8.2.7.1 RMII Transmit AC Timing Specifications

Table 35 shows the RMII transmit AC timing specifications.

**Table 35. RMII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSECn_TX_CLK clock period | $t_{RMT}$ | 15.0 | 20.0 | 25.0 | ns |
| TSECn_TX_CLK duty cycle | $t_{RMTH}$ | 35 | 50 | 65 | % |
| TSECn_TX_CLK peak-to-peak jitter | $t_{RMTJ}$ | — | — | 250 | ps |
| Rise time TSECn_TX_CLK (20%–80%) | $t_{RMTR}$ | 1.0 | — | 2.0 | ns |
| Fall time TSECn_TX_CLK (80%–20%) | $t_{RMTF}$ | 1.0 | — | 2.0 | ns |

**Table 35. RMII Transmit AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTDX}$ | 1.0 | — | 10.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 shows the RMII transmit AC timing diagram.

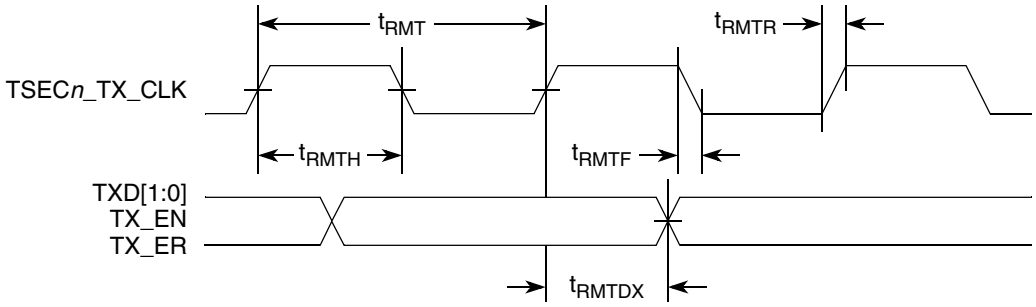



**Figure 19. RMII Transmit AC Timing Diagram**

### 8.2.7.2 RMII Receive AC Timing Specifications

Table 36 shows the RMII receive AC timing specifications.

**Table 36. RMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSECn_TX_CLK clock period | $t_{RMR}$ | 15.0 | 20.0 | 25.0 | ns |
| TSECn_TX_CLK duty cycle | $t_{RMRH}$ | 35 | 50 | 65 | % |
| TSECn_TX_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps |
| Rise time TSECn_TX_CLK (20%–80%) | $t_{RMRR}$ | 1.0 | — | 2.0 | ns |
| Fall time TSECn_TX_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 2.0 | ns |
| RXD[1:0], CRS_DV, RX_ER setup time to TSECn_TX_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns |

**Table 36. RMII Receive AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 2.5/ 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RXD[1:0], CRS_DV, RX_ER hold time to TSECn_TX_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 20 provides the AC test load for eTSEC.

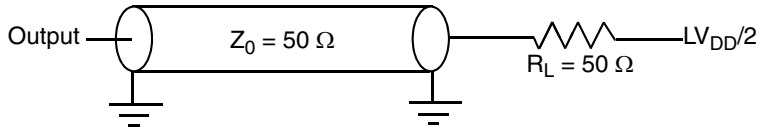



**Figure 20. eTSEC AC Test Load**

Figure 21 shows the RMII receive AC timing diagram.

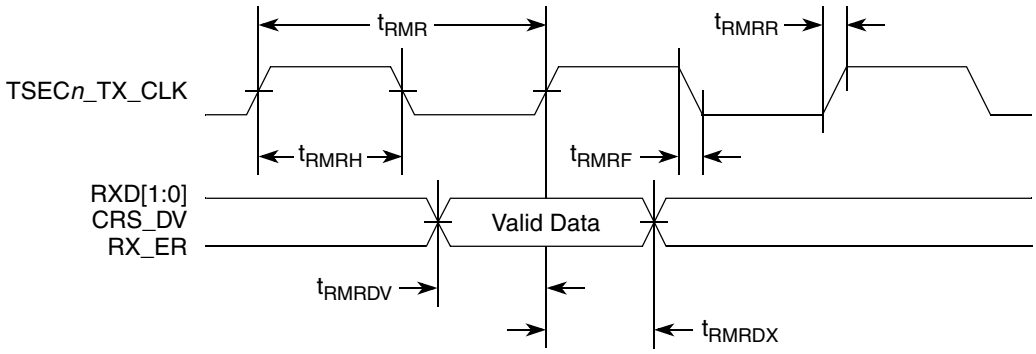



**Figure 21. RMII Receive AC Timing Diagram**

## 8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes 2 interface of MPC8572E as shown in Figure 22, where $C_{TX}$ is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SGND_SRDS2 (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 54.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 21.5, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ pins.

### 8.3.1 DC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 15, "High-Speed Serial Interfaces (HSSI)."

### 8.3.2 AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$

Table 37 lists the SGMII SerDes reference clock AC requirements. Note that SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

**Table 37. SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10 (8) | — | ns | 1 |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –50 | — | 50 | ps | — |

**Note:**
1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected through cfg_srds_sgmii_refclk during POR.

### 8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 38 and Table 39 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2_TX}}$[n]) as depicted in Figure 23.

**Table 38. SGMII DC Transmitter Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $XV_{DD_SRDS2}$ | 1.045 | 1.1 | 1.155 | V | — |
| Output high voltage | VOH | — | — | $XV_{DD_SRDS2\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$ | mV | 1 |
| Output low voltage | VOL | $XV_{DD_SRDS2\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$ | — | — | mV | 1 |
| Output ringing | $V_{RING}$ | — | — | 10 | % | — |
| Output differential voltage[2, 3, 5] | $\lvert V_{OD}\rvert$ | 359 | 550 | 791 | mV | Equalization setting: 1.0x |
| | | 329 | 505 | 725 | | Equalization setting: 1.09x |
| | | 299 | 458 | 659 | | Equalization setting: 1.2x |
| | | 270 | 414 | 594 | | Equalization setting: 1.33x |
| | | 239 | 367 | 527 | | Equalization setting: 1.5x |
| | | 210 | 322 | 462 | | Equalization setting: 1.71x |
| | | 180 | 275 | 395 | | Equalization setting: 2.0x |
| Output offset voltage | $V_{OS}$ | 473 | 550 | 628 | mV | 1, 4 |
| Output impedance (single-ended) | $R_O$ | 40 | — | 60 | Ω | — |
| Mismatch in a pair | $\Delta R_O$ | — | — | 10 | % | — |
| Change in $V_{OD}$ between “0” and “1” | $\Delta \lvert V_{OD}\rvert$ | — | — | 25 | mV | — |

**Table 38. SGMII DC Transmitter Electrical Characteristics (continued)**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Change in $V_{OS}$ between "0" and "1" | $\Delta V_{OS}$ | — | — | 25 | mV | — |
| Output current on short to GND | $I_{SA}$, $I_{SB}$ | — | — | 40 | mA | — |

**Note:**

1. This will not align to DC-coupled SGMII. $XV_{DD_SRDS2\text{-}Typ}$=1.1 V.
2. $|V_{OD}| = |V_{SD2_TXn} - V_{\overline{SD2_TXn}}|$. $|V_{OD}|$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{OD}|$.
3. The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes 2 lanes A & B) or XMITEQ**EF** (for SerDes 2 lanes E & E) bit field of MPC8572E's SerDes 2 Control Register:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. $V_{OS}$ is also referred to as output common mode voltage.
   - 5.The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD_SRDS2\text{-}Typ}$=1.1V, no common mode offset variation ($V_{OS}$ =550mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and $\overline{SD2_TX}$[n].

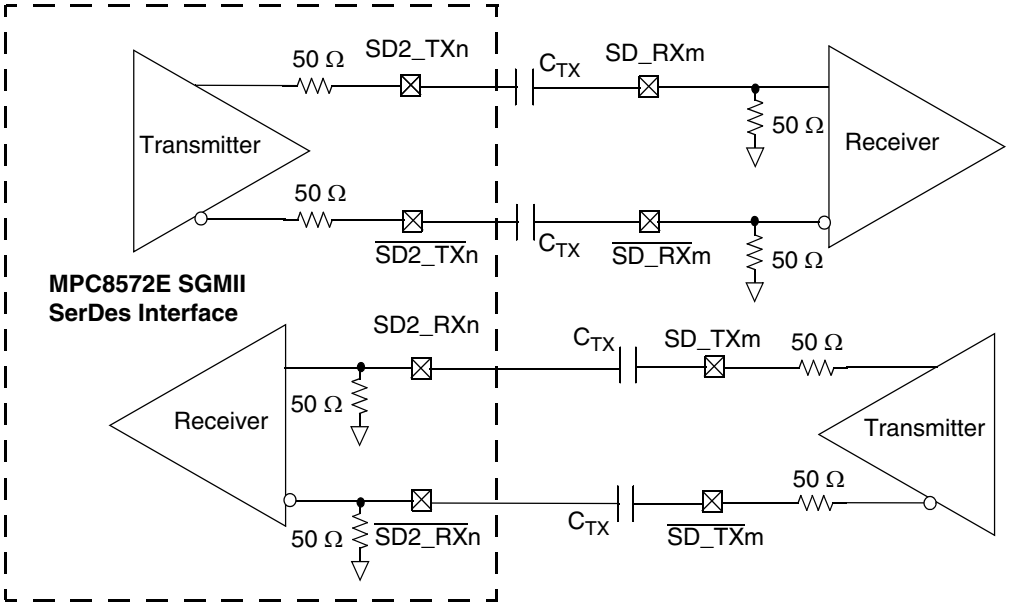



**Figure 22. 4-Wire AC-Coupled SGMII Serial Link Connection Example**

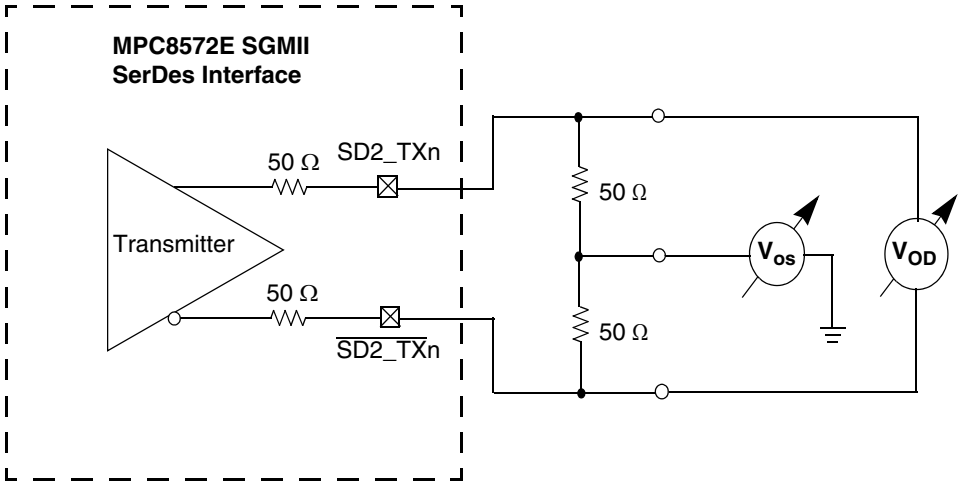



**Figure 23. SGMII Transmitter DC Measurement Circuit**

Table 39 lists the SGMII DC receiver electrical characteristics.

**Table 39. SGMII DC Receiver Electrical Characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $XV_{DD_SRDS2}$ | 1.045 | 1.1 | 1.155 | V | — |
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | LSTS = 0 | $V_{RX_DIFFp-p}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 1 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 0 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 1 | | 65 | — | 175 | | |
| Input AC common mode voltage | | $V_{CM_ACp-p}$ | | — | 100 | mV | 5 |
| Receiver differential input impedance | | $Z_{RX_DIFF}$ | 80 | 100 | 120 | Ω | — |
| Receiver common mode input impedance | | $Z_{RX_CM}$ | 20 | — | 35 | Ω | — |
| Common mode input voltage | | $V_{CM}$ | — | $V_{xcorevss}$ | — | V | 6 |

**Note:**

1. Input must be externally AC-coupled.
2. $V_{RX_DIFFp-p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTS**AB** or LSTS**EF** bit field of MPC8572E's SerDes 2 Control Register.
5. $V_{CM_ACp-p}$ is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

## 8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2_RX}}$[n]) as depicted in Figure 25, respectively.

### 8.3.4.1 SGMII Transmit AC Timing Specifications

Table 40 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

**Table 40. SGMII Transmit AC Timing Specifications**

At recommended operating conditions with $XV_{DD_SRDS2}$ = 1.1V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter | JD | — | — | 0.17 | UI p-p | — |
| Total Jitter | JT | — | — | 0.35 | UI p-p | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 1 |
| $V_{OD}$ fall time (80%-20%) | tfall | 50 | — | 120 | ps | — |
| $V_{OD}$ rise time (20%-80%) | $t_{rise}$ | 50 | — | 120 | ps | — |

**Notes:**
1. Each UI is 800 ps ± 100 ppm.

### 8.3.4.2 SGMII Receive AC Timing Specifications

Table 41 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 24 shows the SGMII receiver input compliance mask eye diagram.

**Table 41. SGMII Receive AC Timing Specifications**

At recommended operating conditions with $XV_{DD_SRDS2}$ = 1.1V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter Tolerance | JD | 0.37 | — | — | UI p-p | 1 |
| Combined Deterministic and Random Jitter Tolerance | JDR | 0.55 | — | — | UI p-p | 1 |
| Sinusoidal Jitter Tolerance | JSIN | 0.1 | — | — | UI p-p | 1 |
| Total Jitter Tolerance | JT | 0.65 | — | — | UI p-p | 1 |
| Bit Error Ratio | BER | — | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 2 |
| AC Coupling Capacitor | $C_{TX}$ | 5 | — | 200 | nF | 3 |

**Notes:**
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.
4. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.

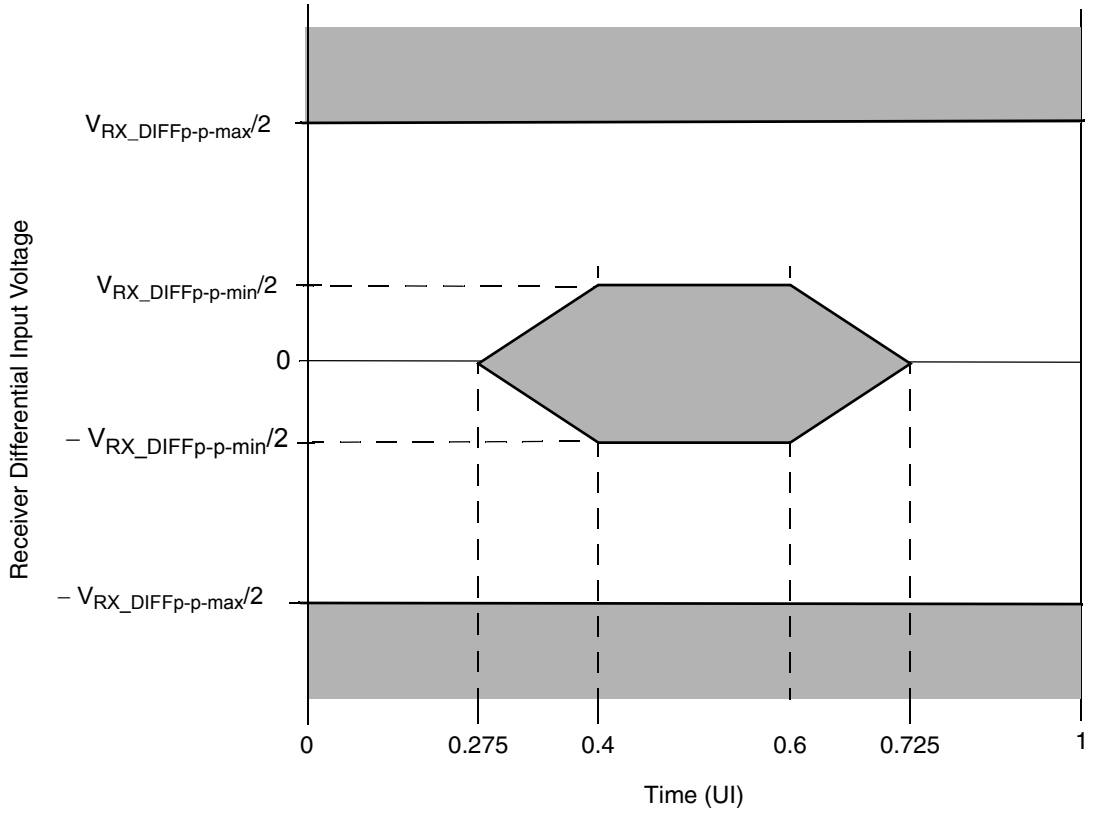



**Figure 24. SGMII Receiver Input Compliance Mask**

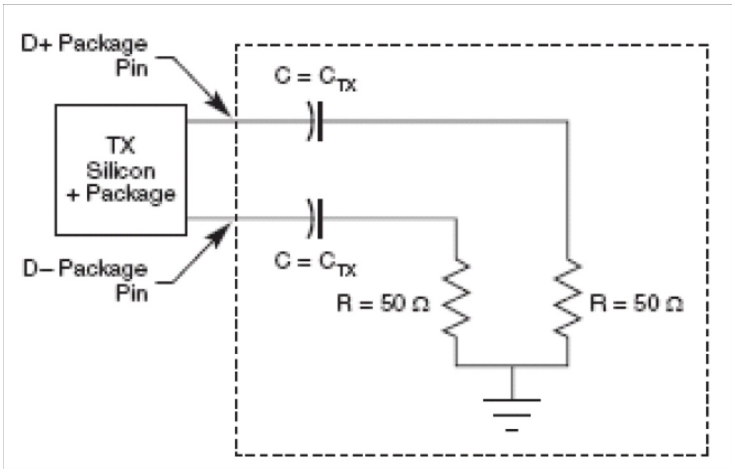



**Figure 25. SGMII AC Test/Measurement Load**

## 8.4 eTSEC IEEE Std 1588™ AC Specifications

Figure 26 shows the data and command output timing diagram.

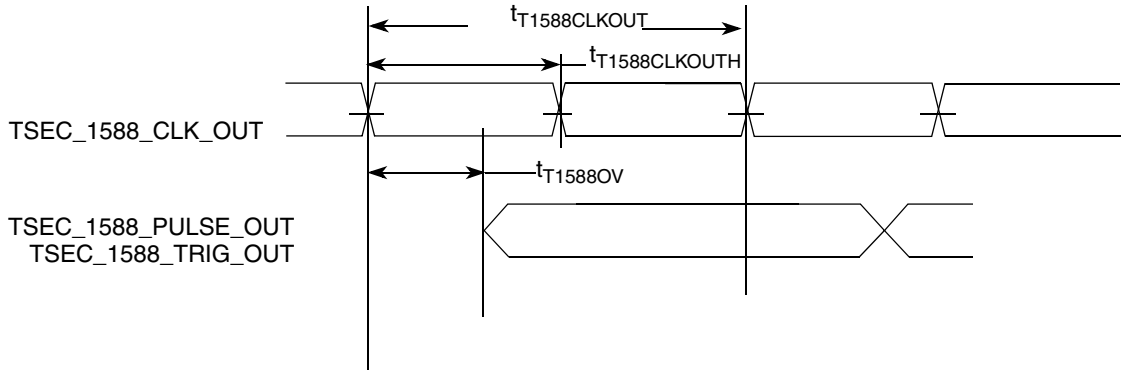



**Figure 26. eTSEC IEEE 1588 Output AC Timing**

1 The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 27 shows the data and command input timing diagram.

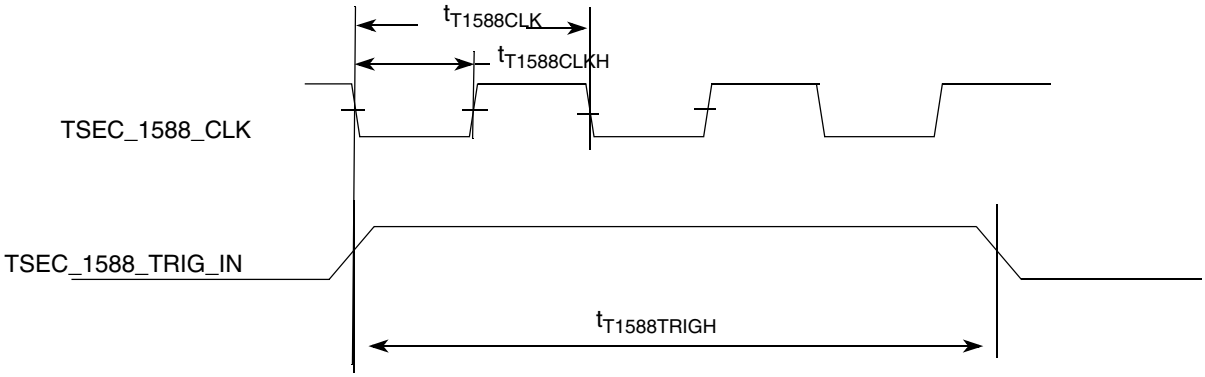



**Figure 27. eTSEC IEEE 1588 Input AC timing**

Table 42 provides the IEEE 1588 AC timing specifications.

**Table 42. eTSEC IEEE 1588 AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TSEC_1588_CLK clock period | $t_{T1588CLK}$ | 3.3 | — | $T_{TX_CLK}$*9 | ns | 1 |
| TSEC_1588_CLK duty cycle | $t_{T1588CLKH}$ /$t_{T1588CLK}$ | 40 | 50 | 60 | % | — |
| TSEC_1588_CLK peak-to-peak jitter | $t_{T1588CLKINJ}$ | — | — | 250 | ps | — |
| Rise time eTSEC_1588_CLK (20%–80%) | $t_{T1588CLKINR}$ | 1.0 | — | 2.0 | ns | — |
| Fall time eTSEC_1588_CLK (80%–20%) | $t_{T1588CLKINF}$ | 1.0 | — | 2.0 | ns | — |
| TSEC_1588_CLK_OUT clock period | $t_{T1588CLKOUT}$ | 2*$t_{T1588CLK}$ | — | — | ns | — |

**Table 42. eTSEC IEEE 1588 AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TSEC_1588_CLK_OUT duty cycle | $t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$ | 30 | 50 | 70 | % | — |
| TSEC_1588_PULSE_OUT | $t_{T1588OV}$ | 0.5 | — | 3.0 | ns | — |
| TSEC_1588_TRIG_IN pulse width | $t_{T1588TRIGH}$ | $2*t_{T1588CLK_MAX}$ | — | — | ns | 2 |

**Note:**

1. When TMR_CTRL[CKSEL] is set as '00', the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in Table 42, "eTSEC IEEE 1588 AC Timing Specifications." The maximum value of $t_{T1588CLK}$ is defined in terms of $T_{TX_CLK}$, that is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running at. When eTSEC1 is configured to operate in the parallel mode, the $T_{TX_CLK}$ is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for SGMII 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600, 360, 72 ns respectively. See the *MPC8572E PowerQUICC™ III Integrated Communications Processor Reference Manual* for detailed description of TMR_CTRL registers.
2. It needs to be at least two times of the clock period of the clock selected by TMR_CTRL[CKSEL].

# 9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals ECn_MDIO (management data input/output) and ECn_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)."

## 9.1 MII Management DC Electrical Characteristics

The ECn_MDC and ECn_MDIO are defined to operate at a supply voltage of 3.3 V or 2.5 V. The DC electrical characteristics for ECn_MDIO and ECn_MDC are provided in Table 43 and Table 44.

**Table 43. MII Management DC Electrical Characteristics ($LV_{DD}/TV_{DD}$=3.3 V)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage (3.3 V) | $LV_{DD}/TV_{DD}$ | 3.13 | 3.47 | V | 1, 2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.10 | $OV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ =Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 2.0 | — | V | — |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($LV_{DD}/TV_{DD}$ = Max, $V_{IN}$ [3] = 2.1 V) | $I_{IH}$ | — | 40 | μA | — |

**Table 43. MII Management DC Electrical Characteristics ($LV_{DD}/TV_{DD}$=3.3 V) (continued)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input low current ($LV_{DD}/TV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA | — |

**Note:**
1. EC1_MDC and EC1_MDIO operate on $LV_{DD}$.
2. EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on $TV_{DD}$.
3. Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbol referenced in Table 1.

**Table 44. MII Management DC Electrical Characteristics ($LV_{DD}/TV_{DD}$=2.5 V)**

| Parameters | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}/TV_{DD}$ | 2.37 | 2.63 | V | 1,2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, IOH = –1.0 mA) | $V_{OH}$ | 2.00 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND – 0.3 | 0.40 | V | — |
| Input high voltage | $V_{IH}$ | 1.70 | $LV_{DD}/TV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.70 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 10 | μA | 1, 2,3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | μA | 3 |

**Note:**

1 EC1_MDC and EC1_MDIO operate on $LV_{DD}$.
2 EC3_MDC & EC3_MDIO and EC5_MDC & EC5_MDIO operate on $TV_{DD}$.
3 Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1.

## 9.2 MII Management AC Electrical Specifications

Table 45 provides the MII management AC timing specifications.There are three sets of Ethernet management signals (EC1_MDC and EC1_MDIO, EC3_MDC and EC3_MDIO, EC5_MDC and EC5_MDIO). These are not explicitly shown in the table or in the figure following.

**Table 45. MII Management AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| ECn_MDC frequency | $f_{MDC}$ | 0.9 | 2.5 | 9.3 | MHz | 2, 3 |
| ECn_MDC period | $t_{MDC}$ | 107.5 | — | 1120 | ns | — |
| ECn_MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| ECn_MDC to ECn_MDIO delay | $t_{MDKHDX}$ | 10 | — | $16*t_{plb_clk}$ | ns | 5 |
| ECn_MDIO to ECn_MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |

**Table 45. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| ECn_MDIO to ECn_MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| ECn_MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | 4 |
| ECn_MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | 4 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency ($f_{CCB}$). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of MPC8572E's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC} = 533/(2*4*8) = 533/64 = 8.3$ MHz. That is, for a system running at a particular platform frequency ($f_{CCB}$), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. Refer to MPC8572E reference manual's MIIMCFG register section for more detail.
3. The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for MPC8572E (600 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for MPC8572E (400 MHz) divided by 448, following the formula described in Note 2 above. The typical ECn_MDC output clock frequency of 2.5 MHz is shown for reference purpose per IEEE 802.3 specification.
4. Guaranteed by design.
5. $t_{plb_clk}$ is the platform (CCB) clock.

Figure 28 shows the MII management AC timing diagram.

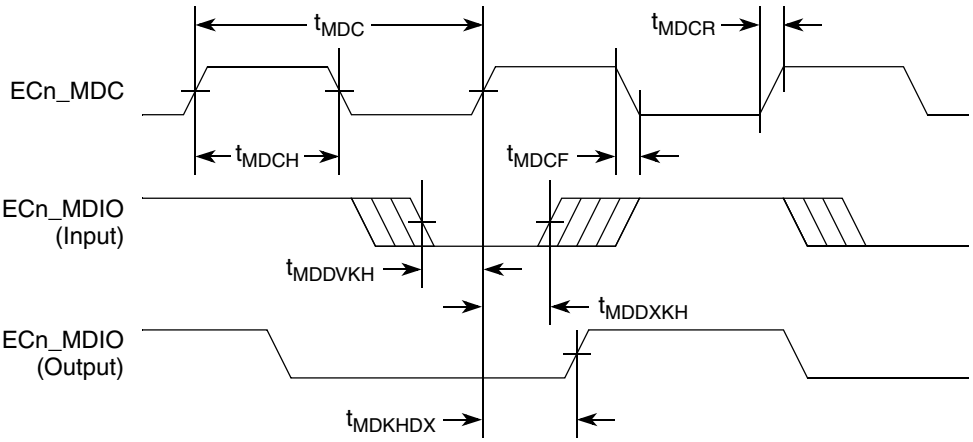



**Figure 28. MII Management Interface Timing Diagram**

# 10 Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8572E.

## 10.1 Local Bus DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 3.3 V DC.

**Table 46. Local Bus DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 3.3V | $BV_{DD}$ | 3.13 | 3.47 | V |
| High-level input voltage | $V_{IH}$ | 2 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. Note that the symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

Table 47 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 2.5 V DC.

**Table 47. Local Bus DC Electrical Characteristics (2.5 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 2.5V | $BV_{DD}$ | 2.37 | 2.63 | V |
| High-level input voltage | $V_{IH}$ | 1.70 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.7 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IH}$ | — | 10 | μA |
| | $I_{IL}$ | | –15 | |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –1 mA) | $V_{OH}$ | 2.0 | $BV_{DD}$ + 0.3 | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 1 mA) | $V_{OL}$ | GND – 0.3 | 0.4 | V |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

Table 48 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD}$ = 1.8 V DC.

**Table 48. Local Bus DC Electrical Characteristics (1.8 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 1.8V | $BV_{DD}$ | 1.71 | 1.89 | V |
| High-level input voltage | $V_{IH}$ | 0.65 x $BV_{DD}$ | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.35 x $BV_{DD}$ | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | TBD | TBD | μA |
| High-level output voltage ($I_{OH}$ = –100 μA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| High-level output voltage ($I_{OH}$ = –2 mA) | $V_{OH}$ | $BV_{DD}$ – 0.45 | — | V |
| Low-level output voltage ($I_{OL}$ = 100 μA) | $V_{OL}$ | — | 0.2 | V |
| Low-level output voltage ($I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.45 | V |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

## 10.2 Local Bus AC Electrical Specifications

Table 49 describes the general timing parameters of the local bus interface at $BV_{DD}$ = 3.3 V DC.

**Table 49. Local Bus General Timing Parameters ($BV_{DD}$ = 3.3 V DC)—PLL Enabled**

At recommended operating conditions with $BV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 6.67 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7,8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 1.8 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.7 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output negation to high impedance for LAD/LDP (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.3 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.4 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.3 | ns | 3 |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 2.3 | ns | 3 |

**Table 49. Local Bus General Timing Parameters ($BV_{DD}$ = 3.3 V DC)—PLL Enabled (continued)**

At recommended operating conditions with $BV_{DD}$ of 3.3 V ± 5%. (continued)

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.7 | — | ns | 3 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.7 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.5 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.5 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 50 describes the general timing parameters of the local bus interface at $BV_{DD}$ = 2.5 V DC.

**Table 50. Local Bus General Timing Parameters ($BV_{DD}$ = 2.5 V DC)—PLL Enabled**

At recommended operating conditions with $BV_{DD}$ of 2.5 V ± 5%

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 6.67 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7, 8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 1.9 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.8 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output negation to high impedance for LAD/LDP (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.4 | ns | — |

**Table 50. Local Bus General Timing Parameters ($BV_{DD}$ = 2.5 V DC)—PLL Enabled (continued)**

At recommended operating conditions with $BV_{DD}$ of 2.5 V ± 5% (continued)

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.5 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.4 | ns | 3 |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 2.4 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.8 | — | ns | 3 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.8 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 51 describes the general timing parameters of the local bus interface at $BV_{DD}$ = 1.8 V DC

**Table 51. Local Bus General Timing Parameters ($BV_{DD}$ = 1.8 V DC)—PLL Enabled**

At recommended operating conditions with $BV_{DD}$ of 1.8 V ± 5%

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 6.67 | 12 | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7, 8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 2.4 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.9 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.1 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.1 | — | ns | 3, 4 |
| LALE output negation to high impedance for LAD/LDP (LATCH hold time) | $t_{LBOTOT}$ | 1.2 | — | ns | 6 |

**Table 51. Local Bus General Timing Parameters ($BV_{DD}$ = 1.8 V DC)—PLL Enabled (continued)**

At recommended operating conditions with $BV_{DD}$ of 1.8 V ± 5% (continued)

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 3.2 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 3.2 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 3.2 | ns | 3 |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 3.2 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.9 | — | ns | 3 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.9 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.6 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.6 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 29 provides the AC test load for the local bus.

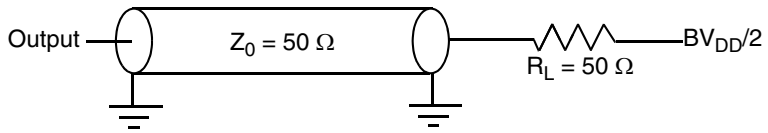



**Figure 29. Local Bus AC Test Load**

Figure 30 through Figure 35 show the local bus signals.

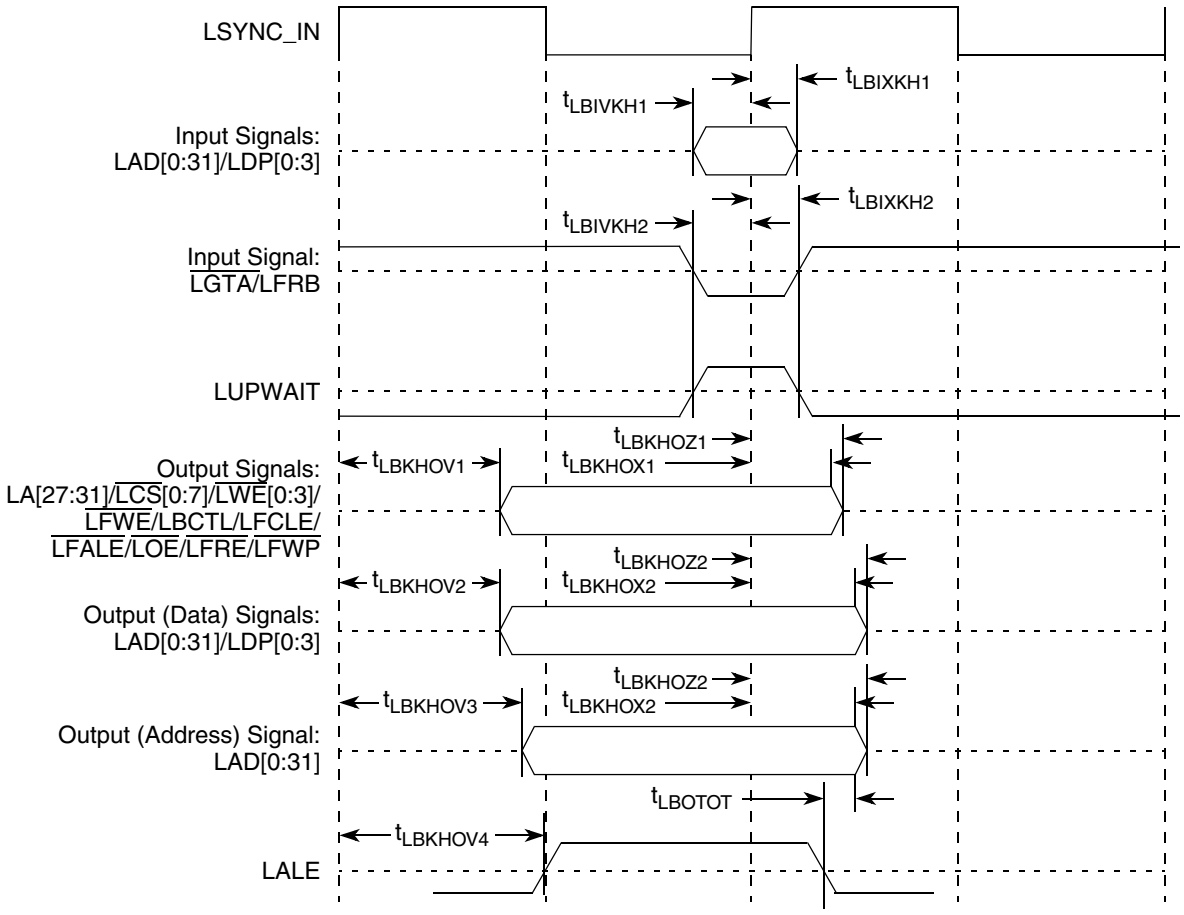



**Figure 30. Local Bus Signals, Non-Special Signals Only (PLL Enabled)**

Table 52 describes the general timing parameters of the local bus interface at $BV_{DD}$ = 3.3 V DC with PLL disabled.

**Table 52. Local Bus General Timing Parameters—PLL Bypassed**

At recommended operating conditions with $BV_{DD}$ of 3.3 V ± 5%

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 12 | — | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 43 | 57 | % | — |
| Internal launch/capture clock to LCLK delay | $t_{LBKHKT}$ | 2.3 | 4.0 | ns | — |
| Input setup to local bus clock (except LGTA/LUPWAIT) | $t_{LBIVKH1}$ | 5.8 | — | ns | 4, 5 |
| LGTA/LUPWAIT input setup to local bus clock | $t_{LBIVKL2}$ | 5.7 | — | ns | 4, 5 |
| Input hold from local bus clock (except LGTA/LUPWAIT) | $t_{LBIXKH1}$ | -1.3 | — | ns | 4, 5 |
| LGTA/LUPWAIT input hold from local bus clock | $t_{LBIXKL2}$ | -1.3 | — | ns | 4, 5 |

**Table 52. Local Bus General Timing Parameters—PLL Bypassed (continued)**

At recommended operating conditions with $BV_{DD}$ of 3.3 V ± 5%

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| LALE output negation to high impedance for LAD/LDP (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKLOV1}$ | — | –0.3 | ns | |
| Local bus clock to data valid for LAD/LDP | $t_{LBKLOV2}$ | — | –0.1 | ns | 4 |
| Local bus clock to address valid for LAD | $t_{LBKLOV3}$ | — | 0.0 | ns | 4 |
| Local bus clock to LALE assertion | $t_{LBKLOV4}$ | — | 0.0 | ns | 4 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKLOX1}$ | –3.3 | — | ns | 4 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKLOX2}$ | –3.3 | — | ns | 4 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKLOZ1}$ | — | 0.2 | ns | 7 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ2}$ | — | 0.2 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by $t_{LBKHKT}$.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

## NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of $t_{LBKHKT}$. In this mode, signals are launched at the rising edge of the internal clock and are captured at the falling edge of the internal clock with the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

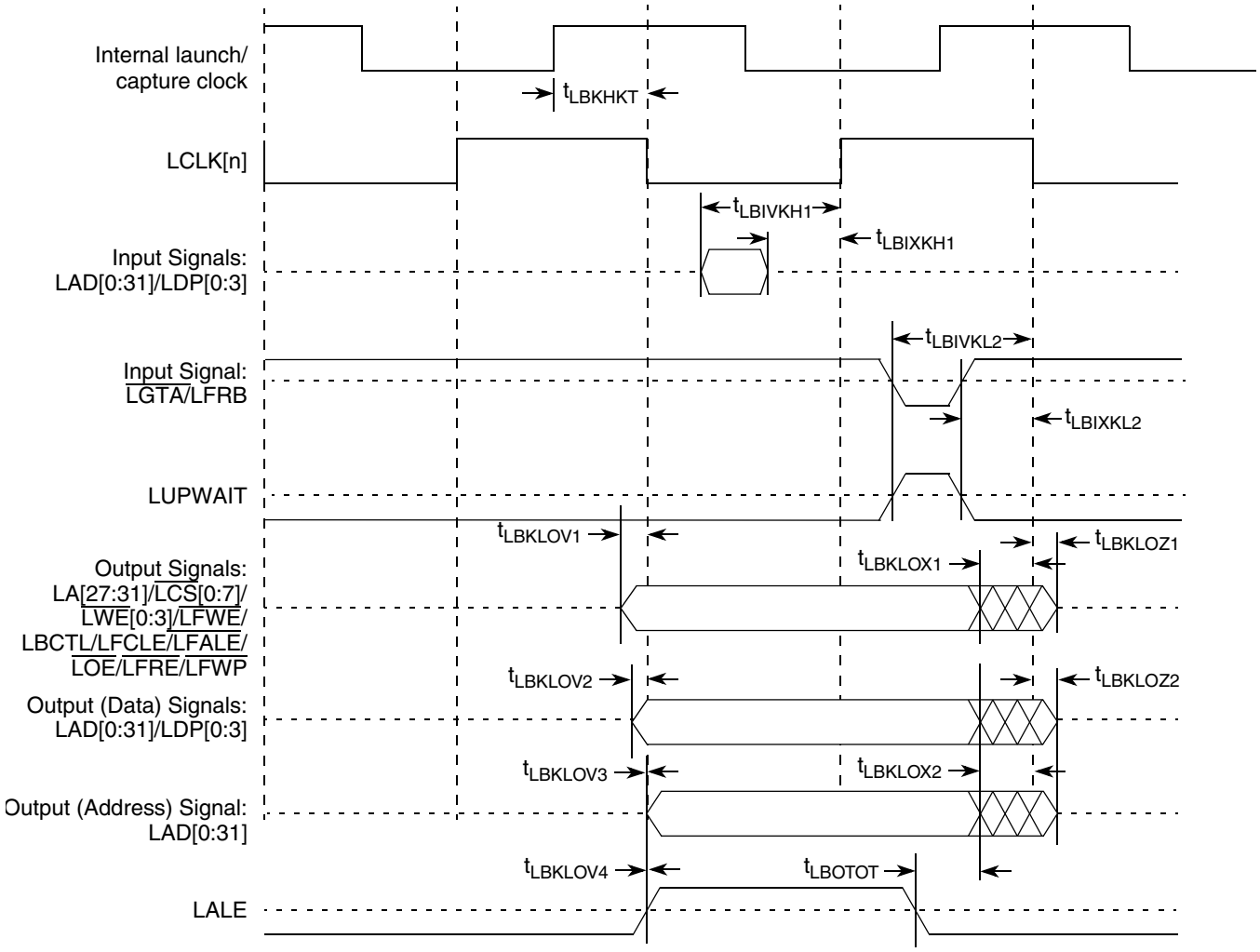



**Figure 31. Local Bus Signals (PLL Bypass Mode)**

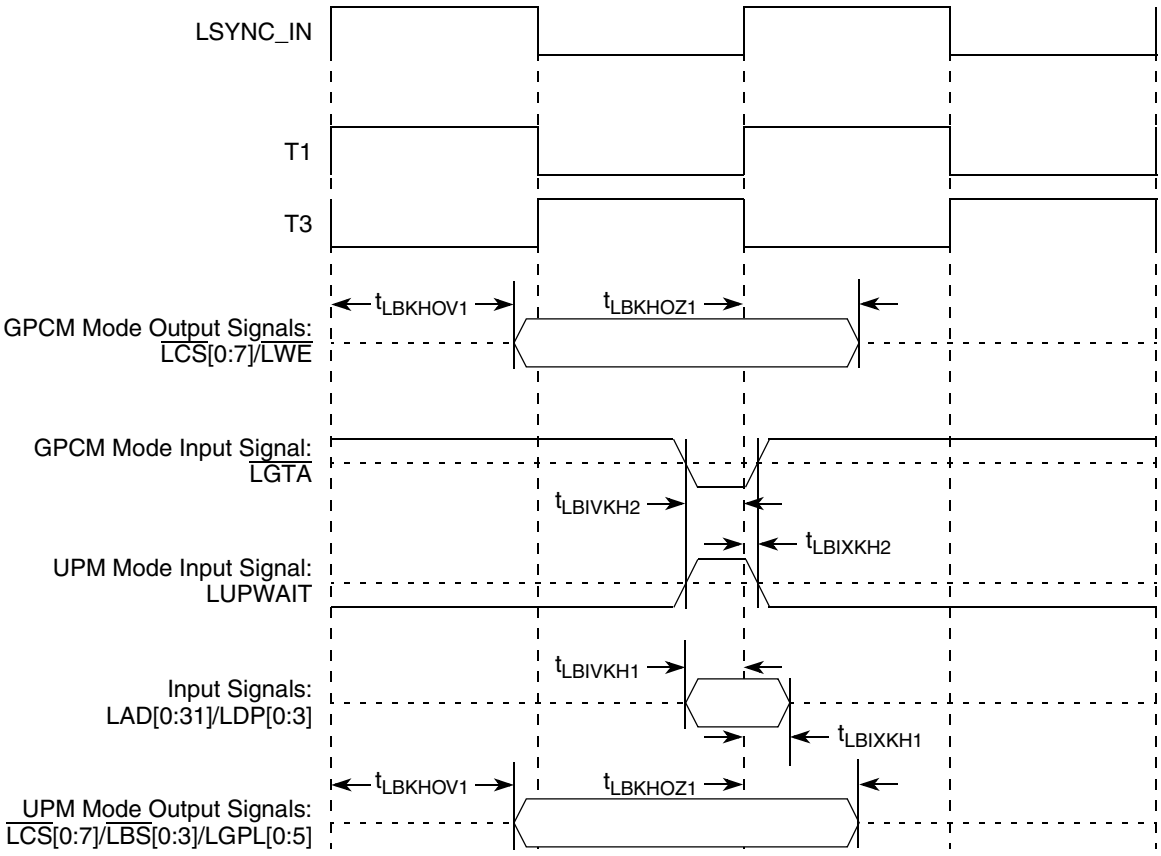



**Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)**

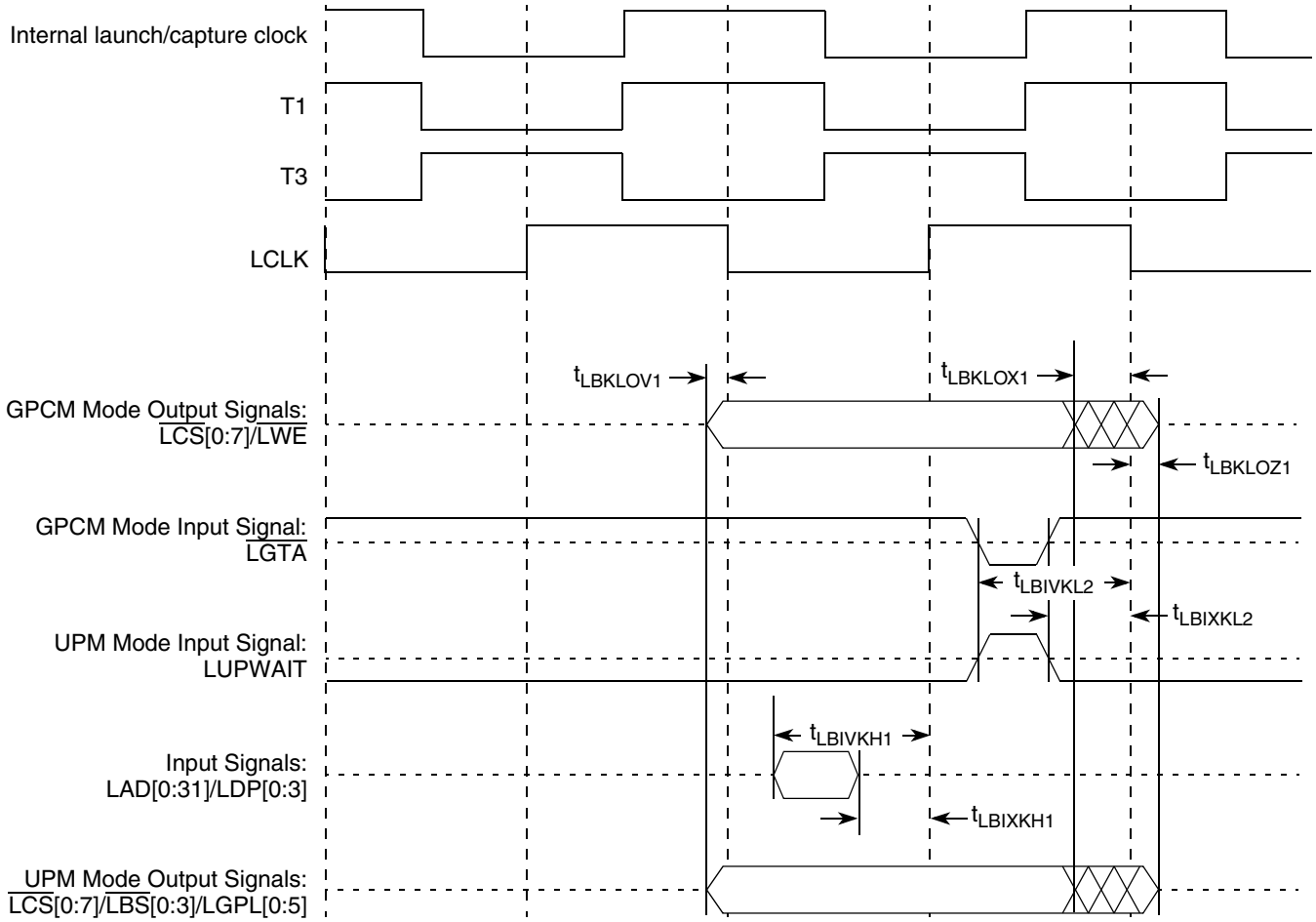



**Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)**

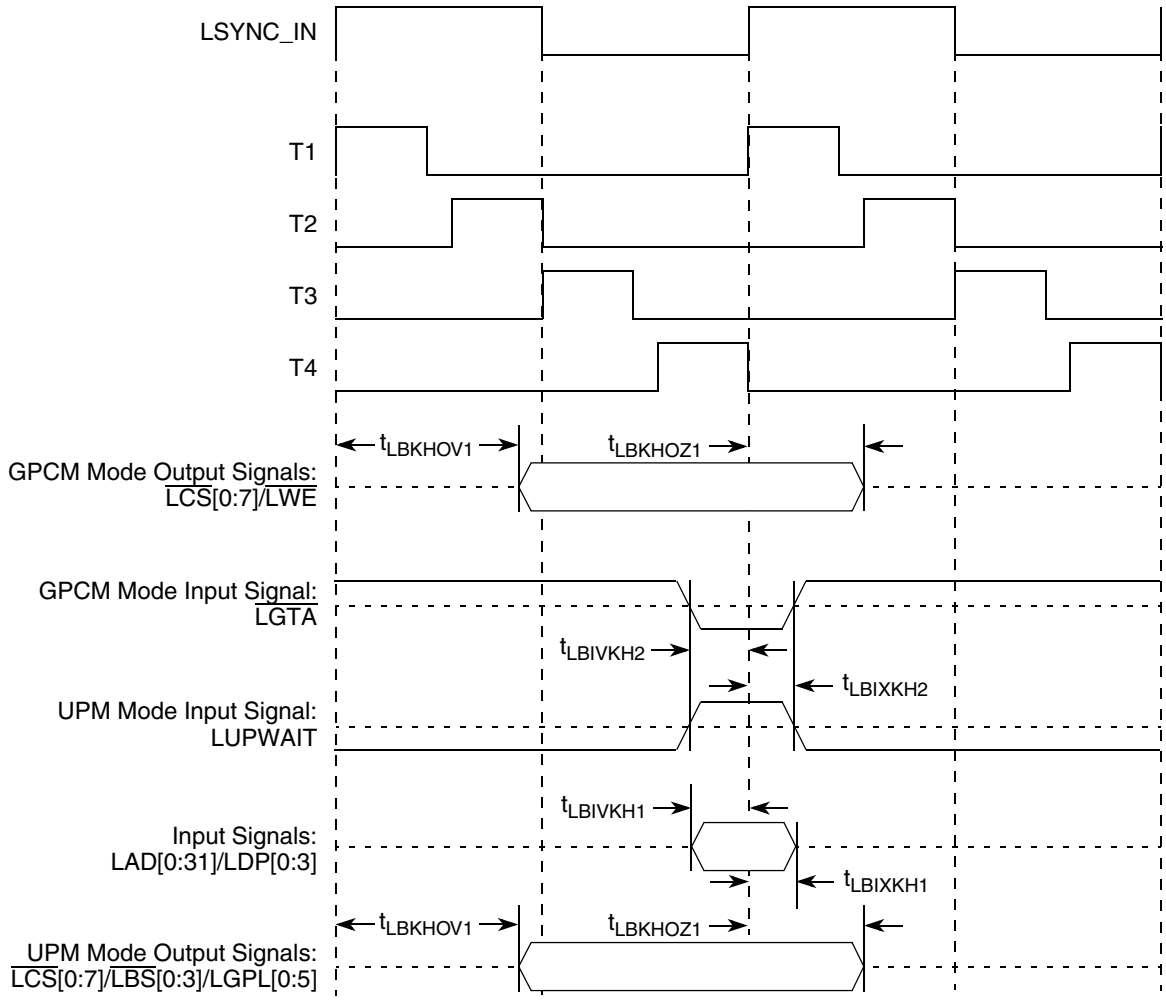



**Figure 34. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)**

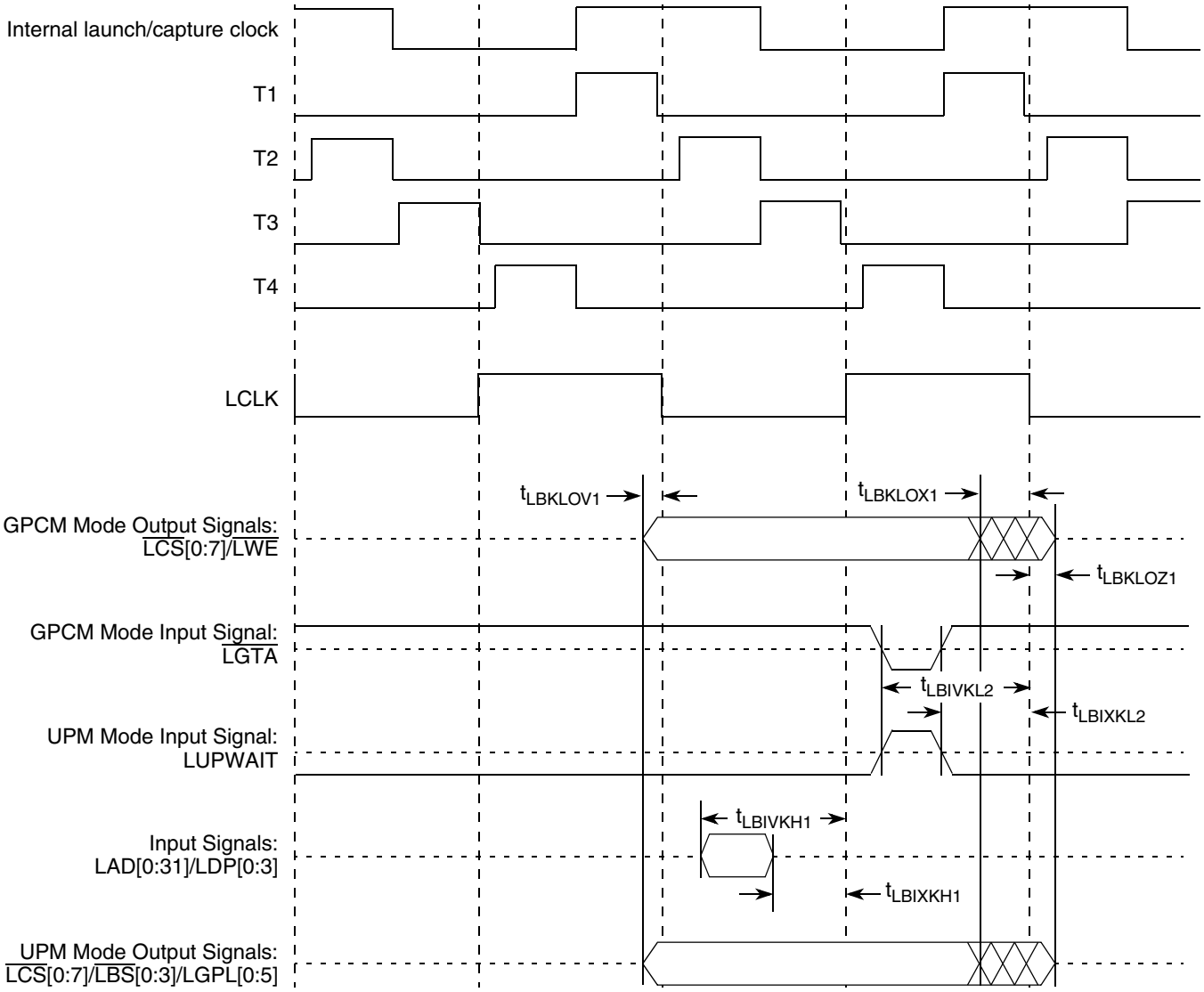



**Figure 35. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)**

# 11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain asserted for at least 3 system clocks (SYSCLK periods).

# 12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8572E.

Table 53 provides the JTAG AC timing specifications as defined in Figure 37 through Figure 39.

**Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) [1]**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | 6 |
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>0 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>20<br>25 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>4<br>4 | <br>20<br>25 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>30<br>30 | <br>—<br>— | ns | 5 |

**Table 53. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>3<br>3 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 36). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design.

Figure 36 provides the AC test load for TDO and the boundary-scan outputs.

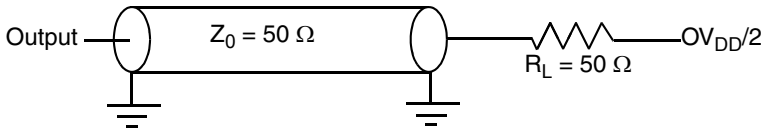



**Figure 36. AC Test Load for the JTAG Interface**

Figure 37 provides the JTAG clock input timing diagram.

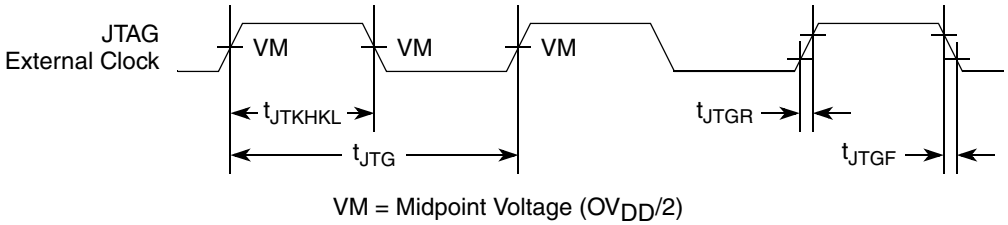



**Figure 37. JTAG Clock Input Timing Diagram**

Figure 38 provides the $\overline{\text{TRST}}$ timing diagram.

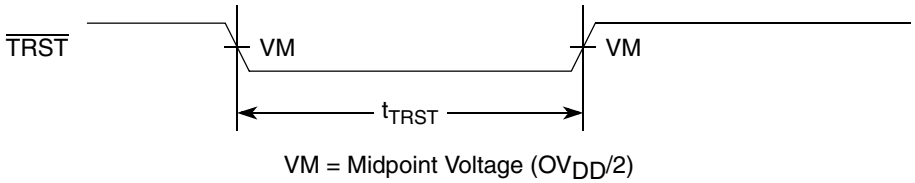



**Figure 38. $\overline{\text{TRST}}$ Timing Diagram**

Figure 39 provides the boundary-scan timing diagram.

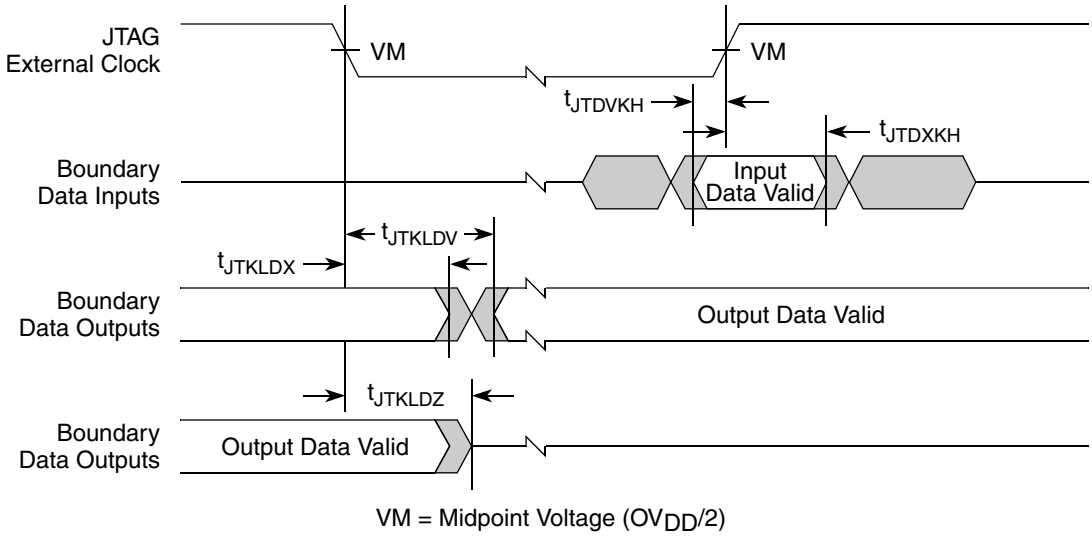



**Figure 39. Boundary-Scan Timing Diagram**

# 13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8572E.

## 13.1 I²C DC Electrical Characteristics

Table 54 provides the DC electrical characteristics for the I²C interfaces.

**Table 54. I²C DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD} + 0.3$ | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | 0.4 | V | 1 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 2 |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max) | $I_I$ | –10 | 10 | μA | 3 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

## 13.2 I²C AC Electrical Specifications

Table 55 provides the AC timing parameters for the I²C interfaces.

**Table 55. I²C AC Electrical Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%. All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 2).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz[4] |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns |
| Data input hold time:<br>CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | <br>—<br>0[2] | <br>—<br>— | μs |
| Data output delay time | $t_{I2OVKL}$ | — | 0.9[3] | μs |
| Setup time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | μs |
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | μs |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times OV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times OV_{DD}$ | — | V |
| Capacitive load for each bus line | Cb | — | 400 | pF |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time.
2. As a transmitter, the MPC8572E provides a delay time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP condition. When the MPC8572E acts as the I2C bus master while transmitting, the MPC8572E drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8572E would not cause unintended generation of START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8572E as transmitter, application note AN2919 referred to in note 4 below is recommended.
3. The maximum $t_{I2OVKL}$ has only to be met if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL*.

Figure 40 provides the AC test load for the $I^2C$.

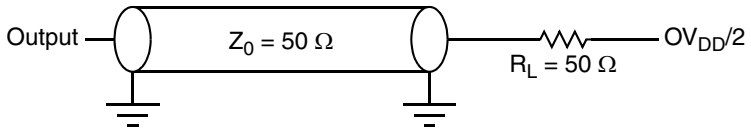



**Figure 40. $I^2C$ AC Test Load**

Figure 41 shows the AC timing diagram for the $I^2C$ bus.

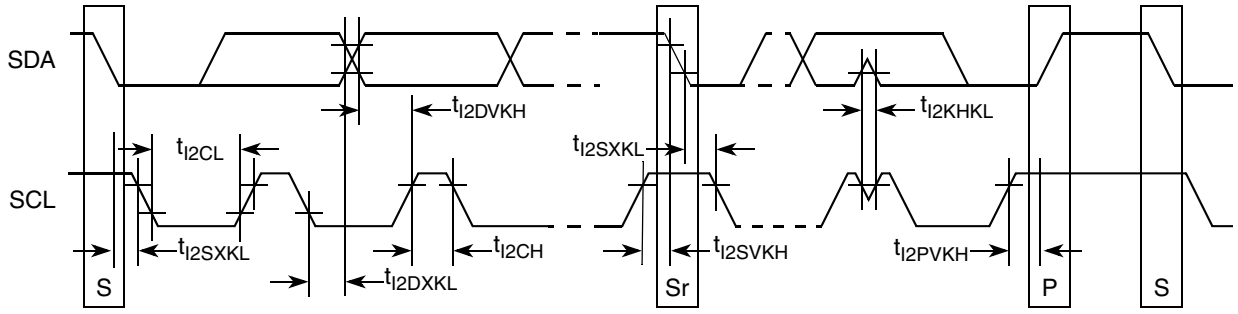



**Figure 41. $I^2C$ Bus AC Timing Diagram**

# 14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8572E.

## 14.1 GPIO DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD}$ = 3.3 V DC.

**Table 56. GPIO DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 3.3V | $BV_{DD}$ | 3.13 | 3.47 | V |
| High-level input voltage | $V_{IH}$ | 2 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. Note that the symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

Table 57 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD}$ = 2.5 V DC.

**Table 57. GPIO DC Electrical Characteristics (2.5 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 2.5V | $BV_{DD}$ | 2.37 | 2.63 | V |
| High-level input voltage | $V_{IH}$ | 1.70 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.7 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IH}$ | — | 10 | μA |
| | $I_{IL}$ | | –15 | |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –1 mA) | $V_{OH}$ | 2.0 | $BV_{DD}$ + 0.3 | V |
| Low-level output voltage ($BV_{DD}$ min, $I_{OL}$ = 1 mA) | $V_{OL}$ | GND – 0.3 | 0.4 | V |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

Table 58 provides the DC electrical characteristics for the GPIO interface operating at $BV_{DD}$ = 1.8 V DC.

**Table 58. GPIO DC Electrical Characteristics (1.8 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 1.8V | $BV_{DD}$ | 1.71 | 1.89 | V |
| High-level input voltage | $V_{IH}$ | 0.65 x $BV_{DD}$ | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.35 x $BV_{DD}$ | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | TBD | TBD | μA |
| High-level output voltage ($I_{OH}$ = –100 μA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| High-level output voltage ($I_{OH}$ = –2 mA) | $V_{OH}$ | $BV_{DD}$ – 0.45 | — | V |
| Low-level output voltage ($I_{OL}$ = 100 μA) | $V_{OL}$ | — | 0.2 | V |
| Low-level output voltage ($I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.45 | V |

**Note:**
1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

## 14.2 GPIO AC Electrical Specifications

Table 59 provides the GPIO input and output AC timing specifications.

**Table 59. GPIO Input AC Timing Specifications[1]**

| Parameter | Symbol | Typ | Unit | Notes |
|---|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns | 2 |

**Notes:**
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYSCLK. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation.

Figure 42 provides the AC test load for the GPIO.

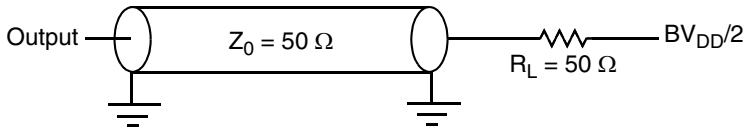



**Figure 42. GPIO AC Test Load**

# 15 High-Speed Serial Interfaces (HSSI)

The MPC8572E features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface can be used for PCI Express and/or Serial RapidIO data transfers. The SerDes2 is dedicated for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

## 15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{\text{SDn_TX}}$) or a receiver input (SDn_RX and $\overline{\text{SDn_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SDn_TX, $\overline{\text{SDn_TX}}$, SDn_RX and $\overline{\text{SDn_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, $V_{OD}$** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The $V_{OD}$ value can be either positive or negative.

3. **Differential Input Voltage, $V_{ID}$** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The $V_{ID}$ value can be either positive or negative.

4. **Differential Peak Voltage, $V_{DIFFp}$**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

**6. Differential Waveform**

1. The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn_TX}$, for example) from the non-inverting signal (SDn_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 52 as an example for differential waveform.

2. Common Mode Voltage, $V_{cm}$

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{\overline{SDn_TX}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

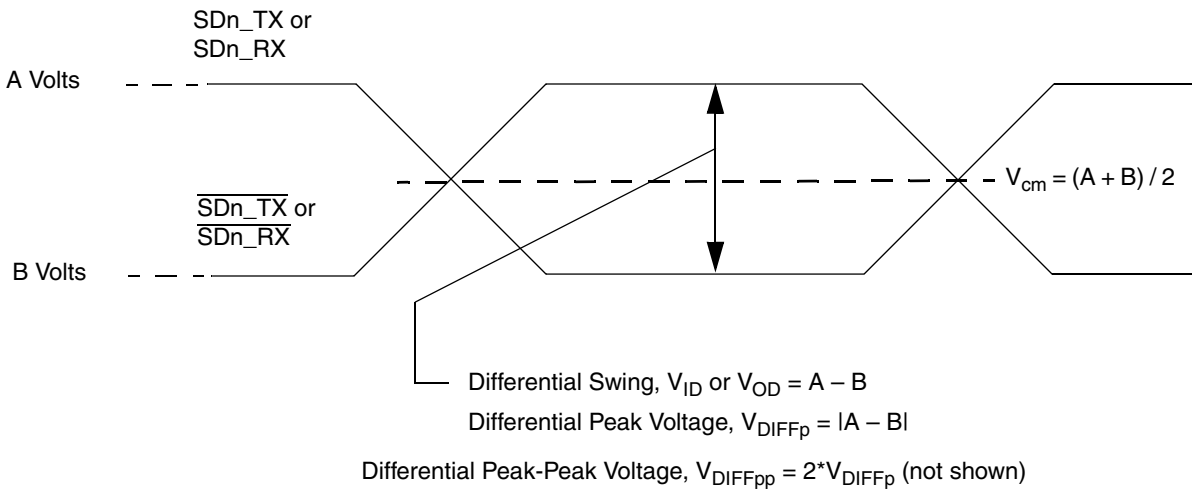



**Figure 43. Differential Voltage Definitions for Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing ($V_{OD}$) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, $V_{OD}$ is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ($V_{DIFFp}$) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

## 15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$ for PCI Express and Serial RapidIO, or SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ for the SGMII interface respectively.

The following sections describe the SerDes reference clock requirements and some application information.

### 15.2.1 SerDes Reference Clock Receiver Characteristics

Figure 44 shows a receiver reference diagram of the SerDes reference clocks. Characteristics are as follows:

- The supply voltage requirements for $XV_{DD_SRDS2}$ are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 44. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{_REF_CLK}}$) has on-chip 50-Ω termination to SGND_SRDSn (xcorevss) followed by on-chip AC-coupling.

— The external reference clock driver must be able to drive this termination.
— The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), because the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

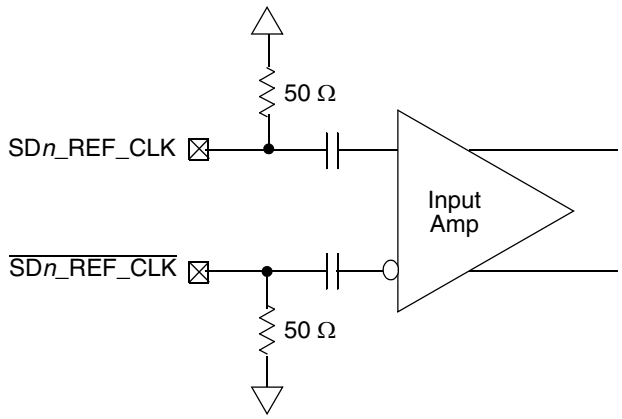



**Figure 44. Receiver of SerDes Reference Clocks**

## 15.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8572E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire

of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 15.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 45 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 46 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**

— The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD}n\text{_REF_CLK}}$ either left unconnected or tied to ground.

— The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 47 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{_REF_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

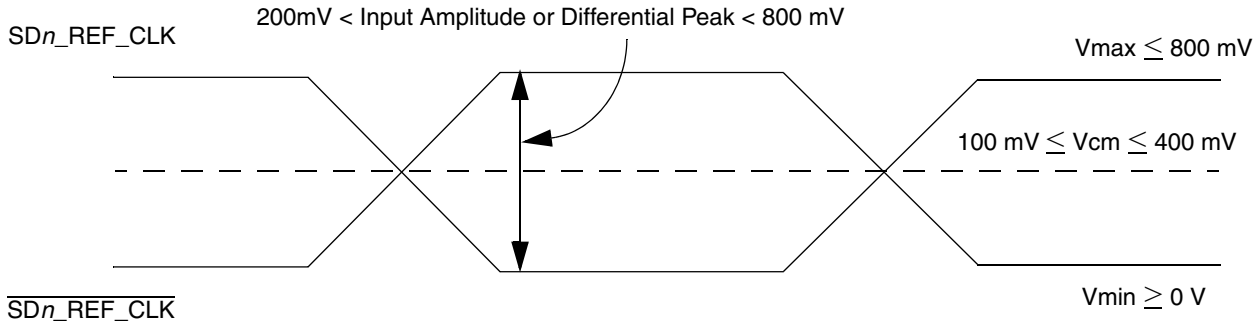



**Figure 45. Differential Reference Clock Input DC Requirements (External DC-Coupled)**

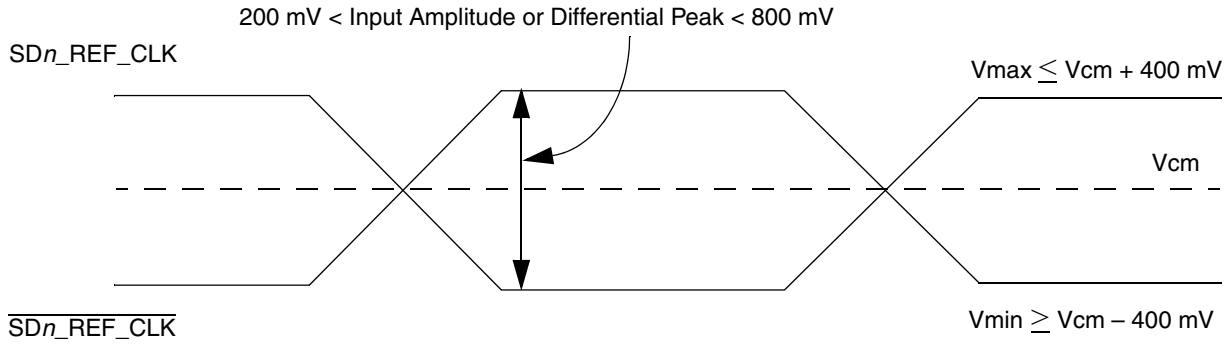



**Figure 46. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

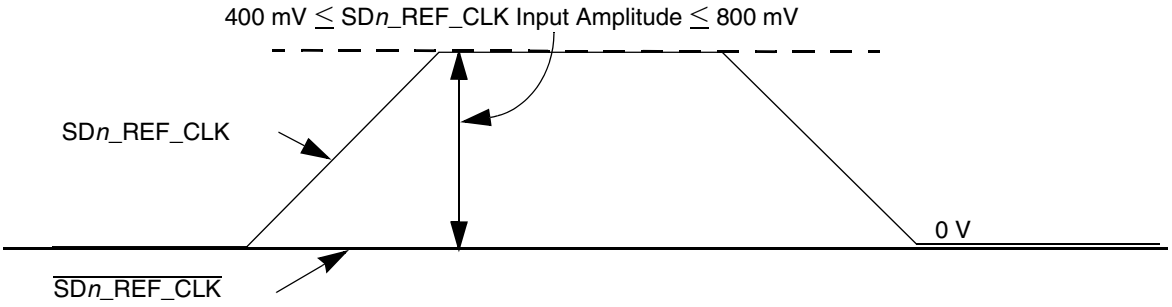



**Figure 47. Single-Ended Reference Clock Input DC Requirements**

### 15.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, additionally to AC-coupling.

**NOTE**

Figure 48 to Figure 51 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8572E SerDes reference clock receiver requirement provided in this document.

Figure 48 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8572E SerDes reference clock input's DC requirement.

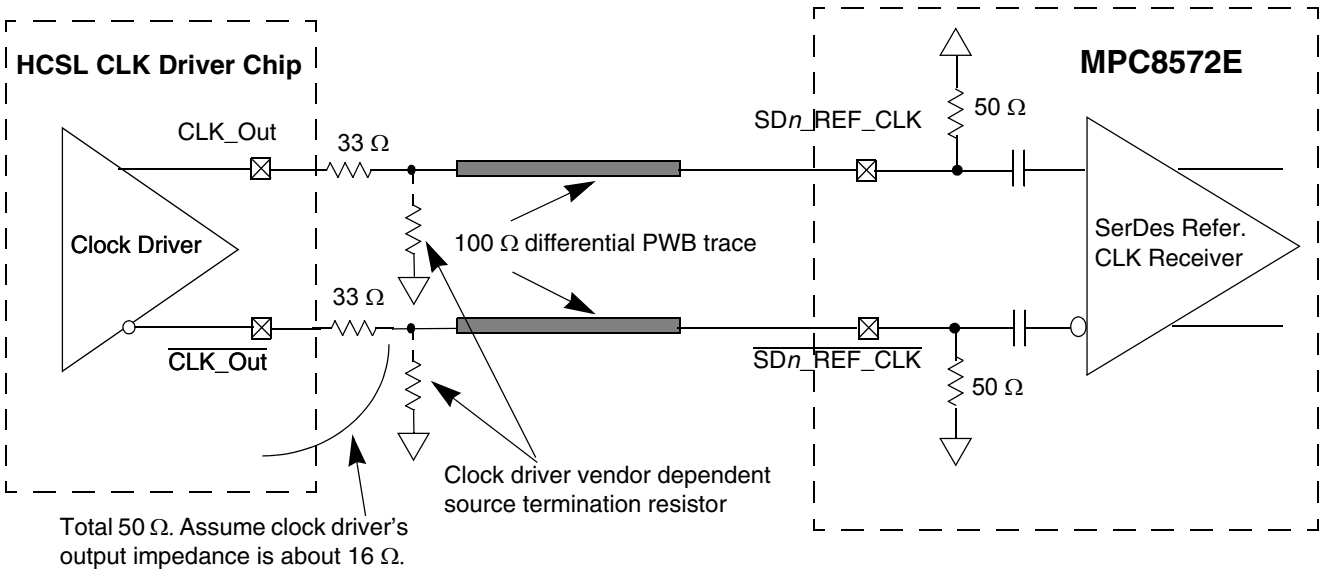



**Figure 48. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)**

Figure 49 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Because LVDS clock driver's common mode voltage is higher than the MPC8572E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

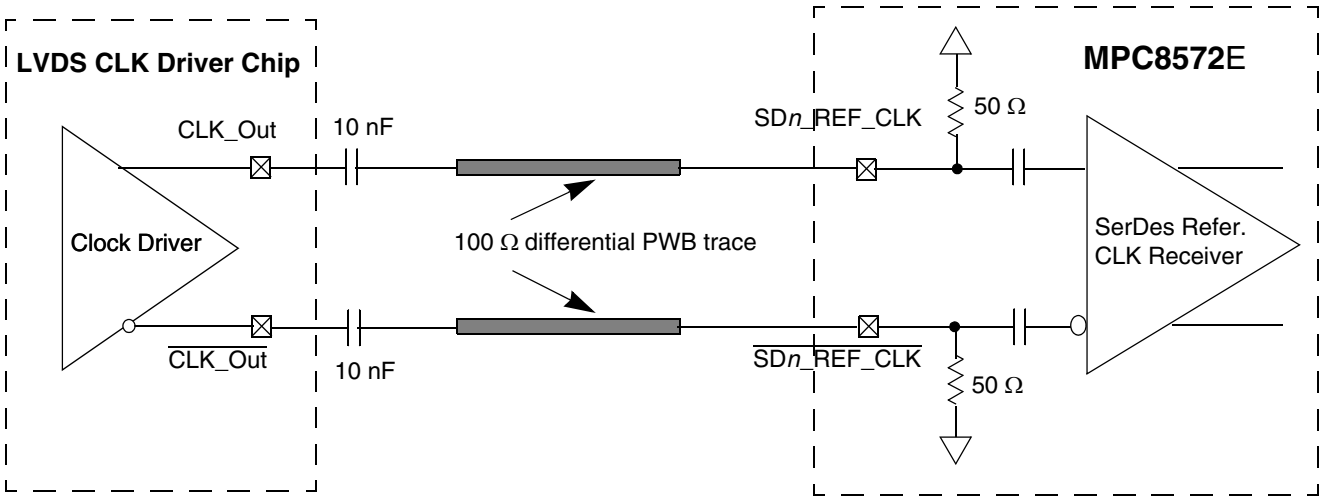



**Figure 49. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)**

Figure 50 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Because LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8572E SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 50 assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8572E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Consult

clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

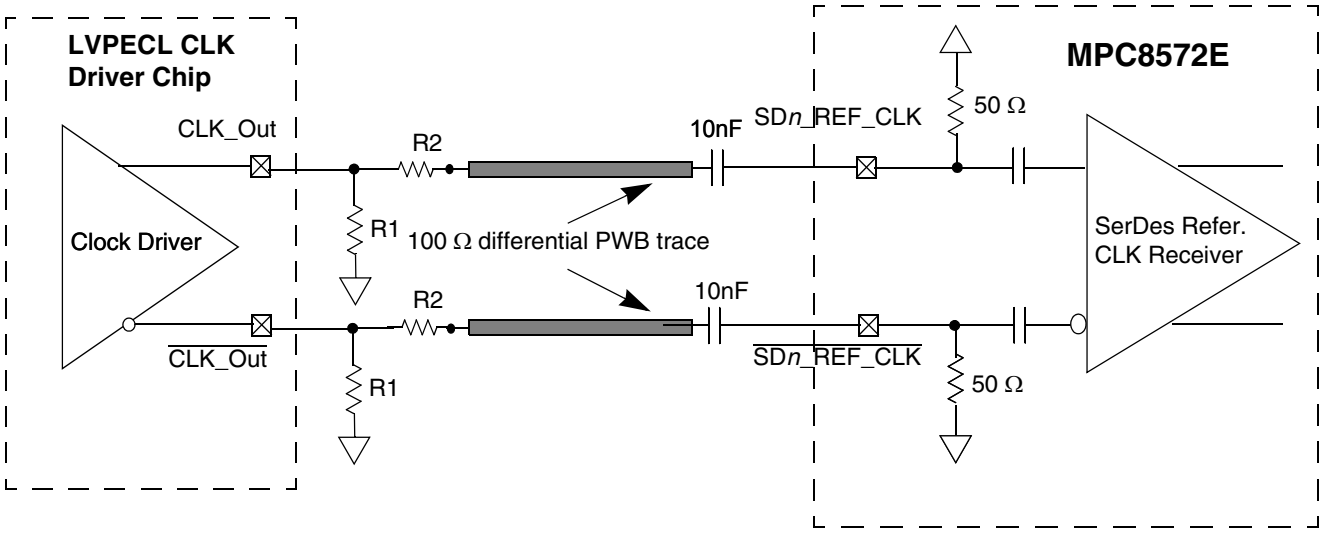



**Figure 50. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

Figure 51 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8572E SerDes reference clock input's DC requirement.

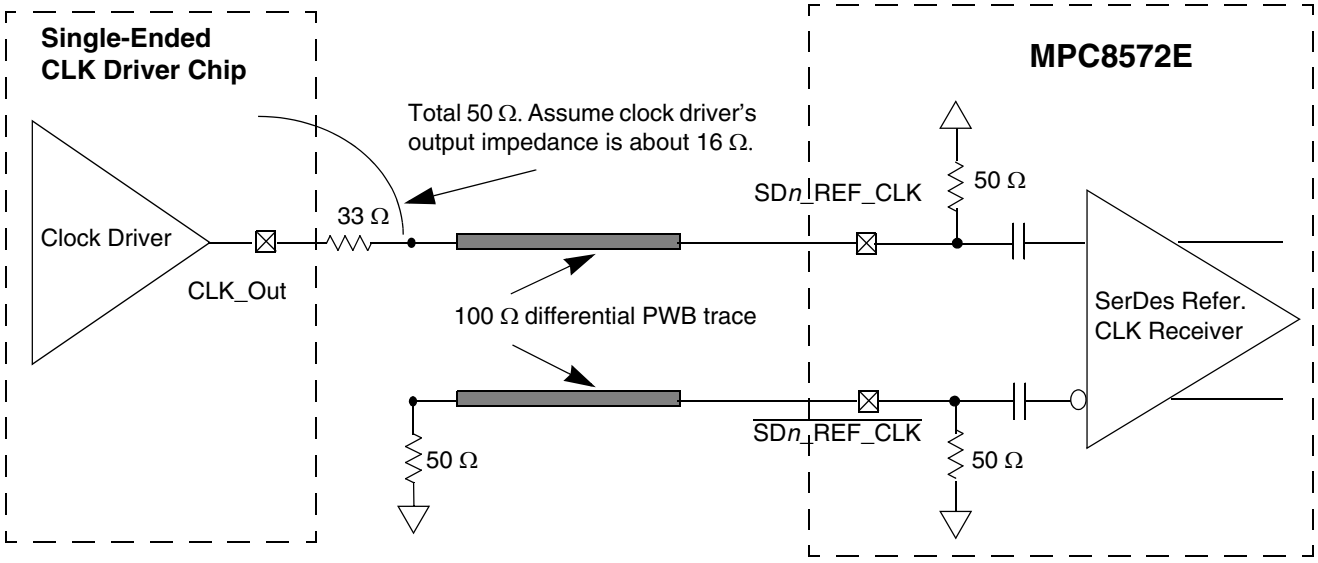



**Figure 51. Single-Ended Connection (Reference Only)**

## 15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise

occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 ohms to match the transmission line and reduce reflections which are a source of noise to the system.

Table 60 describes some AC parameters common to SGMII, PCI Express and Serial RapidIO protocols.

**Table 60. SerDes Reference Clock Common AC Parameters**

At recommended operating conditions with $XV_{DD_SRDS1}$ or $XV_{DD_SRDS2}$ = 1.1V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Rising Edge Rate | Rise Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling Edge Rate | Fall Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential Input High Voltage | $V_{IH}$ | +200 | | mV | 2 |
| Differential Input Low Voltage | $V_{IL}$ | — | -200 | mV | 2 |
| Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn_REF_CLK}}$) matching | Rise-Fall Matching | — | 20 | % | 1, 4 |

**Notes:**

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn_REF_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 52.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn_REF_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn_REF_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn_REF_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 53.

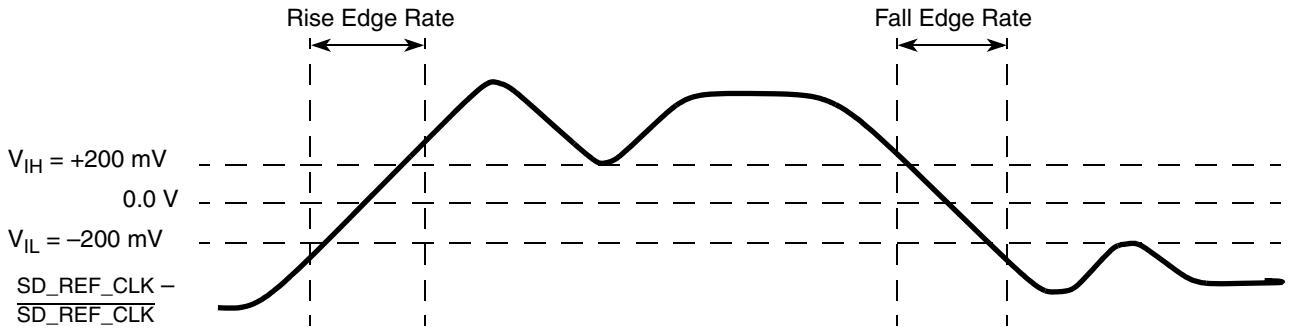



**Figure 52. Differential Measurement Points for Rise and Fall Time**

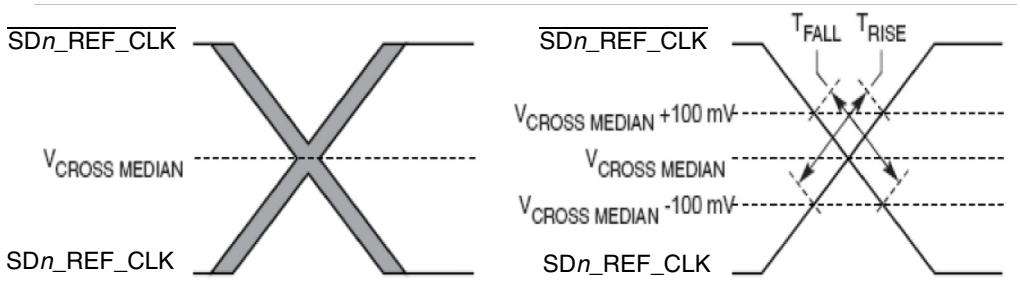



**Figure 53. Single-Ended Measurement Points for Rise and Fall Time Matching**

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 8.3.2, "AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$"
- Section 16.2, "AC Requirements for PCI Express SerDes Reference Clocks"
- Section 17.2, "AC Requirements for Serial RapidIO SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$"

#### 15.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1_REF_CLK}}$ are designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2_REF_CLK}}$ are not to be used with, and should not be clocked by, a spread spectrum clock source.

## 15.3 SerDes Transmitter and Receiver Reference Circuits

Figure 54 shows the reference circuits for SerDes data lane's transmitter and receiver.

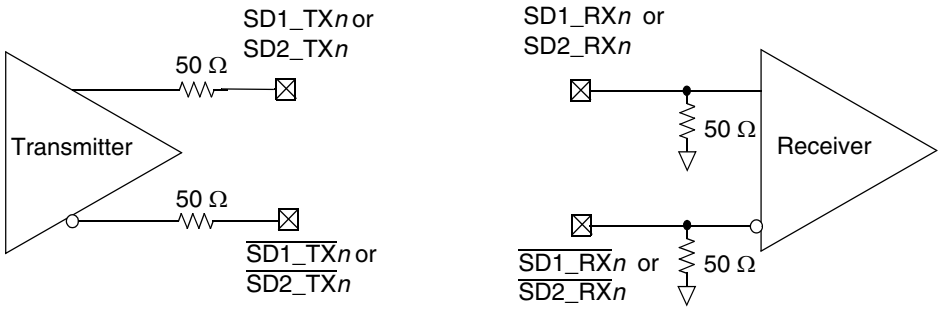



**Figure 54. SerDes Transmitter and Receiver Reference Circuits**

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"
- Section 16, "PCI Express"
- Section 17, "Serial RapidIO"

Note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

# 16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8572E.

## 16.1 DC Requirements for PCI Express SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, "SerDes Reference Clocks."

## 16.2 AC Requirements for PCI Express SerDes Reference Clocks

Table 61 lists AC requirements.

**Table 61. SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10 | — | ns | 1 |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –50 | — | 50 | ps | — |

**Notes:**
1. Typical cycle time is based on PCI Express Card Electromechanical Specification Revision 1.0a.

## 16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

## 16.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, Use the PCI Express Base Specification. REV. 1.0a document.

### 16.4.1 Differential Transmitter (TX) Output

Table 62 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

**Table 62. Differential Transmitter (TX) Output Specifications**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $V_{TX-DIFFp-p}$ | Differential Peak-to-Peak Output Voltage | 0.8 | — | 1.2 | V | $V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 2. |

**Table 62. Differential Transmitter (TX) Output Specifications (continued)**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $V_{TX-DE-RATIO}$ | De- Emphasized Differential Output Voltage (Ratio) | –3.0 | –3.5 | -4.0 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2. |
| $T_{TX-EYE}$ | Minimum TX Eye Width | 0.70 | — | — | UI | The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - $T_{TX-EYE}$= 0.3 UI. See Notes 2 and 3. |
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.15 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3. |
| $T_{TX-RISE}$, $T_{TX-FALL}$ | D+/D- TX Output Rise/Fall Time | 0.125 | — | — | UI | See Notes 2 and 5 |
| $V_{TX-CM-ACp}$ | RMS AC Peak Common Mode Output Voltage | — | — | 20 | mV | $V_{TX-CM-ACp}$ = RMS(\|$V_{TXD+}$ + $V_{TXD-}$\|/2 - $V_{TX-CM-DC}$)<br>$V_{TX-CM-DC}$ = $DC_{(avg)}$ of \|$V_{TX-D+}$ + $V_{TX-D-}$\|/2<br>See Note 2 |
| $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle | 0 | — | 100 | mV | \|$V_{TX-CM-DC\ (during\ L0)}$ - $V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}$\|<=100 mV<br>$V_{TX-CM-DC}$ = $DC_{(avg)}$ of \|$V_{TX-D+}$ + $V_{TX-D-}$\|/2 [L0]<br>$V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of \|$V_{TX-D+}$ + $V_{TX-D-}$\|/2 [Electrical Idle]<br>See Note 2. |
| $V_{TX-CM-DC-LINE-DELTA}$ | Absolute Delta of DC Common Mode between D+ and D– | 0 | — | 25 | mV | \|$V_{TX-CM-DC-D+}$ - $V_{TX-CM-DC-D-}$\| <= 25 mV<br>$V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of \|$V_{TX-D+}$\|<br>$V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of \|$V_{TX-D-}$\|<br>See Note 2. |
| $V_{TX-IDLE-DIFFp}$ | Electrical Idle differential Peak Output Voltage | 0 | — | 20 | mV | $V_{TX-IDLE-DIFFp}$ = \|$V_{TX-IDLE-D+}$ -$V_{TX-IDLE-D-}$\| <= 20 mV<br>See Note 2. |
| $V_{TX-RCV-DETECT}$ | The amount of voltage change allowed during Receiver Detection | | — | 600 | mV | The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6. |
| $V_{TX-DC-CM}$ | The TX DC Common Mode Voltage | 0 | — | 3.6 | V | The allowed DC Common Mode voltage under any conditions. See Note 6. |
| $I_{TX-SHORT}$ | TX Short Circuit Current Limit | | — | 90 | mA | The total current the Transmitter can provide when shorted to its ground |
| $T_{TX-IDLE-MIN}$ | Minimum time spent in Electrical Idle | 50 | — | — | UI | Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set |

**Table 62. Differential Transmitter (TX) Output Specifications (continued)**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$ | Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set | — | — | 20 | UI | After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0. |
| $T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$ | Maximum time to transition to valid TX specifications after leaving an Electrical idle condition | — | — | 20 | UI | Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle |
| $RL_{TX\text{-}DIFF}$ | Differential Return Loss | 12 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4 |
| $RL_{TX\text{-}CM}$ | Common Mode Return Loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4 |
| $Z_{TX\text{-}DIFF\text{-}DC}$ | DC Differential TX Impedance | 80 | 100 | 120 | Ω | TX DC Differential mode Low Impedance |
| $Z_{TX\text{-}DC}$ | Transmitter DC Impedance | 40 | — | — | Ω | Required TX D+ as well as D- DC Impedance during all states |
| $L_{TX\text{-}SKEW}$ | Lane-to-Lane Output Skew | — | — | 500 + 2 UI | ps | Static skew between any two Transmitter Lanes within a single Link |
| $C_{TX}$ | AC Coupling Capacitor | 75 | — | 200 | nF | All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8. |
| $T_{crosslink}$ | Crosslink Random Timeout | 0 | — | 1 | ms | This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 57 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 55.)
3. A $T_{TX\text{-}EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 57). Note that the series capacitors $C_{TX}$ is optional for the return loss measurement.
5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 57 for both $V_{TX\text{-}D+}$ and $V_{TX\text{-}D\text{-}}$.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a.
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a.
8. MPC8572E SerDes transmitter does not have $C_{TX}$ built-in. An external AC Coupling capacitor is required.

### 16.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 55 is specified using the passive compliance/test measurement load (see Figure 57) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

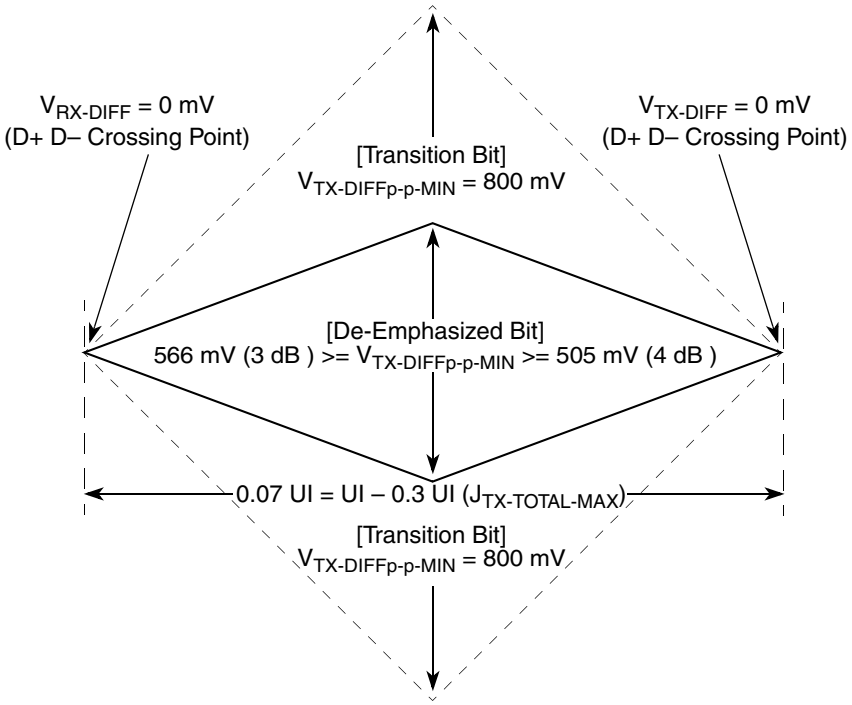



**Figure 55. Minimum Transmitter Timing and Voltage Output Compliance Specifications**

### 16.4.3 Differential Receiver (RX) Input Specifications

Table 63 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

**Table 63. Differential Receiver (RX) Input Specifications**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $V_{RX-DIFFp-p}$ | Differential Input Peak-to-Peak Voltage | 0.175 | — | 1.200 | V | $V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$<br>See Note 2. |
| $T_{RX-EYE}$ | Minimum Receiver Eye Width | 0.4 | — | — | UI | The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI.<br>See Notes 2 and 3. |
| $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7. |
| $V_{RX-CM-ACp}$ | AC Peak Common Mode Input Voltage | — | — | 150 | mV | $V_{RX-CM-ACp} = \|V_{RXD+} + V_{RXD-}\|/2 - V_{RX-CM-DC}$<br>$V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\|/2$<br>See Note 2 |
| $RL_{RX-DIFF}$ | Differential Return Loss | 15 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively.<br>See Note 4 |
| $RL_{RX-CM}$ | Common Mode Return Loss | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4 |
| $Z_{RX-DIFF-DC}$ | DC Differential Input Impedance | 80 | 100 | 120 | Ω | RX DC Differential mode impedance. See Note 5 |
| $Z_{RX-DC}$ | DC Input Impedance | 40 | 50 | 60 | Ω | Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5. |
| $Z_{RX-HIGH-IMP-DC}$ | Powered Down DC Input Impedance | 200 k | — | — | Ω | Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6. |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical Idle Detect Threshold | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$<br>Measured at the package pins of the Receiver |

**Table 63. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nominal | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Unexpected Electrical Idle Enter Detect Threshold Integration Time | — | — | 10 | ms | An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition. |
| $L_{RX-SKEW}$ | Total Skew | — | — | 20 | ns | Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 57 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 56). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 57). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit does not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 56 is specified using the passive compliance/test measurement load (see Figure 57) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 57) is larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 56) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 57). Note that the series capacitors, CTX, are optional for the return loss measurement.

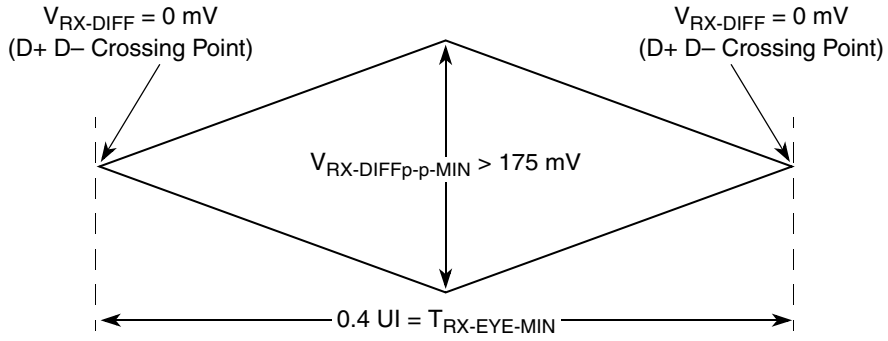



**Figure 56. Minimum Receiver Eye Timing and Voltage Compliance Specification**

### 16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 57.

**NOTE**

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

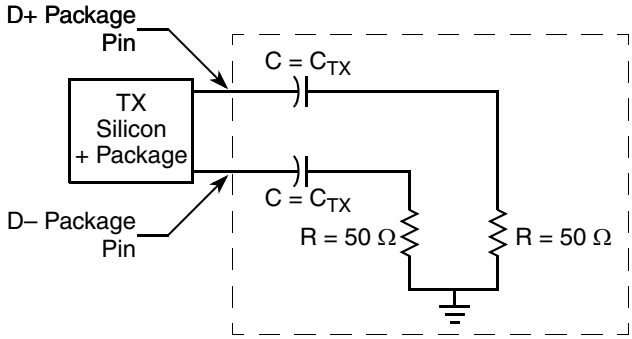



**Figure 57. Compliance Test/Measurement Load**

# 17 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8572E for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

## 17.1 DC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

For more information, see Section 15.2, "SerDes Reference Clocks."

## 17.2 AC Requirements for Serial RapidIO SD1_REF_CLK and SD1_REF_CLK

Figure 64lists the AC requirements.

**Table 64. SD*n*_REF_CLK and SD*n*_REF_CLK AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10(8) | — | ns | 8 ns applies only to serial RapidIO with 125-MHz reference clock |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 80 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –40 | — | 40 | ps | — |

## 17.3 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

## 17.4 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—FIFO/GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics." The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

## 17.5 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

**Table 65. Short Run Transmitter AC Timing Specifications—1.25 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 800 | 800 | ps | +/- 100 ppm |

**Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |

**Table 66. Short Run Transmitter AC Timing Specifications—2.5 GBaud (continued)**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Multiple Output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 400 | 400 | ps | +/- 100 ppm |

**Table 67. Short Run Transmitter AC Timing Specifications—3.125 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 320 | 320 | ps | +/– 100 ppm |

**Table 68. Long Run Transmitter AC Timing Specifications—1.25 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 800 | 800 | ps | +/- 100 ppm |

**Table 69. Long Run Transmitter AC Timing Specifications—2.5 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 400 | 400 | ps | +/- 100 ppm |

**Table 70. Long Run Transmitter AC Timing Specifications—3.125 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 320 | 320 | ps | +/- 100 ppm |

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 58 with the parameters specified in Figure 71 when measured at the output pins of the device and the device is driving a 100 Ω +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

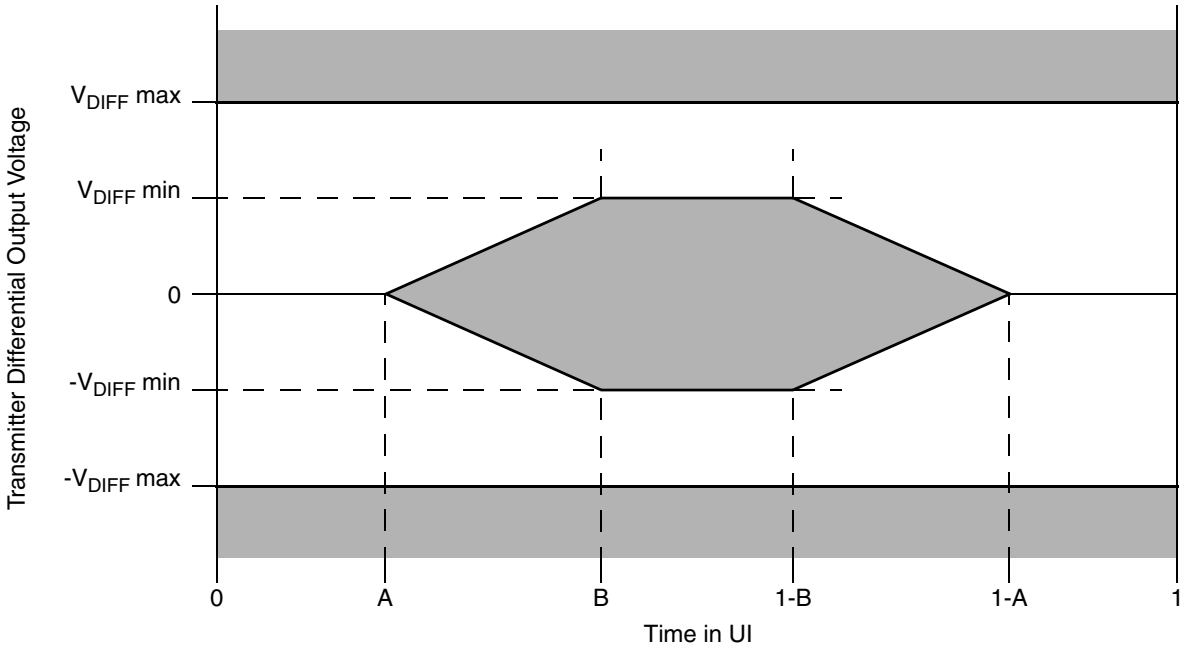



**Figure 58. Transmitter Output Compliance Mask**

**Table 71. Transmitter Differential Output Eye Diagram Parameters**

| Transmitter Type | $V_{DIFF}$min (mV) | $V_{DIFF}$max (mV) | A (UI) | B (UI) |
|---|---|---|---|---|
| 1.25 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 1.25 GBaud long range | 400 | 800 | 0.175 | 0.39 |
| 2.5 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 2.5 GBaud long range | 400 | 800 | 0.175 | 0.39 |
| 3.125 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 3.125 GBaud long range | 400 | 800 | 0.175 | 0.39 |

## 17.6 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25-Ω resistive for common mode.

**Table 72. Receiver AC Timing Specifications—1.25 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential Input Voltage | $V_{IN}$ | 200 | 1600 | mV p-p | Measured at receiver |
| Deterministic Jitter Tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined Deterministic and Random Jitter Tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total Jitter Tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple Input Skew | $S_{MI}$ | — | 24 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit Error Rate | BER | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 800 | 800 | ps | +/– 100 ppm |

**Note:**
1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

**Table 73. Receiver AC Timing Specifications—2.5 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential Input Voltage | $V_{IN}$ | 200 | 1600 | mV p-p | Measured at receiver |
| Deterministic Jitter Tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined Deterministic and Random Jitter Tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total Jitter Tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple Input Skew | $S_{MI}$ | — | 24 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit Error Rate | BER | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 400 | 400 | ps | +/– 100 ppm |

**Note:**
1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

**Table 74. Receiver AC Timing Specifications—3.125 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential Input Voltage | $V_{IN}$ | 200 | 1600 | mV p-p | Measured at receiver |
| Deterministic Jitter Tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined Deterministic and Random Jitter Tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total Jitter Tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple Input Skew | $S_{MI}$ | — | 22 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit Error Rate | BER | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 320 | 320 | ps | +/- 100 ppm |

**Note:**

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 59. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

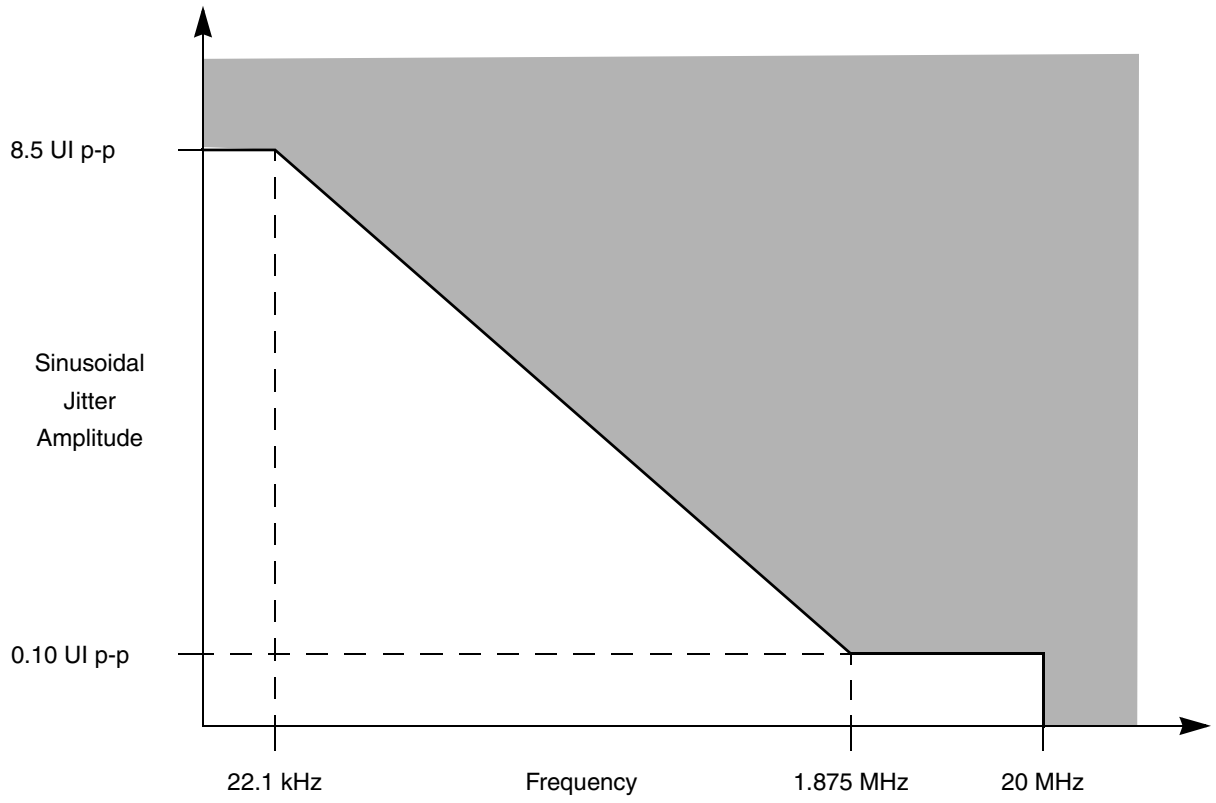



**Figure 59. Single Frequency Sinusoidal Jitter Limits**

## 17.7 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 72, Table 73, and Table 74) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 60 with the parameters specified in Table 75. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100-Ω +/– 5% differential resistive load.

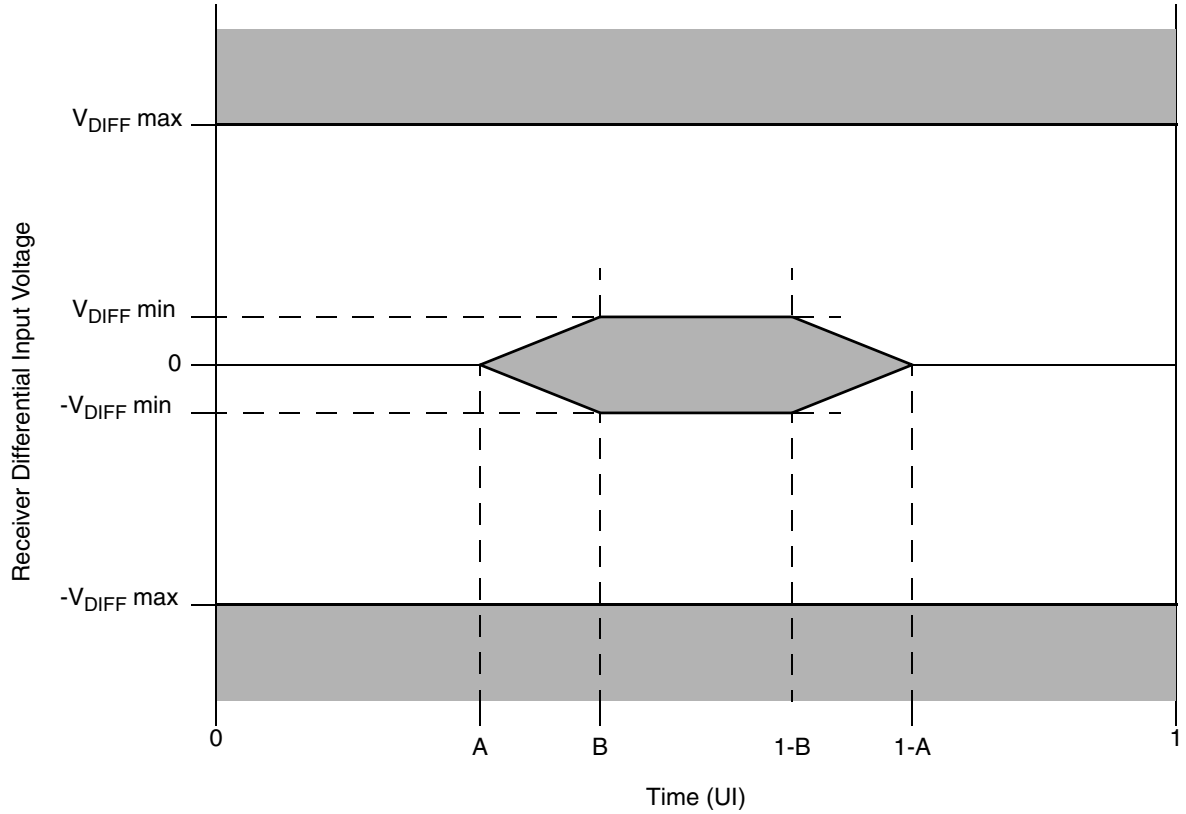



**Figure 60. Receiver Input Compliance Mask**

**Table 75. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter**

| Receiver Type | $V_{DIFF}$min (mV) | $V_{DIFF}$max (mV) | A (UI) | B (UI) |
|---|---|---|---|---|
| 1.25 GBaud | 100 | 800 | 0.275 | 0.400 |
| 2.5 GBaud | 100 | 800 | 0.275 | 0.400 |
| 3.125 GBaud | 100 | 800 | 0.275 | 0.400 |

## 17.8 Measurement and Test Requirements

Because the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. Additionally, the CJPAT test pattern defined in Annex 48A of IEEE 802.3ae-2002 is

specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

### 17.8.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than $10^{-12}$. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive +/– 5% differential to 2.5 GHz.

### 17.8.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

### 17.8.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive +/– 5% differential to 2.5 GHz.

### 17.8.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 17.6, “Receiver Specifications,” and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 60 and Table 75. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 17.6, “Receiver Specifications,” is then added to the signal and the test load is replaced by the receiver being tested.

# 18 Package Description

This section describes package parameters, pin assignments, and dimensions.

## 18.1 Package Parameters for the MPC8572E FC-PBGA

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1023 flip chip plastic ball grid array (FC-PBGA).

| | |
|---|---|
| Package outline | 33 mm × 33 mm |
| Interconnects | 1023 |
| Ball Pitch | 1 mm |
| Ball Diameter (Typical) | 0.6 mm |
| Solder Balls | 63% Sn<br>37% Pb |
| Solder Balls (Lead-Free) | 96.5% Sn<br>3.5% Ag |

## 18.2 Mechanical Dimensions of the MPC8572E FC-PBGA

Figure 61 shows the mechanical dimensions of the MPC8572E FC-PBGA package with full lid.

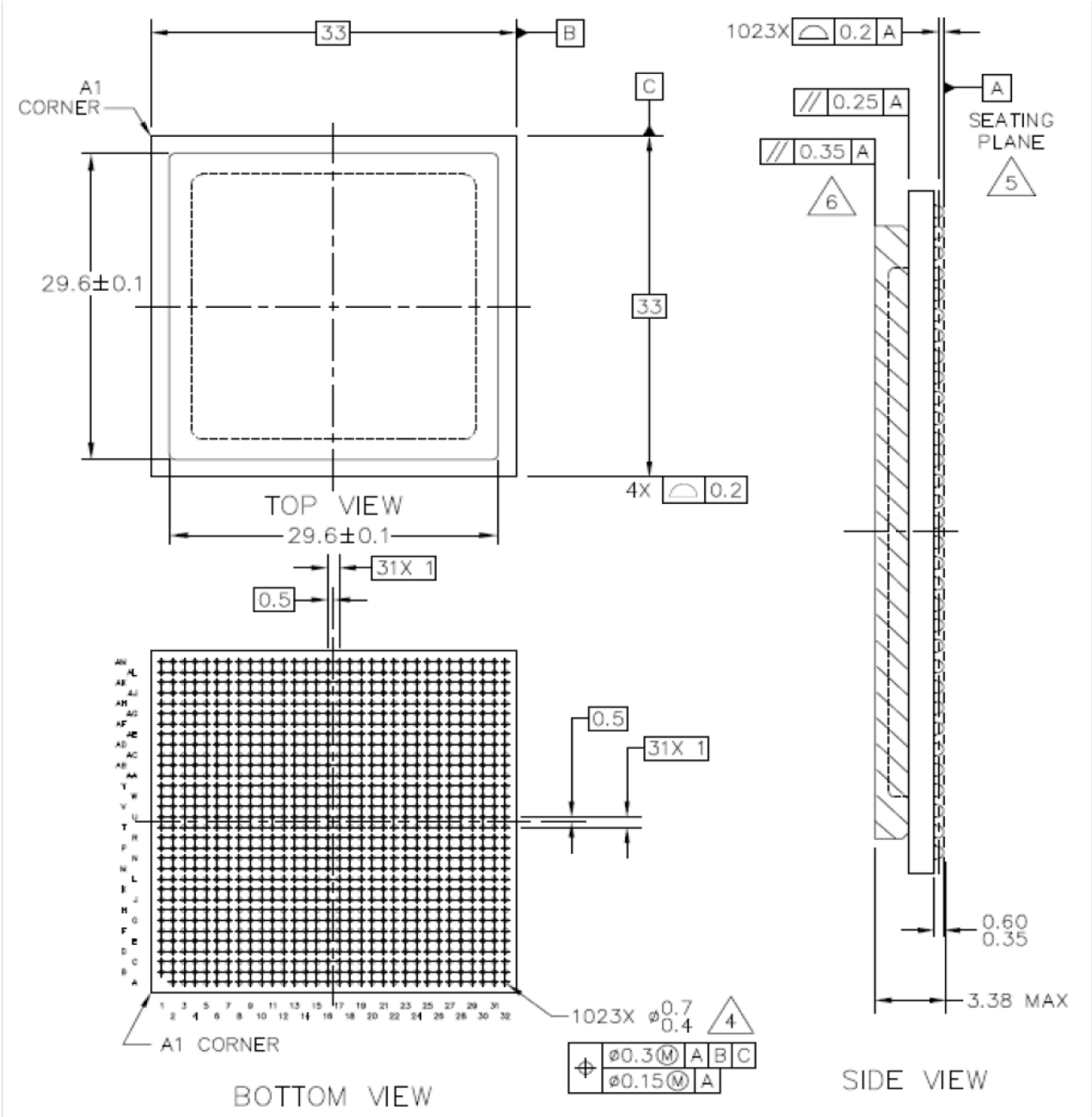



**Figure 61. Mechanical Dimensions of the MPC8572E FC-PBGA with Full Lid**

**NOTES:**
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

6. Parallelism measurement shall exclude any effect of mark on top surface of package.

## 18.3 Pinout Listings

Table 76 provides the pin-out listing for the MPC8572E 1023 FC-PBGA package.

**Table 76. MPC8572E Pinout Listing**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| **DDR SDRAM Memory Interface 1** | | | | | |
| D1_MDQ[0:63] | Data | D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L10, M11, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AK14, AL11, AM11, AK13, AM14, AM15, AJ16, AL18, AM18, AJ15, AL15, AK17, AM17 | I/O | $GV_{DD}$ | — |
| D1_MECC[0:7] | Error Correcting Code | M10, M7, R8, T11, L12, L11, P9, R10 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D1_MAPAR_ERR}}$ | Address Parity Error | P6 | I | $GV_{DD}$ | — |
| D1_MAPAR_OUT | Address Parity Out | W6 | O | $GV_{DD}$ | — |
| D1_MDM[0:8] | Data Mask | C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N11 | O | $GV_{DD}$ | — |
| D1_MDQS[0:8] | Data Strobe | A13, C10, H12, J7, AE8, AM9, AM13, AL17, N9 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D1_MDQS}}$[0:8] | Data Strobe | D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10 | I/O | $GV_{DD}$ | — |
| D1_MA[0:15] | Address | Y7, W8, U6, W9, U7, V8, Y11, V10, T6, V11, AA10, U9, U10, AD11, T8, P7 | O | $GV_{DD}$ | — |
| D1_MBA[0:2] | Bank Select | AA7, AA8, R7 | O | $GV_{DD}$ | — |
| $\overline{\text{D1_MWE}}$ | Write Enable | AC12 | O | $GV_{DD}$ | — |
| $\overline{\text{D1_MCAS}}$ | Column Address Strobe | AC9 | O | $GV_{DD}$ | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| $\overline{\text{D1_MRAS}}$ | Row Address Strobe | AB12 | O | $GV_{DD}$ | — |
| D1_MCKE[0:3] | Clock Enable | M8, L9, T9, N8 | O | $GV_{DD}$ | 11 |
| $\overline{\text{D1_MCS}}$[0:3] | Chip Select | AB9, AF10, AB11, AE11 | O | $GV_{DD}$ | — |
| D1_MCK[0:5] | Clock | V7, E13, AH11, Y9, F14, AG10 | O | $GV_{DD}$ | — |
| $\overline{\text{D1_MCK}}$[0:5] | Clock Complements | Y10, E12, AH12, AA11, F13, AG11 | O | $GV_{DD}$ | — |
| D1_MODT[0:3] | On Die Termination | AD10, AF12, AC10, AE12 | O | $GV_{DD}$ | — |
| D1_MDIC[0:1] | Driver Impedance Calibration | E15, G14 | I/O | $GV_{DD}$ | 25 |
| **DDR SDRAM Memory Interface 2** | | | | | |
| D2_MDQ[0:63] | Data | A6, B7, C5, D5, A7, C8, D8, D6, C4, A3, D3, D2, B4, A4, B1, C1, E3, E1, G2, G6, D1, E4, G5, G3, J4, J2, P4, R5, H3, H1, N5, N3, Y6, Y4, AC3, AD2, V5, W5, AB2, AB3, AD5, AE3, AF6, AG7, AC4, AD4, AF4, AF7, AH5, AJ1, AL2, AM3, AH3, AH6, AM1, AL3, AK5, AL5, AJ7, AK7, AK4, AM4, AL6, AM7 | I/O | $GV_{DD}$ | — |
| D2_MECC[0:7] | Error Correcting Code | J5, H7, L7, N6, H4, H6, M4, M5 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D2_MAPAR_ERR}}$ | Address Parity Error | N1 | I | $GV_{DD}$ | — |
| D2_MAPAR_OUT | Address Parity Out | W2 | O | $GV_{DD}$ | — |
| D2_MDM[0:8] | Data Mask | A5, B3, F4, J1, AA4, AE5, AK1, AM5, K5 | O | $GV_{DD}$ | — |
| D2_MDQS[0:8] | Data Strobe | B6, C2, F5, L4, AB5, AF3, AL1, AM6, L6 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D2_MDQS}}$[0:8] | Data Strobe | C7, A2, F2, K3, AA5, AE6, AK2, AJ6, K6 | I/O | $GV_{DD}$ | — |
| D2_MA[0:15] | Address | W1, U4, U3, T1, T2, T3, R1, R2, T5, R4, Y3, P1, N2, AF1, M2, M1 | O | $GV_{DD}$ | — |
| D2_MBA[0:2] | Bank Select | Y1, W3, P3 | O | $GV_{DD}$ | — |
| $\overline{\text{D2_MWE}}$ | Write Enable | AA2 | O | $GV_{DD}$ | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| D2_MCAS | Column Address Strobe | AD1 | O | $GV_{DD}$ | — |
| D2_MRAS | Row Address Strobe | AA1 | O | $GV_{DD}$ | — |
| D2_MCKE[0:3] | Clock Enable | L3, L1, K1, K2 | O | $GV_{DD}$ | 11 |
| D2_MCS[0:3] | Chip Select | AB1, AG2, AC1, AH2 | O | $GV_{DD}$ | — |
| D2_MCK[0:5] | Clock | V4, F7, AJ3, V2, E7, AG4 | O | $GV_{DD}$ | — |
| D2_MCK[0:5] | Clock Complements | V1, F8, AJ4, U1, E6, AG5 | O | $GV_{DD}$ | — |
| D2_MODT[0:3] | On Die Termination | AE1, AG1, AE2, AH1 | O | $GV_{DD}$ | — |
| D2_MDIC[0:1] | Driver Impedance Calibration | F1, G1 | I/O | $GV_{DD}$ | 25 |
| **Local Bus Controller Interface** | | | | | |
| LAD[0:31] | Muxed Data/Address | M22, L22, F22, G22, F21, G21, E20, H22, K22, K21, H19, J20, J19, L20, M20, M19, E22, E21, L19, K19, G19, H18, E18, G18, J17, K17, K14, J15, H16, J14, H15, G15 | I/O | $BV_{DD}$ | 34 |
| LDP[0:3] | Data Parity | M21, D22, A24, E17 | I/O | $BV_{DD}$ | — |
| LA[27] | Burst Address | J21 | O | $BV_{DD}$ | 5, 9 |
| LA[28:31] | Port Address | F20, K18, H20, G17 | O | $BV_{DD}$ | 5, 7, 9 |
| LCS[0:4] | Chip Selects | B23, E16, D20, B25, A22 | O | $BV_{DD}$ | 10 |
| LCS[5]/DMA2_DREQ[1] | Chip Selects / DMA Request | D19 | I/O | $BV_{DD}$ | 1, 10 |
| LCS[6]/DMA2_DACK[1] | Chip Selects / DMA Ack | E19 | O | $BV_{DD}$ | 1, 10 |
| LCS[7]/DMA2_DDONE[1] | Chip Selects / DMA Done | C21 | O | $BV_{DD}$ | 1, 10 |
| LWE[0]/LBS[0]/LFWE | Write Enable / Byte Select | D17 | O | $BV_{DD}$ | 5, 9 |
| LWE[1]/LBS[1] | Write Enable / Byte Select | F15 | O | $BV_{DD}$ | 5, 9 |
| LWE[2]/LBS[2] | Write Enable / Byte Select | B24 | O | $BV_{DD}$ | 5, 9 |
| LWE[3]/LBS[3] | Write Enable / Byte Select | D18 | O | $BV_{DD}$ | 5, 9 |
| LALE | Address Latch Enable | F19 | O | $BV_{DD}$ | 5, 8, 9 |
| LBCTL | Buffer Control | L18 | O | $BV_{DD}$ | 5, 8, 9 |
| LGPL0/LFCLE | UPM General Purpose Line 0 / Flash Command Latch Enable | J13 | O | $BV_{DD}$ | 5, 9 |
| LGPL1/LFALE | UPM General Purpose Line 1/ Flash Address Latch Enable | J16 | O | $BV_{DD}$ | 5, 9 |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ | UPM General Purpose Line 2 / Output Enable / Flash Read Enable | A27 | O | $BV_{DD}$ | 5, 8, 9 |
| LGPL3/$\overline{\text{LFWP}}$ | UPM General Purpose Line 3 / Flash Write Protect | K16 | O | $BV_{DD}$ | 5, 9 |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE/LFRB | UPM General Purpose Line 4 / Target Ack / Wait / Parity Byte Select / Flash Ready-Busy | L17 | I/O | $BV_{DD}$ | — |
| LGPL5 | UPM General Purpose Line 5 / Amux | B26 | O | $BV_{DD}$ | 5, 9 |
| LCLK[0:2] | Local Bus Clock | F17, F16, A23 | O | $BV_{DD}$ | — |
| LSYNC_IN | Local Bus DLL Synchronization | B22 | I | $BV_{DD}$ | — |
| LSYNC_OUT | Local Bus DLL Synchronization | A21 | O | $BV_{DD}$ | — |
| **DMA** | | | | | |
| $\overline{\text{DMA1_DACK}}$[0:1] | DMA Acknowledge | W25, U30 | O | $OV_{DD}$ | 21 |
| $\overline{\text{DMA2_DACK}}$[0] | DMA Acknowledge | AA26 | O | $OV_{DD}$ | 5, 9 |
| $\overline{\text{DMA1_DREQ}}$[0:1] | DMA Request | Y29, V27 | I | $OV_{DD}$ | — |
| $\overline{\text{DMA2_DREQ}}$[0] | DMA Request | V29 | I | $OV_{DD}$ | — |
| $\overline{\text{DMA1_DDONE}}$[0:1] | DMA Done | Y28, V30 | O | $OV_{DD}$ | 5, 9 |
| $\overline{\text{DMA2_DDONE}}$[0] | DMA Done | AA28 | O | $OV_{DD}$ | 5, 9 |
| $\overline{\text{DMA2_DREQ}}$[2] | DMA Request | M23 | I | $BV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | | |
| $\overline{\text{UDE0}}$ | Unconditional Debug Event Processor 0 | AC25 | I | $OV_{DD}$ | — |
| $\overline{\text{UDE1}}$ | Unconditional Debug Event Processor 1 | AA25 | I | $OV_{DD}$ | — |
| $\overline{\text{MCP0}}$ | Machine Check Processor 0 | M28 | I | $OV_{DD}$ | — |
| $\overline{\text{MCP1}}$ | Machine Check Processor 1 | L28 | I | $OV_{DD}$ | — |
| IRQ[0:11] | External Interrupts | T24, R24, R25, R27, R28, AB27, AB28, P27, R30, AC28, R29, T31 | I | $OV_{DD}$ | — |
| $\overline{\text{IRQ_OUT}}$ | Interrupt Output | U24 | O | $OV_{DD}$ | 2, 4 |
| **1588** | | | | | |
| TSEC_1588_CLK | Clock In | AM22 | I | $LV_{DD}$ | — |
| TSEC_1588_TRIG_IN | Trigger In | AM23 | I | $LV_{DD}$ | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TSEC_1588_TRIG_OUT | Trigger Out | AA23 | O | $LV_{DD}$ | 5, 9 |
| TSEC_1588_CLK_OUT | Clock Out | AC23 | O | $LV_{DD}$ | 5, 9 |
| TSEC_1588_PULSE_OUT1 | Pulse Out1 | AA22 | O | $LV_{DD}$ | 5, 9 |
| TSEC_1588_PULSE_OUT2 | Pulse Out2 | AB23 | O | $LV_{DD}$ | 5, 9 |
| **Ethernet Management Interface 1** | | | | | |
| EC1_MDC | Management Data Clock | AL30 | O | $LV_{DD}$ | 5, 9 |
| EC1_MDIO | Management Data In/Out | AM25 | I/O | $LV_{DD}$ | — |
| **Ethernet Management Interface 3** | | | | | |
| EC3_MDC | Management Data Clock | AF19 | O | $TV_{DD}$ | 5, 9 |
| EC3_MDIO | Management Data In/Out | AF18 | I/O | $TV_{DD}$ | — |
| **Ethernet Management Interface 5** | | | | | |
| EC5_MDC | Management Data Clock | AF14 | O | $TV_{DD}$ | 21 |
| EC5_MDIO | Management Data In/Out | AF15 | I/O | $TV_{DD}$ | — |
| **Gigabit Ethernet Reference Clock** | | | | | |
| EC_GTX_CLK125 | Reference Clock | AM24 | I | $LV_{DD}$ | 32 |
| **Three-Speed Ethernet Controller 1** | | | | | |
| TSEC1_RXD[7:0]/FIFO1_RXD[7:0] | Receive Data | AM28, AL28, AM26, AK23, AM27, AK26, AL29, AM30 | I | $LV_{DD}$ | 1 |
| TSEC1_TXD[7:0]/FIFO1_TXD[7:0] | Transmit Data | AC20, AD20, AE22, AB22, AC22, AD21, AB21, AE21 | O | $LV_{DD}$ | 1, 5, 9 |
| TSEC1_COL/FIFO1_TX_FC | Collision Detect/Flow Control | AJ23 | I | $LV_{DD}$ | 1 |
| TSEC1_CRS/FIFO1_RX_FC | Carrier Sense/Flow Control | AM31 | I/O | $LV_{DD}$ | 1, 16 |
| TSEC1_GTX_CLK | Transmit Clock Out | AK27 | O | $LV_{DD}$ | |
| TSEC1_RX_CLK/FIFO1_RX_CLK | Receive Clock | AL25 | I | $LV_{DD}$ | 1 |
| TSEC1_RX_DV/FIFO1_RX_DV/FIFO1_RXC[0] | Receive Data Valid | AL24 | I | $LV_{DD}$ | 1 |
| TSEC1_RX_ER/FIFO1_RX_ER/FIFO1_RXC[1] | Receive Data Error | AM29 | I | $LV_{DD}$ | 1 |
| TSEC1_TX_CLK/FIFO1_TX_CLK | Transmit Clock In | AB20 | I | $LV_{DD}$ | 1 |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TSEC1_TX_EN/FIFO1_TX_EN/FIFO1_TXC[0] | Transmit Enable | AJ24 | O | $LV_{DD}$ | 1, 22 |
| TSEC1_TX_ER/FIFO1_TX_ERR/FIFO1_TXC[1] | Transmit Error | AK25 | O | $LV_{DD}$ | 1, 5, 9 |
| **Three-Speed Ethernet Controller 2** | | | | | |
| TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/FIFO1_RXD[15:8] | Receive Data | AG22, AH20, AL22, AG20, AK21, AK22, AJ21, AK20 | I | $LV_{DD}$ | 1 |
| TSEC2_TXD[7:0]/FIFO2_TXD[7:0]/FIFO1_TXD[15:8] | Transmit Data | AH21, AF20, AC17, AF21, AD18, AF22, AE20, AB18 | O | $LV_{DD}$ | 1, 5, 9, 24 |
| TSEC2_COL/FIFO2_TX_FC | Collision Detect/Flow Control | AE19 | I | $LV_{DD}$ | 1 |
| TSEC2_CRS/FIFO2_RX_FC | Carrier Sense/Flow Control | AJ20 | I/O | $LV_{DD}$ | 1, 16 |
| TSEC2_GTX_CLK | Transmit Clock Out | AE18 | O | $LV_{DD}$ | — |
| TSEC2_RX_CLK/FIFO2_RX_CLK | Receive Clock | AL23 | I | $LV_{DD}$ | 1 |
| TSEC2_RX_DV/FIFO2_RX_DV/FIFO1_RXC[2] | Receive Data Valid | AJ22 | I | $LV_{DD}$ | 1 |
| TSEC2_RX_ER/FIFO2_RX_ER | Receive Data Error | AD19 | I | $LV_{DD}$ | 1 |
| TSEC2_TX_CLK/FIFO2_TX_CLK | Transmit Clock In | AC19 | I | $LV_{DD}$ | 1 |
| TSEC2_TX_EN/FIFO2_TX_EN/FIFO1_TXC[2] | Transmit Enable | AB19 | O | $LV_{DD}$ | 1, 22 |
| TSEC2_TX_ER/FIFO2_TX_ERR | Transmit Error | AB17 | O | $LV_{DD}$ | 1, 5, 9 |
| **Three-Speed Ethernet Controller 3** | | | | | |
| TSEC3_TXD[3:0]/FEC_TXD[3:0]/FIFO3_TXD[3:0] | Transmit Data | AG18, AG17, AH17, AH19 | O | $TV_{DD}$ | 1, 5, 9 |
| TSEC3_RXD[3:0]/FEC_RXD[3:0]/FIFO3_RXD[3:0] | Receive Data | AG16, AK19, AD16, AJ19 | I | $TV_{DD}$ | 1 |
| TSEC3_GTX_CLK | Transmit Clock Out | AE17 | O | $TV_{DD}$ | |
| TSEC3_RX_CLK/FEC_RX_CLK/FIFO3_RX_CLK | Receive Clock | AF17 | I | $TV_{DD}$ | 1 |
| TSEC3_RX_DV/FEC_RX_DV/FIFO3_RX_DV | Receive Data Valid | AG14 | I | $TV_{DD}$ | 1 |
| TSEC3_RX_ER/FEC_RX_ER/FIFO3_RX_ER | Receive Error | AH15 | I | $TV_{DD}$ | 1 |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| TSEC3_TX_CLK/FEC_TX_CLK/FIFO3_TX_CLK | Transmit Clock In | AF16 | I | $TV_{DD}$ | 1 |
| TSEC3_TX_EN/FEC_TX_EN/FIFO3_TX_EN | Transmit Enable | AJ18 | O | $TV_{DD}$ | 1, 22 |
| **Three-Speed Ethernet Controller 4** | | | | | |
| TSEC4_TXD[3:0]/TSEC3_TXD[7:4]/FIFO3_TXD[7:4] | Transmit Data | AD15, AC16, AC14, AB16 | O | $TV_{DD}$ | 1, 5, 9 |
| TSEC4_RXD[3:0]/TSEC3_RXD[7:4]/FIFO3_RXD[7:4] | Receive Data | AE15, AF13, AE14, AH14 | I | $TV_{DD}$ | 1 |
| TSEC4_GTX_CLK | Transmit Clock Out | AB14 | O | $TV_{DD}$ | — |
| TSEC4_RX_CLK/TSEC3_COL/FEC_COL/FIFO3_TX_FC | Receive Clock | AG13 | I | $TV_{DD}$ | 1 |
| TSEC4_RX_DV/TSEC3_CRS/FEC_CRS/FIFO3_RX_FC | Receive Data Valid | AD13 | I/O | $TV_{DD}$ | 1, 23 |
| TSEC4_TX_EN/TSEC3_TX_ER/FEC_TX_ER/FIFO3_TX_ER | Transmit Enable | AB15 | O | $TV_{DD}$ | 1, 22 |
| **DUART** | | | | | |
| $\overline{\text{UART_CTS}}$[0:1] | Clear to Send | W30, Y27 | I | $OV_{DD}$ | — |
| $\overline{\text{UART_RTS}}$[0:1] | Ready to Send | W31, Y30 | O | $OV_{DD}$ | 5, 9 |
| UART_SIN[0:1] | Receive Data | Y26, W29 | I | $OV_{DD}$ | — |
| UART_SOUT[0:1] | Transmit Data | Y25, W26 | O | $OV_{DD}$ | 5, 9 |
| **$I^2C$ Interface** | | | | | |
| IIC1_SCL | Serial Clock | AC30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC1_SDA | Serial Data | AB30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC2_SCL | Serial Clock | AD30 | I/O | $OV_{DD}$ | 4, 20 |
| IIC2_SDA | Serial Data | AD29 | I/O | $OV_{DD}$ | 4, 20 |
| **SerDes (x10) PCIe, SRIO** | | | | | |
| SD1_RX[7:0] | Receive Data (positive) | P32, N30, M32, L30, G30, F32, E30, D32 | I | $XV_{DD_SRDS1}$ | — |
| $\overline{\text{SD1_RX}}$[7:0] | Receive Data (negative) | P31, N29, M31, L29, G29, F31, E29, D31 | I | $XV_{DD_SRDS1}$ | — |
| SD1_TX[7] | PCIe1 Tx Data Lane 7 / SRIO or PCIe2 Tx Data Lane 3 / PCIe3 TX Data Lane 1 | M26 | O | $XV_{DD_SRDS1}$ | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| SD1_TX[6] | PCIe1 Tx Data Lane 6 / SRIO or PCIe2 Tx Data Lane 2 / PCIe3 TX Data Lane 0 | L24 | O | $XV_{DD_SRDS1}$ | — |
| SD1_TX[5] | PCIe1 Tx Data Lane 5 / SRIO or PCIe2 Tx Data Lane 1 | K26 | O | $XV_{DD_SRDS1}$ | — |
| SD1_TX[4] | PCIe1 Tx Data Lane 4 / SRIO or PCIe2 Tx Data Lane 0 | J24 | O | $XV_{DD_SRDS1}$ | — |
| SD1_TX[3] | PCIe1 Tx Data Lane 3 | G24 | O | $XV_{DD_SRDS1}$ | — |
| SD1_TX[2] | PCIe1 Tx Data Lane 2 | F26 | O | $XV_{DD_SRDS1}$ | — |
| SD1_TX[1] | PCIe1 Tx Data Lane 1] | E24 | O | $XV_{DD_SRDS1}$ | — |
| SD1_TX[0] | PCIe1 Tx Data Lane 0 | D26 | O | $XV_{DD_SRDS1}$ | — |
| $\overline{\text{SD1_TX}}$[7:0] | Transmit Data (negative) | M27, L25, K27, J25, G25, F27, E25, D27 | O | $XV_{DD_SRDS1}$ | — |
| SD1_PLL_TPD | PLL Test Point Digital | J32 | O | $XV_{DD_SRDS1}$ | 17 |
| SD1_REF_CLK | PLL Reference Clock | H32 | I | $XV_{DD_SRDS1}$ | — |
| $\overline{\text{SD1_REF_CLK}}$ | PLL Reference Clock Complement | H31 | I | $XV_{DD_SRDS1}$ | — |
| Reserved | — | C29, K32 | — | — | 26 |
| Reserved | — | C30, K31 | — | — | 27 |
| Reserved | — | C24, C25, H26, H27 | — | — | 28 |
| Reserved | — | AL20, AL21 | — | — | 29 |
| **SerDes (x4) SGMII** | | | | | |
| SD2_RX[3:0] | Receive Data (positive) | AK32, AJ30, AF30, AE32 | I | $XV_{DD_SRDS2}$ | — |
| $\overline{\text{SD2_RX}}$[3:0] | Receive Data (negative) | AK31, AJ29, AF29, AE31 | I | $XV_{DD_SRDS2}$ | — |
| SD2_TX[3] | SGMII Tx Data eTSEC4 | AH26 | O | $XV_{DD_SRDS2}$ | — |
| SD2_TX[2] | SGMII Tx Data eTSEC3 | AG24 | O | $XV_{DD_SRDS2}$ | — |
| SD2_TX[1] | SGMII Tx Data eTSEC2 | AE24 | O | $XV_{DD_SRDS2}$ | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| SD2_TX[0] | SGMII Tx Data eTSEC1 | AD26 | O | $XV_{DD_SR\ DS2}$ | — |
| $\overline{\text{SD2_TX}}$[3:0] | Transmit Data (negative) | AH27, AG25, AE25, AD27 | O | $XV_{DD_SR\ DS2}$ | — |
| SD2_PLL_TPD | PLL Test Point Digital | AH32 | O | $XV_{DD_SR\ DS2}$ | 17 |
| SD2_REF_CLK | PLL Reference Clock | AG32 | I | $XV_{DD_SR\ DS2}$ | — |
| $\overline{\text{SD2_REF_CLK}}$ | PLL Reference Clock Complement | AG31 | I | $XV_{DD_SR\ DS2}$ | — |
| Reserved | — | AF26, AF27 | — | — | 28 |
| **General-Purpose Input/Output** | | | | | |
| GPINOUT[0:7] | General Purpose Input / Output | B27, A28, B31, A32, B30, A31, B28, B29 | I/O | $BV_{DD}$ | — |
| **System Control** | | | | | |
| $\overline{\text{HRESET}}$ | Hard Reset | AC31 | I | $OV_{DD}$ | — |
| $\overline{\text{HRESET_REQ}}$ | Hard Reset Request | L23 | O | $OV_{DD}$ | 21 |
| $\overline{\text{SRESET}}$ | Soft Reset | P24 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP_IN0}}$ | Checkstop In Processor 0 | N26 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP_IN1}}$ | Checkstop In Processor 1 | N25 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP_OUT0}}$ | Checkstop Out Processor 0 | U29 | O | $OV_{DD}$ | 2, 4 |
| $\overline{\text{CKSTP_OUT1}}$ | Checkstop Out Processor 1 | T25 | O | $OV_{DD}$ | 2, 4 |
| **Debug** | | | | | |
| TRIG_IN | Trigger In | P26 | I | $OV_{DD}$ | — |
| TRIG_OUT/READY_P0/$\overline{\text{QUIESCE}}$ | Trigger Out / Ready Processor 0/ Quiesce | P25 | O | $OV_{DD}$ | 21 |
| READY_P1 | Ready Processor 1 | N28 | O | $OV_{DD}$ | 5, 9 |
| MSRCID[0:1] | Memory Debug Source Port ID | U27, T29 | O | $OV_{DD}$ | 5, 9, 30 |
| MSRCID[2:4] | Memory Debug Source Port ID | U28, W24, W28 | O | $OV_{DD}$ | 21 |
| MDVAL | Memory Debug Data Valid | V26 | O | $OV_{DD}$ | 2, 21 |
| CLK_OUT | Clock Out | U32 | O | $OV_{DD}$ | 11 |
| **Clock** | | | | | |
| RTC | Real Time Clock | V25 | I | $OV_{DD}$ | — |
| SYSCLK | System Clock | Y32 | I | $OV_{DD}$ | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| DDRCLK | DDR Clock | AA29 | I | $OV_{DD}$ | 31 |
| **JTAG** | | | | | |
| TCK | Test Clock | T28 | I | $OV_{DD}$ | |
| TDI | Test Data In | T27 | I | $OV_{DD}$ | 12 |
| TDO | Test Data Out | T26 | O | $OV_{DD}$ | — |
| TMS | Test Mode Select | U26 | I | $OV_{DD}$ | 12 |
| $\overline{\text{TRST}}$ | Test Reset | AA32 | I | $OV_{DD}$ | 12 |
| **DFT** | | | | | |
| L1_TSTCLK | L1 Test Clock | V32 | I | $OV_{DD}$ | 18 |
| L2_TSTCLK | L2 Test Clock | V31 | I | $OV_{DD}$ | 18 |
| $\overline{\text{LSSD_MODE}}$ | LSSD Mode | N24 | I | $OV_{DD}$ | 18 |
| $\overline{\text{TEST_SEL}}$ | Test Select 0 | K28 | I | $OV_{DD}$ | 18 |
| **Power Management** | | | | | |
| ASLEEP | Asleep | P28 | O | $OV_{DD}$ | 9, 15, 21 |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| **Power and Ground Signals** | | | | | |
| GND | Ground | A18, A25, A29, C3, C6, C9, C12, C15, C20, C22, E5, E8, E11, E14, F3, G7, G10, G13, G16, H5, H21, J3, J9, J12, J18, K7, L5, L13, L15, L16, L21, M3, M9, M12, M14, M16, M18, N7, N13, N15, N17, N19, N21, N23, P5, P12, P14, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, R26, T7, T12, T14, T16, T18, T20, T22, T30, U5, U11, U13, U15, U16, U17, U19, U21, U23, U25, V3, V9, V12, V14, V16, V18, V20, V22, W7, W11, W13, W15, W17, W19, W21, W27, W32, Y5, Y12, Y14, Y16, Y18, Y20, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA30, AB7, AB26, AC5, AC11, AC13, AD3, AD9, AD14, AD17, AD22, AE7, AE13, AF5, AF11, AG3, AG9, AG15, AG19, AH7, AH13, AH22, AJ5, AJ11, AJ17, AK3, AK9, AK15, AK24, AL7, AL13, AL19, AL26 | — | — | — |
| XGND_SRDS1 | SerDes Transceiver Pad GND (xpadvss) | C23, C27, D23, D25, E23, E26, F23, F24, G23, G27, H23, H25, J23, J26, K23, K24, L27, M25 | — | — | — |
| XGND_SRDS2 | SerDes Transceiver Pad GND (xpadvss) | AD23, AD25, AE23, AE27, AF23, AF24, AG23, AG26, AH23, AH25, AJ27 | — | — | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| SGND_SRDS1 | SerDes Transceiver Core Logic GND (xcorevss) | C28, C32, D30, E31, F28, F29, G32, H28, H30, J28, K29, L32, M30, N31, P29, R32 | — | — | — |
| SGND_SRDS2 | SerDes Transceiver Core Logic GND (xcorevss) | AE28, AE30, AF28, AF32, AG28, AG30, AH28, AJ28, AJ31, AL32 | — | — | — |
| AGND_SRDS1 | SerDes PLL GND | J31 | — | — | — |
| AGND_SRDS2 | SerDes PLL GND | AH31 | — | — | — |
| OVDD | General I/O Supply | U31, V24, V28, Y31, AA27, AB25, AB29 | — | OVDD | — |
| LVDD | TSEC 1&2 I/O Supply | AC18, AC21, AG21, AL27 | — | LVDD | — |
| TVDD | TSEC 3&4 I/O Supply | AC15, AE16, AH18 | — | TVDD | — |
| GVDD | SSTL_1.8 DDR Supply | B2, B5, B8, B11, B14, D4, D7, D10, D13, E2, F6, F9, F12, G4, H2, H8, H11, H14, J6, K4, K10, K13, L2, L8, M6, N4, N10, P2, P8, R6, T4, T10, U2, U8, V6, W4, W10, Y2, Y8, AA6, AB4, AB10, AC2, AC8, AD6, AD12, AE4, AE10, AF2, AF8, AG6, AG12, AH4, AH10, AH16, AJ2, AJ8, AJ14, AK6, AK12, AK18, AL4, AL10, AL16, AM2 | — | GVDD | — |
| BVDD | Local Bus and GPIO Supply | A26, A30, B21, D16, D21, F18, G20, H17, J22, K15, K20 | — | BVDD | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| VDD | Core, L2, Logic Supply | L14, M13, M15, M17, N12, N14, N16, N20, N22, P11, P13, P15, P17, P19, P21, P23, R12, R14, R16, R18, R20, R22, T13, T15, T19, T21, T23, U12, U14, U18, U20, U22, V13, V15, V17, V19, V21, W12, W14, W16, W18, W20, W22, Y13, Y15, Y17, Y19, Y21, AA12, AA14, AA16, AA18, AA20, AB13 | — | VDD | — |
| SVDD_SRDS1 | SerDes Core 1 Logic Supply (xcorevdd) | C31, D29, E28, E32, F30, G28, G31, H29, K30, L31, M29, N32, P30 | — | — | — |
| SVDD_SRDS2 | SerDes Core 2 Logic Supply (xcorevdd) | AD32, AF31, AG29, AJ32, AK29, AK30 | — | — | — |
| XVDD_SRDS1 | SerDes1 Transceiver Supply (xpadvdd) | C26, D24, E27, F25, G26, H24, J27, K25, L26, M24, N27 | — | — | — |
| XVDD_SRDS2 | SerDes2 Transceiver Supply (xpadvdd) | AD24, AD28, AE26, AF25, AG27, AH24, AJ26 | — | — | — |
| AVDD_LBIU | Local Bus PLL Supply | A19 | — | — | 19 |
| AVDD_DDR | DDR PLL Supply | AM20 | — | — | 19 |
| AVDD_CORE0 | CPU PLL Supply | B18 | — | — | 19 |
| AVDD_CORE1 | CPU PLL Supply | A17 | — | — | 19 |
| AVDD_PLAT | Platform PLL Supply | AB32 | — | — | 19 |
| AVDD_SRDS1 | SerDes1 PLL Supply | J29 | — | — | 19 |
| AVDD_SRDS2 | SerDes2 PLL Supply | AH29 | — | — | 19 |
| SENSEVDD | VDD Sensing Pin | N18 | — | — | 13 |
| SENSEVSS | GND Sensing Pin | P18 | — | — | 13 |
| **Analog Signals** | | | | | |
| MVREF1 | SSTL_1.8 Reference Voltage | C16 | I | $GV_{DD}/2$ | — |
| MVREF2 | SSTL_1.8 Reference Voltage | AM19 | I | $GV_{DD}/2$ | — |
| SD1_IMP_CAL_RX | SerDes1 Rx Impedance Calibration | B32 | I | 200Ω (±1%) to GND | — |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| SD1_IMP_CAL_TX | SerDes1 Tx Impedance Calibration | T32 | I | 100Ω (±1%) to GND | — |
| SD1_PLL_TPA | SerDes1 PLL Test Point Analog | J30 | O | AVDD_SRDS analog | 17 |
| SD2_IMP_CAL_RX | SerDes2 Rx Impedance Calibration | AC32 | I | 200Ω (±1%) to GND | — |
| SD2_IMP_CAL_TX | SerDes2 Tx Impedance Calibration | AM32 | I | 100Ω (±1%) to GND | — |
| SD2_PLL_TPA | SerDes2 PLL Test Point Analog | AH30 | O | AVDD_SRDS analog | 17 |
| TEMP_ANODE | Temperature Diode Anode | AA31 | — | internal diode | 14 |
| TEMP_CATHODE | Temperature Diode Cathode | AB31 | — | internal diode | 14 |
| No Connection Pins | | | | | |

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|
| N/C | No Connection | A16, A20, B16, B17, B19, B20, C17, C18, C19, D28, R31, T17, V23, W23, Y22, Y23, Y24, AA24, AB24, AC24, AC26, AC27, AC29, AD31, AE29, AJ25, AK28, AL31, AM21 | — | — | 17 |

**Note:**

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OVDD.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kO pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[29:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.2, “CCB/SYSCLK PLL Ratio.”
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 19.3, “e500 Core PLL Ratio.”
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore be described as an I/O for boundary scan.
10. If this pin is configured for local bus controller usage, recommend a weak pull-up resistor (2-10 KΩ) be placed on this pin to BVDD, to ensure no random chip select assertion due to possible noise and so on.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the VDD/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive diode.
15. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
16. This pin is only an output in FIFO mode when used as Rx Flow Control.
17. Do not connect.
18. These are test signals for factory use only and must be pulled up (100 Ω - 1 KΩ) to OVDD for normal machine operation.
19. Independent supplies derived from board VDD.
20. Recommend a pull-up resistor (~1 KΩ) be placed on this pin to OVDD.
21. The following pins must NOT be pulled down during power-on reset: $\overline{\text{DMA1_DACK}}$[0:1], EC5_MDC, $\overline{\text{HRESET_REQ}}$, TRIG_OUT/READY_P0/$\overline{\text{QUIESCE}}$, MSRCID[2:4], MDVAL, ASLEEP.
22. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
23. This pin is only an output in eTSEC3 FIFO mode when used as Rx flow control.
24. TSEC2_TXD[1] is used as cfg_dram_type. IT MUST BE VALID AT POWER-UP, EVEN BEFORE HRESET ASSERTION.

**Table 76. MPC8572E Pinout Listing (continued)**

| Signal | Signal Name | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|---|

25. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
26. These pins should be connected to XVDD_SRDS1.
27. These pins should be pulled to ground (XGND_SRDS1) through a 300-Ω (±10%) resistor.
28. These pins should be left floating.
29. These pins should be pulled up to TVDD through a 2–10 KΩ resistor.
30. These pins have other manufacturing or debug test functions. It is recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
31. DDRCLK input is only required when the MPC8572E DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* Rev.0, Table 4-3 in section 4.2.2 “Clock Signals”, section 4.4.3.2 “DDR PLL Ratio” and Table 4-10 “DDR Complex Clock PLL Ratio” for more detailed description regarding DDR controller operation in asynchronous and synchronous modes.
32. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
33. These pins should be pulled to ground (GND).
34. These pins are sampled at POR for General Purpose configuration use by software. Their value has no impact on the functionality of the hardware.

# 19 Clocking

This section describes the PLL configuration of the MPC8572E. Note that the platform clock is identical to the core complex bus (CCB) clock.

## 19.1 Clock Ranges

Table 77 provides the clocking specifications for both processor cores.

**Table 77. MPC8572E Processor Core Clocking Specifications**

| Characteristic | Maximum Processor Core Frequency | | | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1067 MHz | | 1200 MHz | | 1333 MHz | | 1500 MHz | | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | | |
| e500 core processor frequency | 800 | 1067 | 800 | 1200 | 800 | 1333 | 800 | 1500 | MHz | 1, 2 |
| CCB frequency | 400 | 533 | 400 | 533 | 400 | 533 | 400 | 600 | MHz | |
| DDR Data Rate | 400 | 667 | 400 | 667 | 400 | 667 | 400 | 800 | MHz | |

**Notes**:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” Section 19.3, “e500 Core PLL Ratio,” and Section 19.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The processor core frequency speed bins listed also reflect the maximum platform (CCB) and DDR data rate frequency supported by production test. Running CCB and/or DDR data rate higher than the limit shown above, although logically possible via valid clock ratio setting in some condition, is not supported.

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL with clock provided on DDRCLK input pin. Table 78 provides the clocking specifications for the memory bus.

**Table 78. Memory Bus Clocking Specifications**

| Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Memory bus clock frequency | 200 | 400 | MHz | 1, 2, 3, 4 |

**Notes:**
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” Section 19.3, “e500 Core PLL Ratio,” and Section 19.4, “DDR/DDRCLK PLL Ratio,” for ratio settings.
2. The Memory bus clock refers to the MPC8572E memory controllers’ Dn_MCK[0:5] and $\overline{\text{Dn_MCK}}$[0:5] output clocks, running at half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform (CCB) frequency. If the desired DDR data rate is higher than the platform (CCB) frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to Section 19.4, “DDR/DDRCLK PLL Ratio.” The memory bus clock speed must be less than or equal to the CCB clock rate which in turn must be less than the DDR data rate.

As a general guideline when selecting the DDR data rate or platform (CCB) frequency, the following procedures can be used:

- Start with the processor core frequency selection;
- After the processor core frequency is determined, select the platform (CCB) frequency from the limited options listed in Table 80 and Table 81;
- Check the CCB to SYSCLK ratio to verify a valid ratio can be choose from Table 79;
- If the desired DDR data rate can be same as the CCB frequency, use the synchronous DDR mode; Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from Table 82. Note that in asynchronous mode, the DDR data rate must be greater than the platform (CCB) frequency. In other words, running DDR data rate lower than the platform (CCB) frequency in asynchronous mode is not supported by MPC8572E.
- Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

## 19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 79:

- SYSCLK input signal
- Binary value on LA[29:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that, in synchronous mode, the DDR data rate is the determining factor in selecting the CCB bus frequency, because the CCB frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the CCB bus frequency.

**Table 79. CCB Clock Ratio**

| Binary Value of LA[29:31] Signals | CCB:SYSCLK Ratio |
|---|---|
| 000 | 4:1 |
| 001 | 5:1 |
| 010 | 6:1 |
| 011 | 8:1 |
| 100 | 10:1 |
| 101 | 12:1 |
| 110 | Reserved |
| 111 | Reserved |

## 19.3 e500 Core PLL Ratio

The clock speed for each e500 core can be configured differently, determined by the values of various signals at power up.

Table 80 describes the clock ratio between e500 Core0 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LBCTL, LALE and LGPL2/LOE/LFRE at power up, as shown in Table 80.

**Table 80. e500 Core0 to CCB Clock Ratio**

| Binary Value of LBCTL, LALE, LGPL2/LOE/LFRE Signals | e500 Core0:CCB Clock Ratio | Binary Value of LBCTL, LALE, LGPL2/LOE/LFRE Signals | e500 Core0:CCB Clock Ratio |
|---|---|---|---|
| 000 | Reserved | 100 | 2:1 |
| 001 | Reserved | 101 | 5:2 (2.5:1) |
| 010 | Reserved | 110 | 3:1 |
| 011 | 3:2 (1.5:1) | 111 | 7:2 (3.5:1) |

Table 81 describes the clock ratio between e500 Core1 and the e500 core complex bus (CCB). This ratio is determined by the binary value of LWE[0]/LBS[0]/LFWE, UART_SOUT[1], and READY_P1 signals at power up, as shown in Table 81.

**Table 81. e500 Core1 to CCB Clock Ratio**

| Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals | e500 Core1:CCB Clock Ratio | Binary Value of LWE[0]/LBS[0]/ LFWE, UART_SOUT[1], READY_P1 Signals | e500 Core1:CCB Clock Ratio |
|---|---|---|---|
| 000 | Reserved | 100 | 2:1 |
| 001 | Reserved | 101 | 5:2 (2.5:1) |
| 010 | Reserved | 110 | 3:1 |
| 011 | 3:2 (1.5:1) | 111 | 7:2 (3.5:1) |

## 19.4 DDR/DDRCLK PLL Ratio

The dual DDR memory controller complexes can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 82 describes the clock ratio between the DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for both DDR controllers to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode.

In asynchronous mode, the DDR PLL rate to DDRCLK ratios listed in Table 82 reflects the DDR data rate to DDRCLK ratio, because the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output.

Note that the DDR PLL reference clock input, DDRCLK, is only required in asynchronous mode. MPC8572E does not support running one DDR controller in synchronous mode and the other in asynchronous mode.

**Table 82. DDR Clock Ratio**

| Binary Value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals | DDR:DDRCLK Ratio |
|---|---|
| 000 | 3:1 |
| 001 | 4:1 |
| 010 | 6:1 |
| 011 | 8:1 |
| 100 | 10:1 |
| 101 | 12:1 |
| 110 | 14:1 |
| 111 | Synchronous mode |

## 19.5 Frequency Options

### 19.5.1 Platform to Sysclk Frequency Options

Table 83 shows the expected frequency values for the platform frequency when using the specified CCB clock to SYSCLK ratio.

**Table 83. Frequency Options for Platform Frequency**

| CCB to SYSCLK Ratio | SYSCLK (MHz) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 33.33 | 41.66 | 50 | 66.66 | 83 | 100 | 111 | 133.33 |
| | Platform /CCB Frequency (MHz) | | | | | | | |
| 4 | | | | | | 400 | 444 | 533 |
| 5 | | | | | 415 | 500 | 555 | |
| 6 | | | | 400 | 498 | 600 | | |
| 8 | | | 400 | 533 | | | | |
| 10 | | 417 | 500 | | | | | |
| 12 | 400 | 500 | 600 | | | | | |

### 19.5.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

Section 4.4.3.6, "I/O Port Selection," in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* describes various high-speed interface configuration options. Note that the CCB clock frequency must be considered for proper operation of such interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

See Section 21.1.3.2, "Link Width," in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for PCI Express interface width details. Note that the "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

See Section 20.4, "1x/4x LP-Serial Signal Descriptions," in the *MPC8572E PowerQUICC III Integrated Host Processor Family Reference Manual* for Serial RapidIO interface width and frequency details.

# 20 Thermal

This section describes the thermal specifications of the MPC8572E.

Table 84 shows the thermal characteristics for the package, 1023 33 × 33 FC-PBGA.

The package uses a 29.6 × 29.6 mm lid that attaches to the substrate. Recommended maximum heat sink force is 10 pounds force (45 Newton).

**Table 84. Package Thermal Characteristics**

| Rating | Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction to ambient, natural convection | Single-layer (1s) | $R_{\Theta JA}$ | 15 | °C/W | 1, 2 |
| Junction to ambient, natural convection | Four-layer (2s2p) | $R_{\Theta JA}$ | 11 | °C/W | 1, 3 |
| Junction to ambient (at 200 ft./min.) | Single-layer (1s) | $R_{\Theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction to ambient (ar 200 ft./min.) | Four-layer (2s2p) | $R_{\Theta JMA}$ | 8 | °C/W | 1, 3 |
| Junction to board | — | $R_{\Theta JB}$ | 4 | °C/W | 4 |

**Table 84. Package Thermal Characteristics (continued)**

| Rating | Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction to case | — | $R_{\Theta JC}$ | 0.5 | °C/W | 5 |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1).

## 20.1 Temperature Diode

The MPC8572E has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each MPC8572E device be calibrated.

The following are the specifications of the on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

Operating range 2–300 μA

Diode leakage < 10 nA @ 125°C

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[ e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ ln\frac{I_H}{I_L} \right]$$

Where:

$I_{fw}$ = Forward current
$I_s$ = Saturation current
$V_d$ = Voltage at diode

$V_f$ = Voltage forward biased
$V_H$ = Diode voltage while $I_H$ is flowing
$V_L$ = Diode voltage while $I_L$ is flowing
$I_H$ = Larger diode bias current
$I_L$ = Smaller diode bias current
q = Charge of electron ($1.6 \times 10^{-19}$ C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant ($1.38 \times 10^{-23}$ Joules/K)
T = Temperature (Kelvins)

The ratio of $I_H$ to $I_L$ is usually selected to be 10:1. The above simplifies to the following:

$$\mathbf{V_H - V_L = 1.986 \times 10^{-4} \times nT}$$

Solving for T, the equation becomes:

$$\mathbf{nT} = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

# 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8572E.

## 21.1 System Clocking

The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 19.2, "CCB/SYSCLK PLL Ratio." The MPC8572E includes seven PLLs, with the following functions:

- Two core PLLs have ratios that are individually configurable. Each e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 19.3, "e500 Core PLL Ratio."
- The DDR complex PLL generates the clocking for the DDR controllers.
- The local bus PLL generates the clock for the local bus.
- The PLL for the SerDes1 module is used for PCI Express and Serial Rapid IO interfaces.
- The PLL for the SerDes2 module is used for the SGMII interface.

## 21.2 Power Supply Design

### 21.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}$_PLAT, $AV_{DD}$_CORE0, $AV_{DD}$_CORE1, $AV_{DD}$_DDR, $AV_{DD}$_LBIU, $AV_{DD}$_SRDS1 and $AV_{DD}$_SRDS2 respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 62, one to each of the $AV_{DD}$ pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of the 1023 FC-PBGA footprint, without the inductance of vias.

Figure 62 shows the PLL power supply filter circuits.

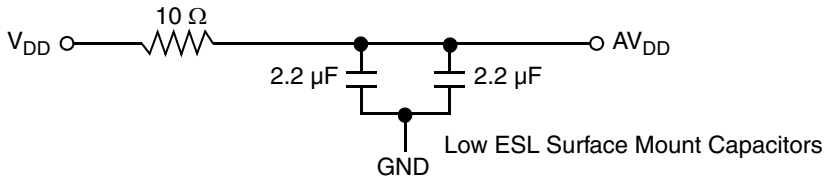


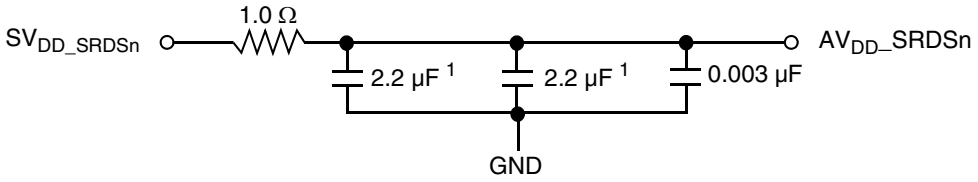

**Figure 62. PLL Power Supply Filter Circuit**

**NOTE**

It is recommended to have the minimum number of vias in the $AV_{DD}$ trace for board layout. For example, zero vias might be possible if the $AV_{DD}$ filter is placed on the component side. One via might be possible if it is placed on the opposite of the component side. Additionally, all traces for $AV_{DD}$ and the filter components should be low impedance, 10 to 15 mils wide and short. This includes traces going to GND and the supply rails they are filtering.

The $AV_{DD}$_SRDSn signal provides power for the analog portions of the SerDesn PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the $AV_{DD}$_SRDSn ball to ensure it filters out as much noise as possible. The ground connection should be near the $AV_{DD}$_SRDSn ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from

$AV_{DD}$_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.




1. An 0805 sized capacitor is recommended for system initial bring-up.

**Figure 63. SerDes PLL Power Supply Filter**

**NOTE**

$AV_{DD}$_SRDSn should be a filtered version of $SV_{DD}$_SRDS*n*.

**NOTE**

Signals on the SerDesn interface are fed from the $XV_{DD}$_SRDS*n* power plane.

## 21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8572E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each $V_{DD}$, $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ pin of the device. These decoupling capacitors should receive their power from separate $V_{DD}$, $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the $V_{DD}$, $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

## 21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes1 and SerDes2 blocks require a clean, tightly regulated source of power ($SV_{DD}$_SRDSn and $XV_{DD}$_SRDSn) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply ($SV_{DD}$_SRDSn and $XV_{DD}$_SRDSn) to the board ground plane on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

## 21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$, as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$, and GND pins of the device.

## 21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8572E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including $I^2C$ pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must NOT be pulled down during power-on reset: $\overline{\text{DMA_DACK[0:1]}}$, EC5_MDC, $\overline{\text{HRESET_REQ}}$, TRIG_OUT/READY_P0/$\overline{\text{QUIESCE}}$, MSRCID[2:4], MDVAL, and ASLEEP. The $\overline{\text{TEST_SEL}}$ pin must be set to a proper state during POR configuration. For more details, refer to the pinlist table of the individual device.

## 21.7 Output Buffer DC Impedance

The MPC8572E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for $I^2C$).

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 64). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

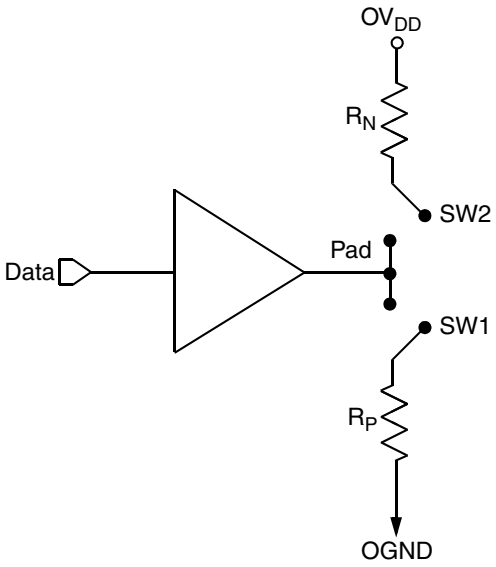



**Figure 64. Driver Impedance Measurement**

Table 85 summarizes the signal impedance targets. The driver impedances are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 85. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|
| $R_N$ | 45 Target | 18 Target (full strength mode)<br>36 Target (half strength mode) | $Z_0$ | Ω |
| $R_P$ | 45 Target | 18 Target (full strength mode)<br>36 Target (half strength mode) | $Z_0$ | Ω |

**Note:** Nominal supply voltages. See Table 1, $T_j$ = 105°C.

## 21.8 Configuration Pin Muxing

The MPC8572E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio, DDR complex PLL and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 66. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset

state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 66 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 65, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 65 is common to all known emulators.

### 21.9.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 66. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO or TCK.

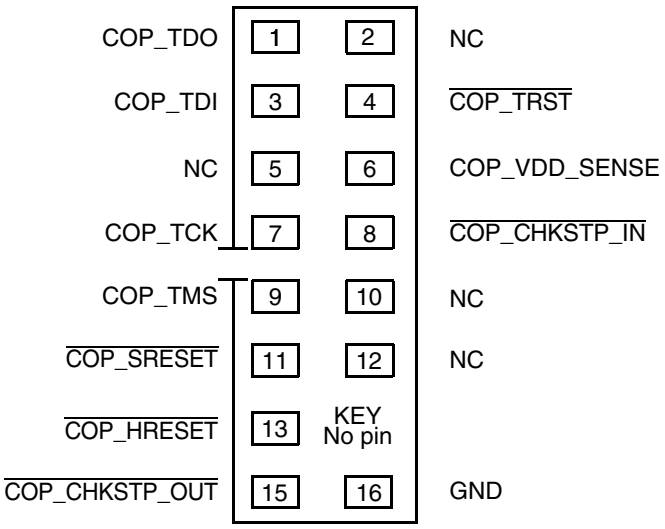
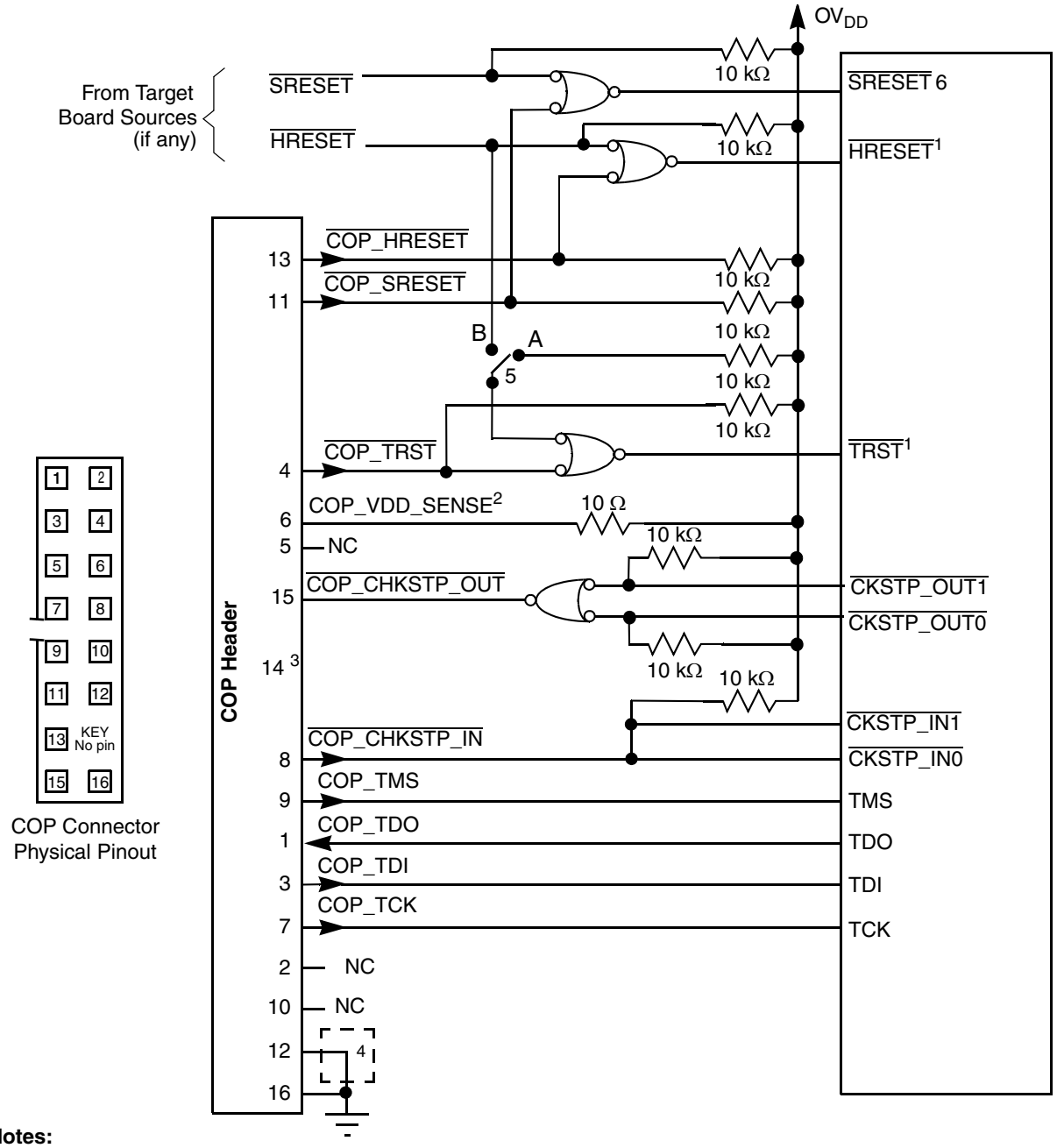



**Figure 65. COP Connector Physical Pinout**




**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 cores.

**Figure 66. JTAG Interface Connection**

## 21.10 Guidelines for High-Speed Interface Termination

### 21.10.1 SerDes 1 Interface Entirely Unused

If the high-speed SerDes 1 interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD1_TX[7:0]
- $\overline{\text{SD1_TX}}$[7:0]
- Reserved pins C24, C25, H26, H27

The following pins must be connected to XGND_SRDS1:

- SD1_RX[7:0]
- $\overline{\text{SD1_RX}}$[7:0]
- SD1_REF_CLK
- $\overline{\text{SD1_REF_CLK}}$

Pins K32 and C29 must be tied to $XV_{DD}$_SRDS1. Pins K31 and C30 must be tied to XGND_SRDS1 through a 300-Ω resistor.

The POR configuration pin cfg_srds1_en on TSEC2_TXD[5] can be used to power down SerDes 1 block for power saving. Note that both SVDD_SRDS1 and XVDD_SRDS1 must remain powered.

### 21.10.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes 1 interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:0]
- $\overline{\text{SD1_TX}}$[7:0]
- Reserved pins: C24, C25, H26, H27

The following pins must be connected to XGND_SRDS1 if not used:

- SD1_RX[7:0]
- $\overline{\text{SD1_RX}}$[7:0]

Pins K32 and C29 must be tied to $XV_{DD}$_SRDS1. Pins K31 and C30 must be tied to XGND_SRDS1 through a 300-Ω resistor.

### 21.10.3 SerDes 2 Interface (SGMII) Entirely Unused

If the high-speed SerDes 2 interface (SGMII) is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2_TX[3:0]
- $\overline{\text{SD2_TX}}$[3:0]
- Reserved pins: AF26, AF27

The following pins must be connected to XGND_SRDS2:

- SD2_RX[3:0]
- $\overline{\text{SD2_RX}}$[3:0]
- SD2_REF_CLK
- $\overline{\text{SD2_REF_CLK}}$

The POR configuration pin cfg_srds_sgmii_en on $\overline{\text{UART_RTS}}$[1] can be used to power down SerDes 2 block for power saving. Note that both SVDD_SRDS2 and XVDD_SRDS2 must remain powered.

### 21.10.4 SerDes 2 Interface (SGMII) Partly Unused

If only part of the high speed SerDes 2 interface (SGMII) pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD2_TX[3:0]
- $\overline{\text{SD2_TX}}$[3:0]
- Reserved pins: AF26, AF27

The following pins must be connected to XGND_SRDS2:

- SD2_RX[3:0]
- $\overline{\text{SD2_RX}}$[3:0]

# 22 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 22.1, "Part Numbers Fully Addressed by this Document."

## 22.1 Part Numbers Fully Addressed by this Document

Table 86 through Table 88 provide the Freescale part numbering nomenclature for the MPC8572E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

**Table 86. Part Numbering Nomenclature—Rev 2.2.1**

| MPC | *nnnn* | *e* | *t* | *l* | *pp* | *ffm* | *r* |
|---|---|---|---|---|---|---|---|
| **Product Code[1]** | **Part Identifier** | **Security Engine** | **Temperature** | **Power** | **Package Sphere Type[2]** | **Processor Frequency/ DDR Data Rate[3]** | **Silicon Revision** |
| MPC<br>PPC | 8572 | E = Included | Blank = 0 to 105°C<br>C = –40 to 105°C | Blank = Standard<br>L = Low | PX = Leaded, FC-PBGA<br>VT = Pb-free, FC-PBGA[4]<br>VJ = Fully Pb-free FC-PBGA[5] | AVN = 1500-MHz processor; 800 MT/s DDR data rate<br>AUL = 1333-MHz processor; 667 MT/s DDR data rate<br>ATL = 1200-MHz processor; 667 MT/s DDR data rate<br>ARL = 1067-MHz processor; 667 MT/s DDR data rate | E = Ver. 2.2.1 (SVR = 0x80E8_0022) SEC included |
| | | Blank = Not included | | | | | E = Ver. 2.2.1 (SVR = 0x80E0_0022) SEC not included |

**Notes:**

1 MPC stands for "Qualified."
PPC stands for "Prototype"

2 See Section 18, "Package Description," for more information on the available package types.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

4. The VT part number is ROHS-compliant with the permitted exception of the C4 die bumps.

5. The VJ part number is entirely lead-free. This includes the C4 die bumps.

**Table 87. Part Numbering Nomenclature—Rev 2.1**

| MPC | *nnnn* | *e* | *t* | *l* | *pp* | *ffm* | *r* |
|---|---|---|---|---|---|---|---|

| Product Code[1] | Part Identifier | Security Engine | Temperature | Power | Package Sphere Type[2] | Processor Frequency/ DDR Data Rate[3] | Silicon Revision |
|---|---|---|---|---|---|---|---|
| MPC<br>PPC | 8572 | E = Included | Blank = 0 to 105°C<br>C = –40 to 105°C | Blank = Standard<br>L = Low | PX = Leaded, FC-PBGA<br>VT = Pb-free, FC-PBGA | AVN = 150- MHz processor; 800 MT/s DDR data rate<br><br>AUL = 1333-MHz processor; 667 MT/s DDR data rate<br><br>ATL = 1200-MHz processor; 667 MT/s DDR data rate<br><br>ARL = 1067-MHz processor; 667 MT/s DDR data rate | D= Ver. 2.1 (SVR = 0x80E8_0021) SEC included |
| | | Blank = Not included | | | | | D= Ver. 2.1 (SVR = 0x80E0_0021) SEC not included |

**Notes:**

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

**Table 88. Part Numbering Nomenclature—Rev 1.1.1**

| MPC | *nnnn* | *e* | *t* | *pp* | *ffm* | *r* |
|---|---|---|---|---|---|---|

| Product Code[1] | Part Identifier | Security Engine | Temperature | Package Sphere Type[2] | Processor Frequency/ DDR Data Rate[3] | Silicon Revision |
|---|---|---|---|---|---|---|
| MPC<br>PPC | 8572 | E = Included | Blank=0 to 105°C<br>C= –40 to 105°C | PX = Leaded, FC-PBGA<br>VT = Pb-free, FC-PBGA | AVN = 1500-MHz processor; 800 MT/s DDR data rate<br>AUL = 1333-MHz process or; 667 MT/s DDR datarate<br>ATL = 1200-MHz processor; 667 MT/s DDR data rate<br>ARL = 1067-MHz processor; 667 MT/s DDR data rate | B = Ver. 1.1.1 (SVR = 0x80E8_0011) SEC included |
| | | Blank = Not included | | | | B = Ver. 1.1.1 (SVR = 0x80E0_0011) SEC not included |

**Notes:**

1 MPC stands for “Qualified.”
PPC stands for “Prototype”

2 See Section 18, “Package Description,” for more information on the available package types.

[3] Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

## 22.2 Part Marking

Parts are marked as the example shown in Figure 67.

FC-PBGA

**Notes:**
MMMMM is the 5-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

**Figure 67. Part Marking for FC-PBGA Device**

Table 89 explains line four of Figure 67.

**Table 89. Meaning of Last Line of Part Marking**

| Digit | Description |
|---|---|
| A | Assembly Site<br>E Oak Hill<br>Q KLM |
| WL | Lot number |
| YY | Year assembled |
| WW | Work week assembled |

# 23 Document Revision History

Table 90 provides a revision history for the MPC8572E hardware specification.

**Table 90. Document Revision History**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 6 | 06/2014 | • Updated Table 76, “MPC8572E Pinout Listing,” TDO signal is not driven during HRSET* assertion.<br>• In Table 86, “Part Numbering Nomenclature—Rev 2.2.1,“ added full Pb-free part code. |

**Table 90. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 5 | 01/2011 | • Editorial changes throughout<br>• Updated Table 4, “MPC8572E Power Dissipation,” to include low power product.<br>• In Section 22.1, “Part Numbers Fully Addressed by this Document,” defined PPC as “Prototype” and changed table headings to say “Package Sphere Type”.<br>• Added Table 86, “Part Numbering Nomenclature—Rev 2.2.1.” |
| 4 | 06/2010 | • In Section 18.3, “Pinout Listings,” updated Table 76 showing GPINOUT power rail as BVDD.<br>• Updated Section 14.1, “GPIO DC Electrical Characteristics.” |
| 3 | 03/2010 | • In Section 2.1, “Overall DC Electrical Characteristics,” changed GPIO power from OVDD to BVDD.<br>• In Section 22.1, “Part Numbers Fully Addressed by this Document,” added Table 87 for Rev 2.1 silicon.<br>• In Section 22.1, “Part Numbers Fully Addressed by this Document,” updated Table 88 for Rev 1.1.1 silicon. |
| 2 | 06/2009 | • In Section 3, “Power Characteristics,” updated CCB Max to 533MHz for 1200MHz core device in Table 5, “MPC8572EL Power Dissipation.”<br>• In Section 4.4, “DDR Clock Timing,” changed DDRCLK Max to 100MHz. This change was announced in Product Bulletin #13572.<br>• Clarified restrictions in Section 4.5, “Platform to eTSEC FIFO Restrictions.”<br>• In Table 9, “RESET Initialization Timing Specifications,” added note 2.<br>• Added Section 14, “GPIO.”<br>• In Section 18.1, “Package Parameters for the MPC8572E FC-PBGA,” updated material composition to 63% Sn, 37% Pb.<br>• In Section 18.2, “Mechanical Dimensions of the MPC8572E FC-PBGA, updated Figure 61 to correct the package thickness and top view.<br>• In Section 19.1, “Clock Ranges,” updated CCB Max to 533MHz for 1200MHz core device in Table 77, “MPC8572E Processor Core Clocking Specifications.”<br>• In Section 19.5.2, “Minimum Platform Frequency Requirements for High-Speed Interfaces,” changed minimum CCB clock frequency for proper PCI Express operation.<br>• Added LPBSE to description of LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE/LFRB signal in Table 76, “MPC8572E Pinout Listing.”<br>• Corrected supply voltage for GPIO pins in Table 76, “MPC8572E Pinout Listing.”<br>• Applied note to SD1_PLL_TPA in Table 76, “MPC8572E Pinout Listing.”<br>• Updated note regarding MDIC in Table 76, “MPC8572E Pinout Listing.”<br>• Added note for LAD pins in Table 76, “MPC8572E Pinout Listing.”<br>• Updated Table 88, “,Part Numbering Nomenclature—Rev 1.1.1” with Rev 2.0 and Rev 2.1 part number information. Added note indicating that silicon version 2.0 is available for prototype purposes only and will not be available as a qualified device. |
| 1 | 08/2008 | • In Section 22.1, “Part Numbers Fully Addressed by this Document,” added SVR information in, Table 88 “Part Numbering Nomenclature—Rev 1.1.1,” for devices without Security Engine feature. |
| 0 | 07/2008 | • Initial release. |

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Document Number: MPC8572EEC
Rev. 6
06/2014