

Automotive-grade N-channel 200 V, 0.066 Ω typ., 30 A, STripFET™ Power MOSFET in D²PAK package

Datasheet - production data

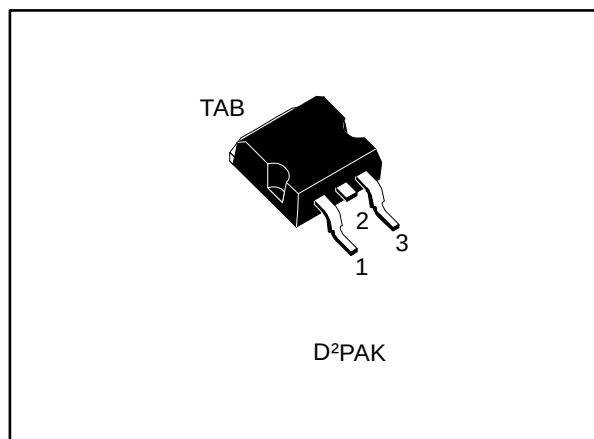
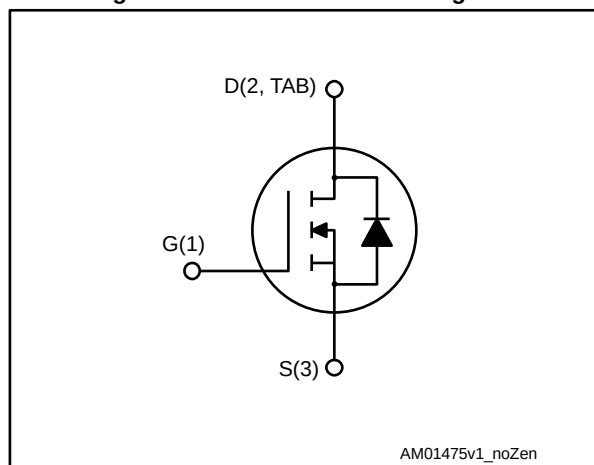


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB30NF20L	200 V	0.075 Ω	30 A	150 W

- AEC-Q101 qualified
- Gate charge minimized
- 100% avalanche tested
- Excellent FoM (figure of merit)
- Very low intrinsic capacitance



Applications

- Switching applications

Description

This N-channel enhancement mode Power MOSFET benefits from the latest refinement of STMicroelectronics' unique "single feature size" strip-based process, which decreases the critical alignment steps to offer exceptional manufacturing reproducibility. The result is a transistor with extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

Table 1: Device summary

Order code	Marking	Package	Packaging
STB30NF20L	30NF20L	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	200	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	30	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	19	A
$I_{DM}^{(1)}$	Drain current (pulsed)	120	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	150	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
T_{stg}	Storage temperature range	- 55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width is limited by safe operating area.

⁽²⁾ $I_{SD} \leq 30\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	1	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance junction-ambient	62.5	$^{\circ}\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax.}$)	30	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	140	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	200			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 200 V			1	μA
		V _{GS} = 0 V, V _{DS} = 200 V, T _C = 125 °C ⁽¹⁾			10	μA
I _{GSS}	Gate source leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±100	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	2	3	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 5 V, I _D = 15 A		0.066	0.075	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	1990	-	pF
C _{oss}	Output capacitance		-	297	-	pF
C _{rss}	Reverse transfer capacitance		-	42	-	pF
Q _g	Total gate charge	V _{DD} = 160 V, I _D = 30 A, V _{GS} = 0 to 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	65	-	nC
Q _{gs}	Gate-source charge		-	7	-	nC
Q _{gd}	Gate-drain charge		-	21	-	nC

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 100\text{ V}$, $I_D = 15\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	14	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	68	-	ns
t_f	Fall time		-	14	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	$V_{SD} = 1.5\text{ V}$	-		30	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		120	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 30\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 30\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	140		ns
Q_{rr}	Reverse recovery charge		-	0.75		μC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	$I_{SD} = 30\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	170		ns
Q_{rr}	Reverse recovery charge		-	1.1		μC
I_{RRM}	Reverse recovery current		-	14		A

Notes:

⁽¹⁾Pulse width is limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

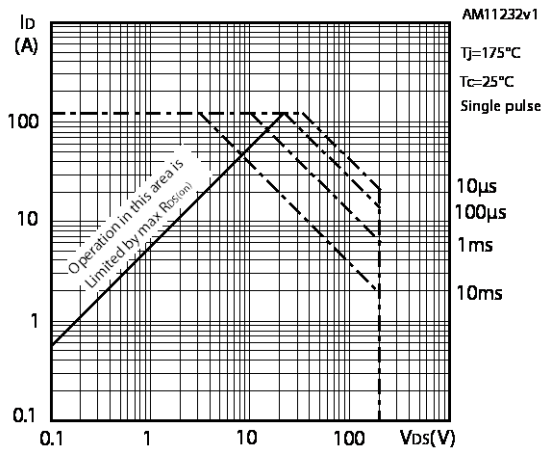


Figure 3: Thermal impedance

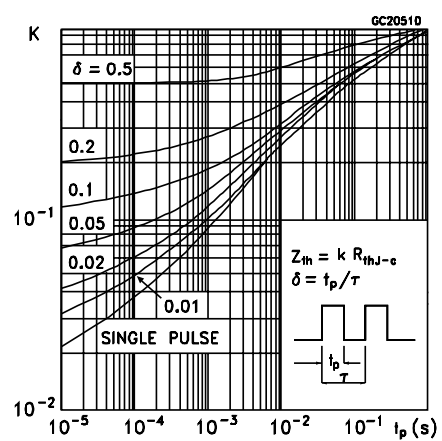


Figure 4: Output characteristics

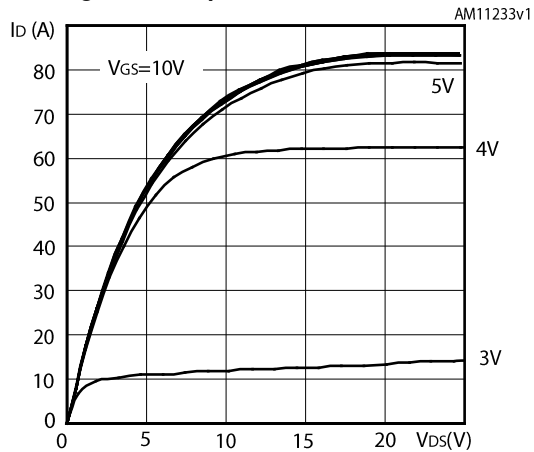


Figure 5: Transfer characteristics

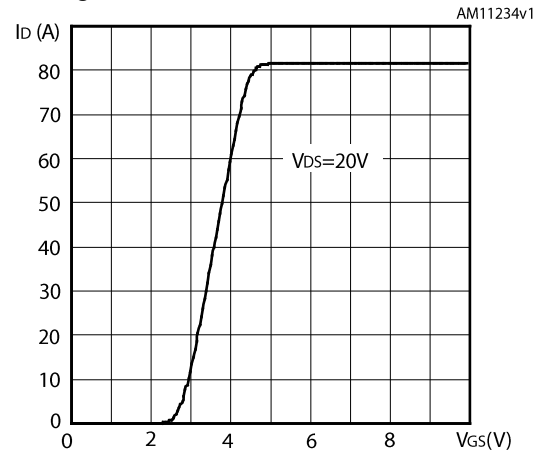
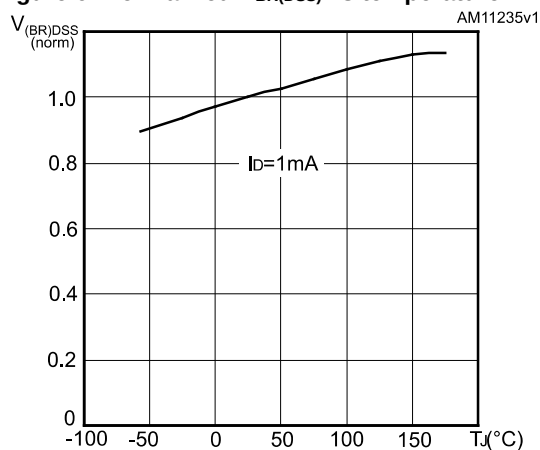
Figure 6: Normalized $V_{BR(DSS)}$ vs temperature

Figure 7: Static drain-source on-resistance

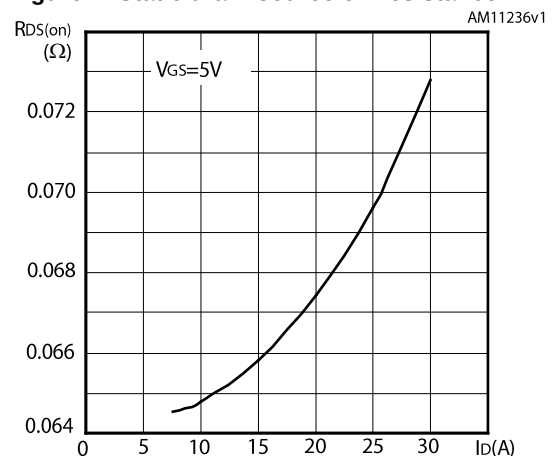


Figure 8: Gate charge vs gate-source voltage

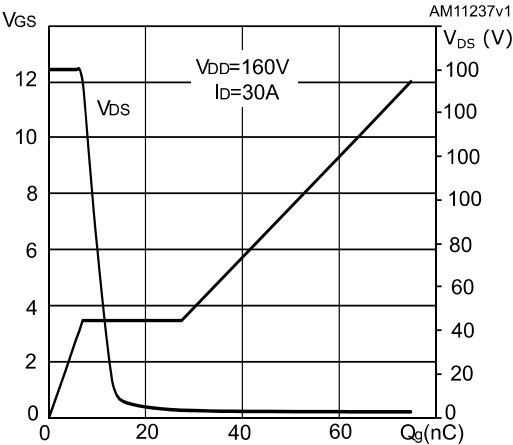


Figure 9: Capacitance variations

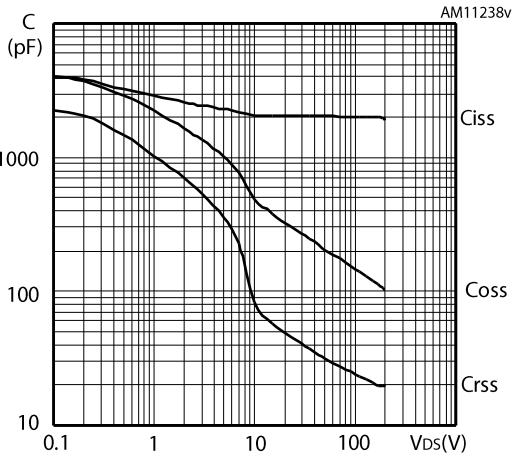


Figure 10: Normalized gate threshold voltage vs temperature

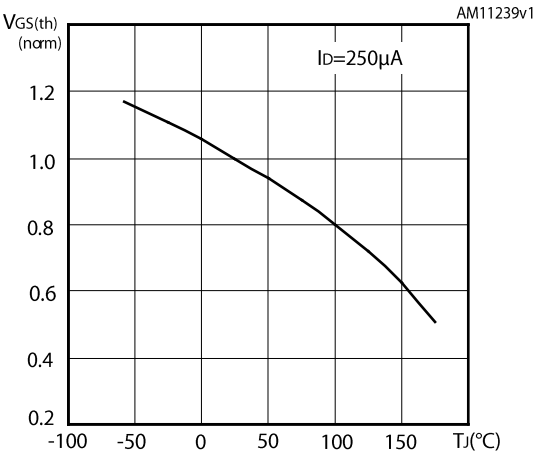


Figure 11: Normalized on-resistance vs temperature

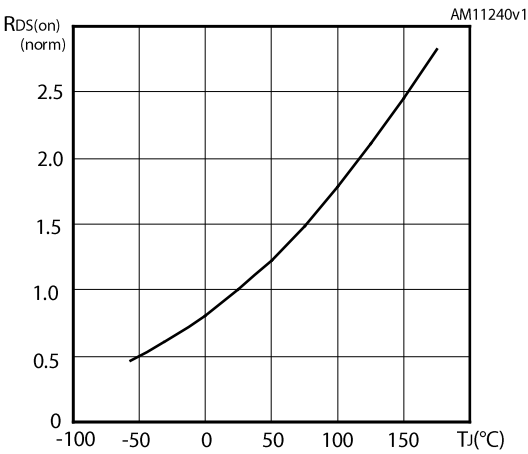
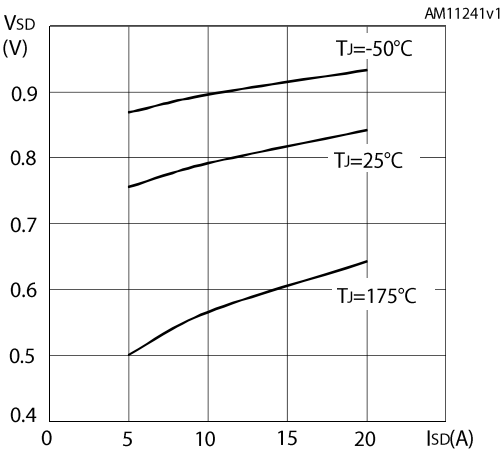
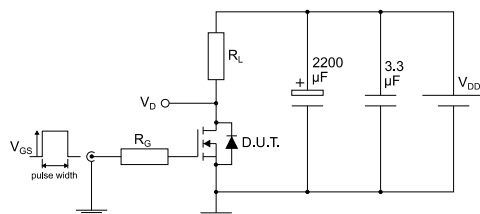


Figure 12: Source-drain diode forward characteristics



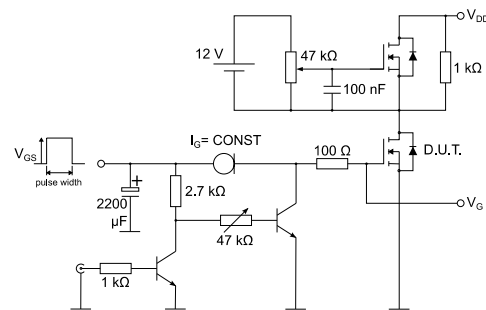
3 Test circuits

Figure 13: Test circuit for resistive load switching times



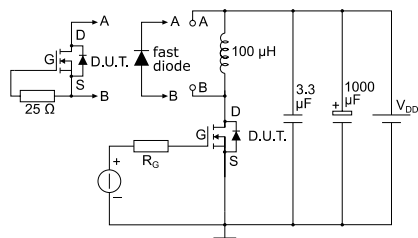
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Figure 14: Test circuit for gate charge behavior



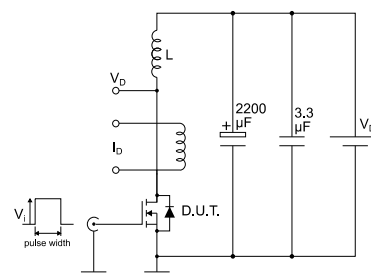
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Figure 15: Test circuit for inductive load switching and diode recovery times



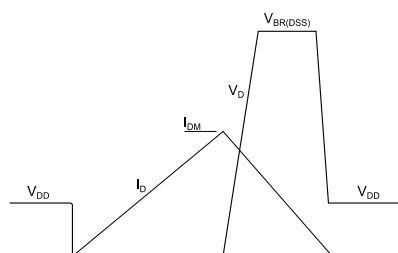
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Figure 16: Unclamped inductive load test circuit



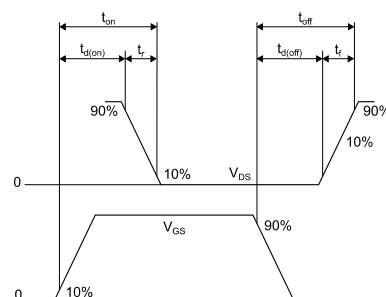
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK package information

Figure 19: D²PAK (TO-263) type A package outline

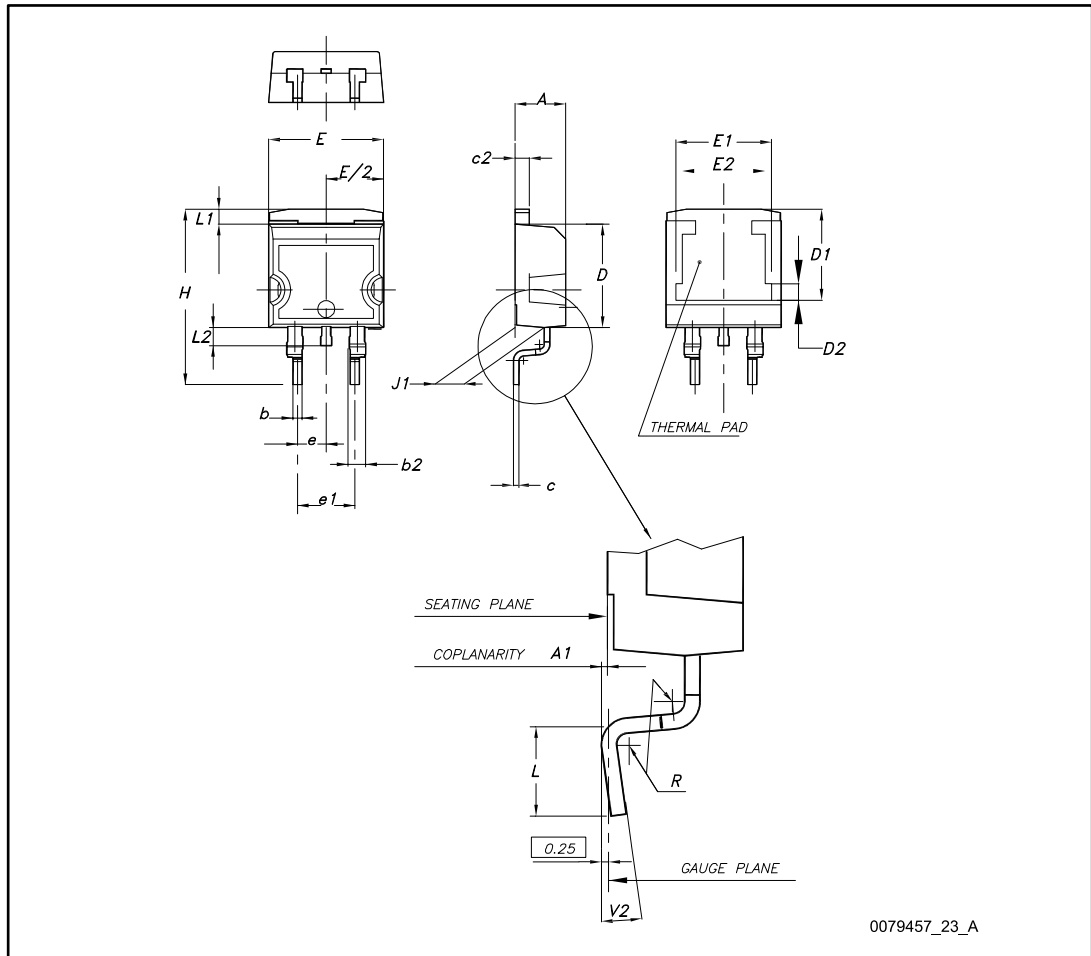
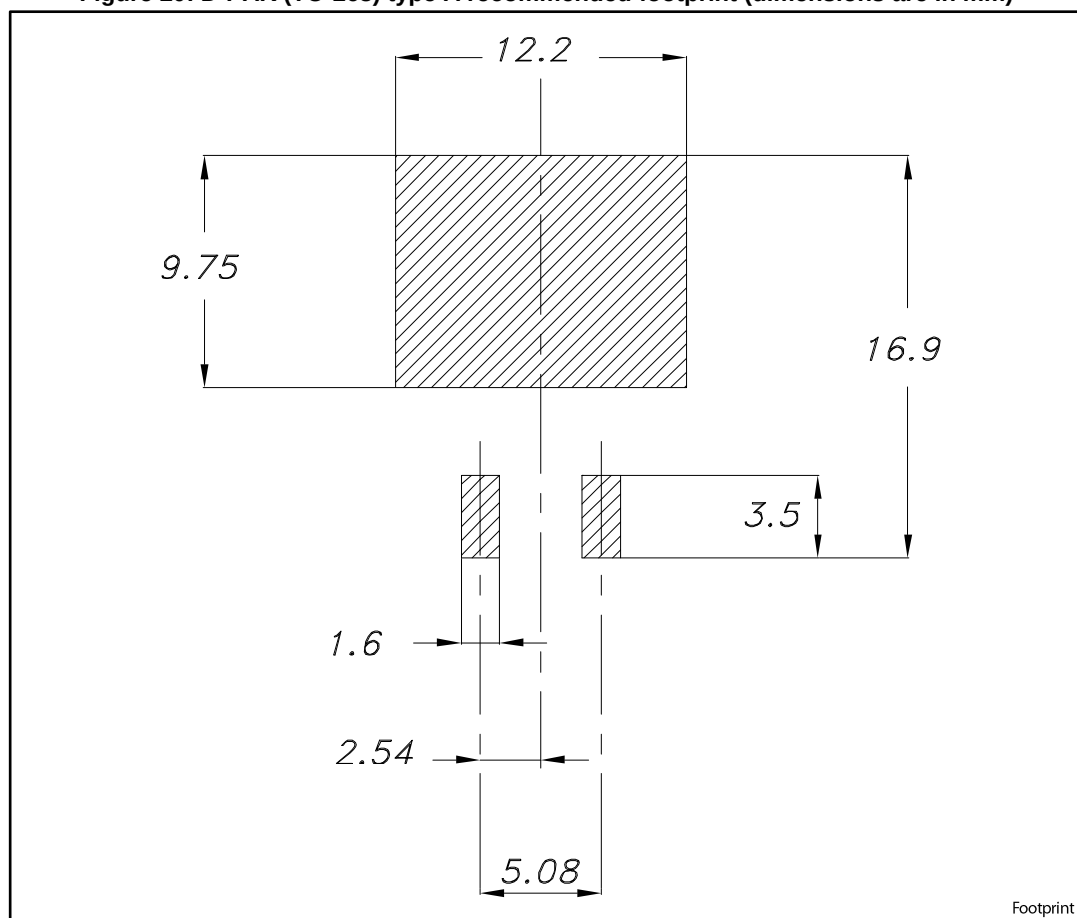


Table 9: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 20: D²PAK (TO-263) type A recommended footprint (dimensions are in mm)

4.2 D²PAK packing information

Figure 21: D²PAK type A tape outline

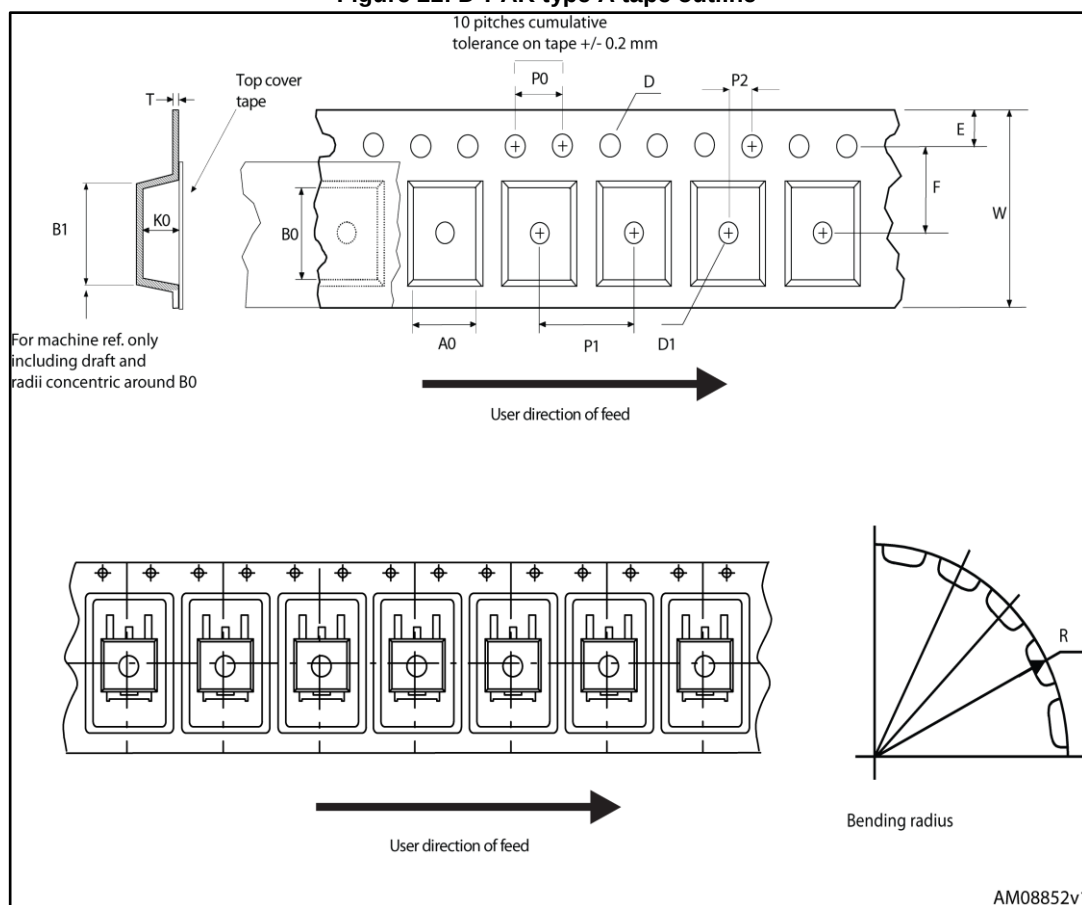
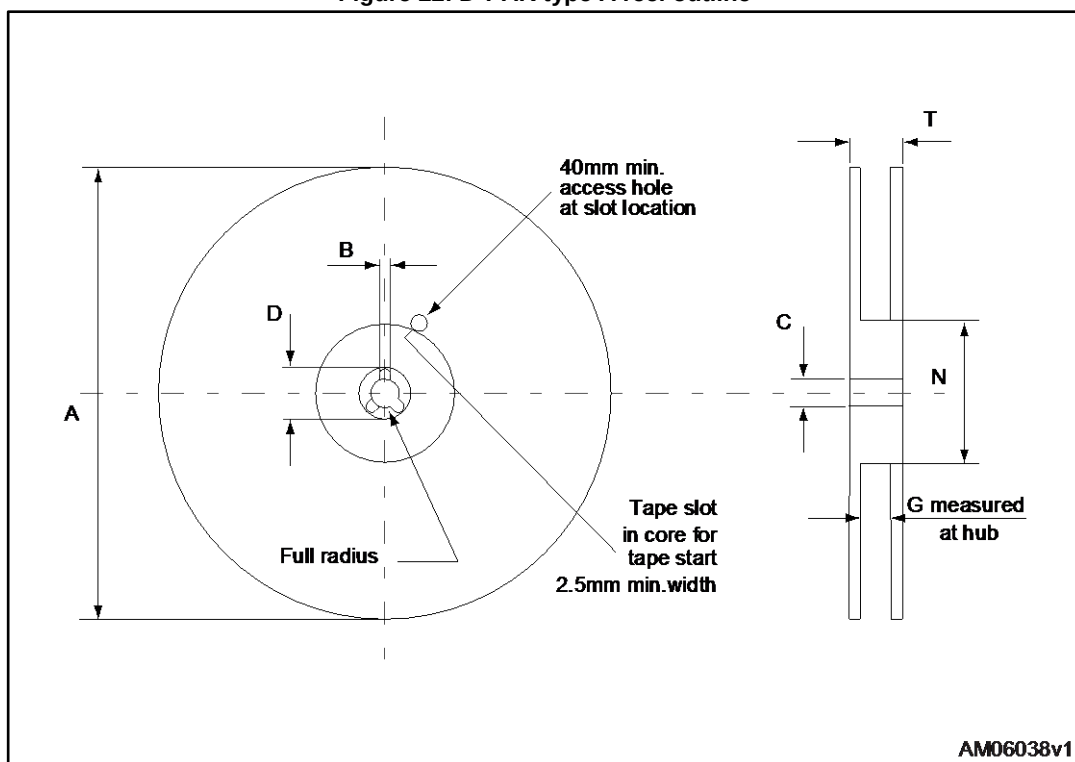


Figure 22: D²PAK type A reel outlineTable 10: D²PAK type A tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
01-Feb-2012	1	First release
07-Mar-2012	2	P _{TOT} in cover page and in <i>Table 2</i> has been updated. <i>Figure 2</i> , <i>Figure 6</i> , <i>Figure 10</i> and <i>Figure 11</i> have been updated.
02-Mar-2017	3	Updated title and features on cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 5: "On/off states"</i> and <i>Figure 3: "Thermal impedance"</i> . Minor text changes

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