

TC7WH245FU

(UNDER DEVELOPMENT)

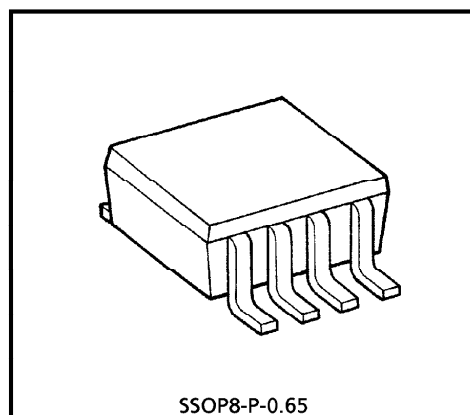
DUAL BUS TRANSCEIVER

The TC7WH245FU is an advanced high speed CMOS DUAL BUS TRANSCEIVER fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input (\bar{G}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.



SSOP8-P-0.65

Weight : 0.02g (Typ.)

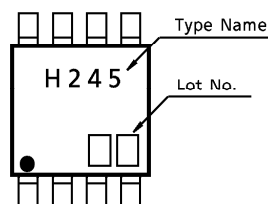
FEATURES

- High Speed $t_{pd} = 4.0ns$ (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation $I_{CC} = 4\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Balanced Propagation Delays $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC} (opr) = 2 \sim 5.5V$
- Low Noise $V_{OLP} = 0.8V$ (Max.)

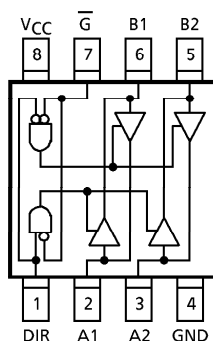
APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.
- 3) A parasitic diode is formed between the bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

MARKING



PIN ASSIGNMENT (TOP VIEW)



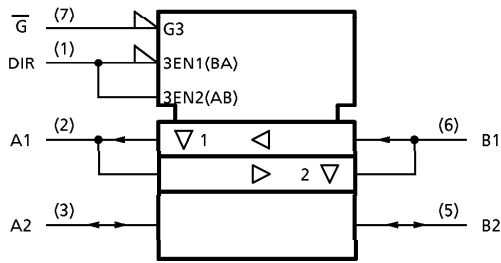
961001EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V _{CC}	− 0.5~7.0	V
DC Input Voltage	V _{IN}	− 0.5~7.0	V
DC Output Voltage	V _{OUT}	− 0.5~V _{CC} + 0.5	V
Input Diode Current	I _{IK}	− 20	mA
Output Diode Current	I _{OK}	± 20	mA
DC Output Current	I _{OUT}	± 25	mA
DC V _{CC} / Ground Current	I _{CC}	± 50	mA
Power Dissipation	P _D	300	mW
Storage Temperature	T _{stg}	− 65~150	°C
Lead Temperature (10 s)	T _L	260	°C

LOGIC DIAGRAM



TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
\overline{G}	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	x	High impedance		Z

x : Don't care
Z : High impedance

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	2.0~5.5	V
Input Voltage	V _{IN}	0~5.5	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	− 40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V _{CC} = 3.3 ± 0.3V)	ns / V
		0~20 (V _{CC} = 5 ± 0.5V)	

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = - 40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0~5.5	V _{CC} × 0.7	—	—	V _{CC} × 0.7	—	
Low-Level Input Voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	V _{CC} × 0.3	—	V _{CC} × 0.3	
High-Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = - 4mA	3.0	2.58	—	—	2.48	—	
			I _{OH} = - 8mA	4.5	3.94	—	—	3.80	—	
Low-Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I _{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3-State Output Off-State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	± 0.25	—	± 2.5	μA
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	C _L (pF)	MIN.	TYP.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	5.8	8.4	ns
				50	—	8.3	11.9	
			5.0 ± 0.5	15	—	4.0	5.5	
				50	—	5.5	7.5	
3-State Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1\text{k}\Omega$	3.3 ± 0.3	15	—	8.5	13.2	ns
				50	—	11.0	16.7	
			5.0 ± 0.5	15	—	5.8	8.5	
				50	—	7.3	10.6	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1\text{k}\Omega$	3.3 ± 0.3	50	—	11.5	15.8	ns
			5.0 ± 0.5	50	—	7.0	9.7	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	
Input Capacitance	C _{IN}	DIR, \overline{G}	—	—	—	4	10	pF
Bus Input Capacitance	C _{I/O}	An, Bn	—	—	—	8	—	pF
Power Dissipation Capacitance	C _{PD}	(Note 2)	—	—	—	21	—	pF

(Note 1) : Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

(Note 2) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Ta = 25°C, Input $t_r = t_f = 3\text{ns}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	IMIT	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.5	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	− 0.5	− 0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

INPUT EQUIVALENT CIRCUIT

