Application Note

Module name: P0340WQL … series

P0430WQL … series

Issue date: 2008/02/25

Version: 1.1

Note:

1. The information contained herein may be change without prior notice. It is therefore advisable to contact CHI MEI EL Corp before designed your product based on this specification.

Reversion History

Version	Date	Page	Description
Ver.1.0	2007/12/20	All	Application note was first issued.
Ver.1.1	2008/02/25	1	Add P0340WQCL series module.
		5	Modify section 3.1 interface definition.
		10	Add section 4.3 gamma command setting.

List of Contents

1. General Description

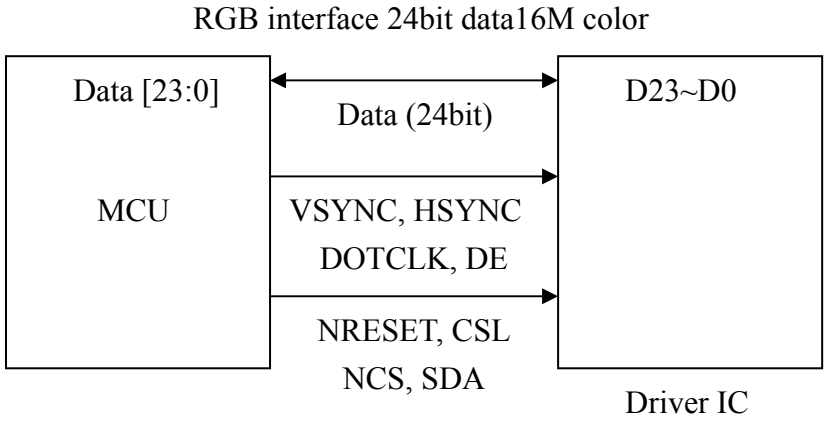
HX5116-A is a timing controller and integrated the power circuit. It can drive the 480RGBx272 graphics on LTPS AMOLED panel displays in 16,777,216 colors.

It supports Horizontal Reverse (S1 -> S160 or S160 ->S1).

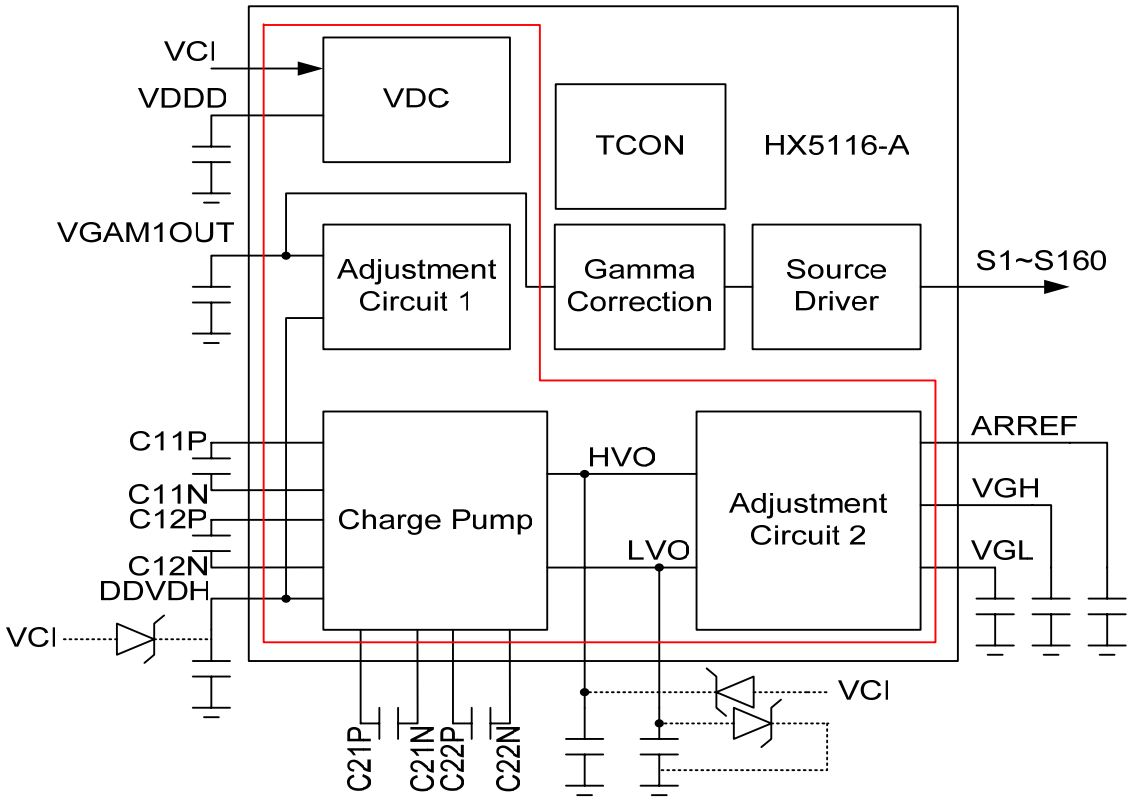
HX5116-A supports serial RGB、parallel RGB.

2. Block Diagram of system Circuit

2.1 RGB interface 24bit data 16M color

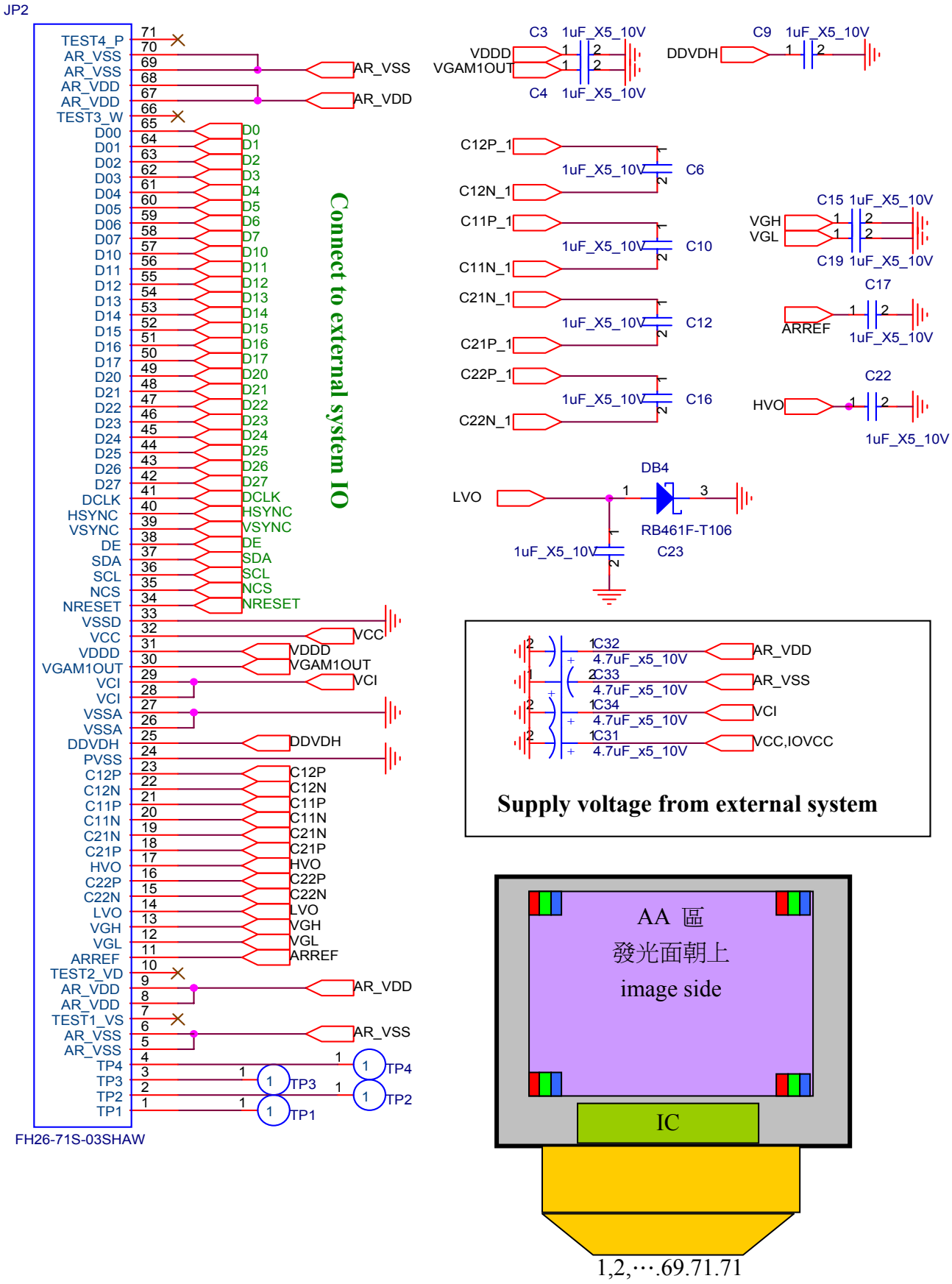


2.1 Block Diagram of Power Circuit



3. Function Description

3.1 interface definition



3.1.1 Specification

The specification of power supply circuit and pins connection are shown as following table:

3.1.1.1 Adoptability of Capacitor and PCB layout resistance.

Pins connection	Recommended voltage	Capacity	Resistance of wire (Ω)
C11P/N, C12P/N, DDVDH	10V	1 μF	< 10
VGAM1OUT	10V	1 μF	< 15
C21P/N, C22P/N	10V	1 μF	< 10
HVO, LVO	16V	1 μF	< 10
VGH, VGL,ARREF	16V	1 μF	< 15
VDDD	10V	1uF	< 10
VCI, VSSD, VSSA, VSSP	-	-	< 5

3.1.1.2 Adoptability of Schottkey diode

Pins connection	Feature
VCI – HVO, VCI – DDVDH, LVO – VSSA	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: HSC226)

Table 5.1

3.1.2 Connector

We use connector HRS FH26-71S-0.3SHW.

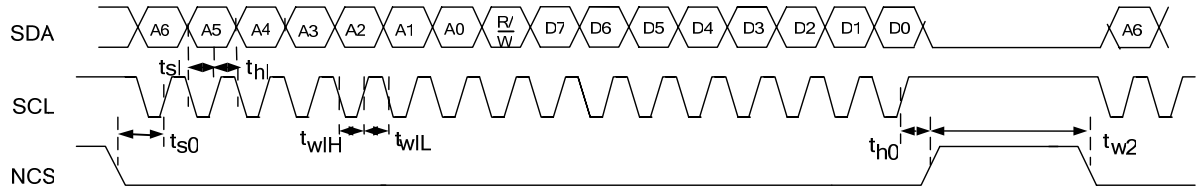
3.2 Serial Interface

The HX5116-A offers 3-wire serial interface to display initialization setting and to selecting display function.

The clock synchronized serial peripheral interface (SPI) using the chip select line (NCS), serial transfer clock line (SCL), serial input/output data (SDA). The SPI read or write is decision by R/W bit. If the R/W control bit is high, the data byte D7~D0 will be read from HX5116-A. If it is low, the data byte D7~D0 will be a write to HX5116-A.

The HX5116-A starts serial data transfer at the falling edge of NCS input and it ends serial data transfer at the rising edge of NCS input. In serial bus interface, the data is transferred with the MSB first. On write mode, it needs to input 16 valid data to SPA. Under 16 or over 16 data, HX5116-A will judge as invalid data and ignore this command.

3.2.1 Connector wire SPI Timing



3.2.2 SPI timing diagram

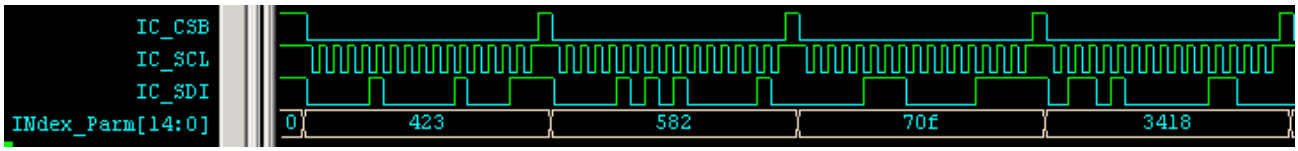
Parameter	Symbol	Min.	Typ.	Max.	Unit
Time from NCS to SCL	Ts0	40	-	-	ns
Time from SCL to NCS	Th0	60	-	-	ns
SCL low time	TwlH	-	Tcyc/2	-	ns
SCL high time	TwlL	-	Tcyc/2	-	ns
Setup time of SDI	TsI	40	-	-	ns
Hold time of SDI	ThI	40	-	-	ns
NCS high pulse width	Tw2	500			ns
Serial Clock Cycle Time	Tcyc	100	500	-	ns

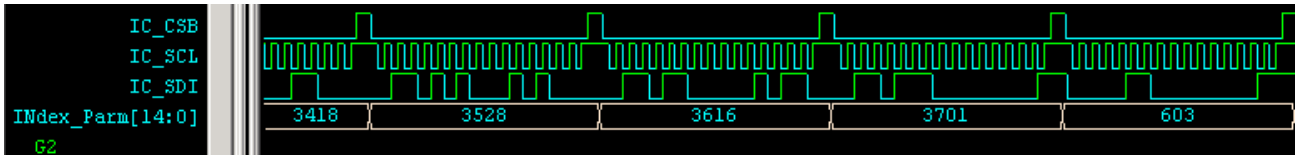
3.3 Data Interface

The HX5116-A supports 8-bit serial RGB, 24-bit parallel RGB. For digital RGB input data format, both SYNC mode and DE mode are supported. When DE mode selected, display operations is executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DCLK). The display data are transferred in pixel unit via Data bus(D27~D20、D17~D10、D07~D00) and according to the signal of data enable(DE). When SYNC mode is selected, display operation is executed in synchronization with only VSYNC, HSYNC and DCLK.

4. Display command

4.1 Display command of parallel RGB interface





Index_out(0x04); Parameter_out(0x23); //set display mode 24-bit parallel RGB (DE)
Index_out(0x05); Parameter_out(0x82); //set display mode
Index_out(0x07); Parameter_out(0x0F); //set driver capability
Index_out(0x34); Parameter_out(0x18); //set display timing
Index_out(0x35); Parameter_out(0x28); //set display timing
Index_out(0x36); Parameter_out(0x16); //set display timing
Index_out(0x37); Parameter_out(0x01); //set display timing
(Gamma command setting, sections4.3)
Index_out(0x06); Parameter_out(0x03); //set display on

4.2 Display command of serial RGB interface

Index_out(0x04); Parameter_out(0x21); //set display mode 8-bit serial RGB (DE)
Index_out(0x05); Parameter_out(0x82); //set display mode
Index_out(0x07); Parameter_out(0x0F); //set driver capability
Index_out(0x34); Parameter_out(0x48); //set display timing
Index_out(0x35); Parameter_out(0x78); //set display timing
Index_out(0x36); Parameter_out(0x42); //set display timing
Index_out(0x37); Parameter_out(0x01); //set display timing
(Gamma command setting, sections4.3)
Index_out(0x06); Parameter_out(0x03); //set display on

4.3 Gamma command setting

This is an example for gamma command setting. So the value of parameter_out maybe can't meet our standard product. The correct value of parameter_out should be referring to our final product specification.

```
Index_out(0x09);   Parameter_out(0x24); //set VGAM1OUT
Index_out(0x10);   Parameter_out(0x7A); //set R slop
Index_out(0x11);   Parameter_out(0x7D); //set G slop
Index_out(0x12);   Parameter_out(0x7A); //set B slop
Index_out(0x13);   Parameter_out(0x00); //set R_0
Index_out(0x14);   Parameter_out(0x05); //set R_10
Index_out(0x15);   Parameter_out(0x05); //set R_36
Index_out(0x16);   Parameter_out(0x03); //set R_80
Index_out(0x17);   Parameter_out(0x02); //set R_124
Index_out(0x18);   Parameter_out(0x03); //set R_168
Index_out(0x19);   Parameter_out(0x04); //set R_212
Index_out(0x1A);   Parameter_out(0x0A); //set R_255
Index_out(0x1B);   Parameter_out(0x00); //set G_0
Index_out(0x1C);   Parameter_out(0x07); //set G_10
Index_out(0x1D);   Parameter_out(0x05); //set G_36
Index_out(0x1E);   Parameter_out(0x04); //set G_80
Index_out(0x1F);   Parameter_out(0x04); //set G_124
Index_out(0x20);   Parameter_out(0x04); //set G_168
Index_out(0x21);   Parameter_out(0x05); //set G_212
Index_out(0x22);   Parameter_out(0x0B); //set G_255
Index_out(0x23);   Parameter_out(0x00); //set G_0
Index_out(0x24);   Parameter_out(0x05); //set B_10
Index_out(0x25);   Parameter_out(0x07); //set B_36
Index_out(0x26);   Parameter_out(0x05); //set B_80
Index_out(0x27);   Parameter_out(0x04); //set B_124
Index_out(0x28);   Parameter_out(0x04); //set B_168
Index_out(0x29);   Parameter_out(0x04); //set B_212
Index_out(0x2A);   Parameter_out(0x09); //set B_255
```

ARVDD=4.6V, ARVSS=-5.4V

5. Electrical Characteristic

5.1 DC Characteristics

(Unless otherwise specified, Voltage Referenced to VSS = 0V, VCC = 1.5 to 3.6V, T_A = -20 to 70C)

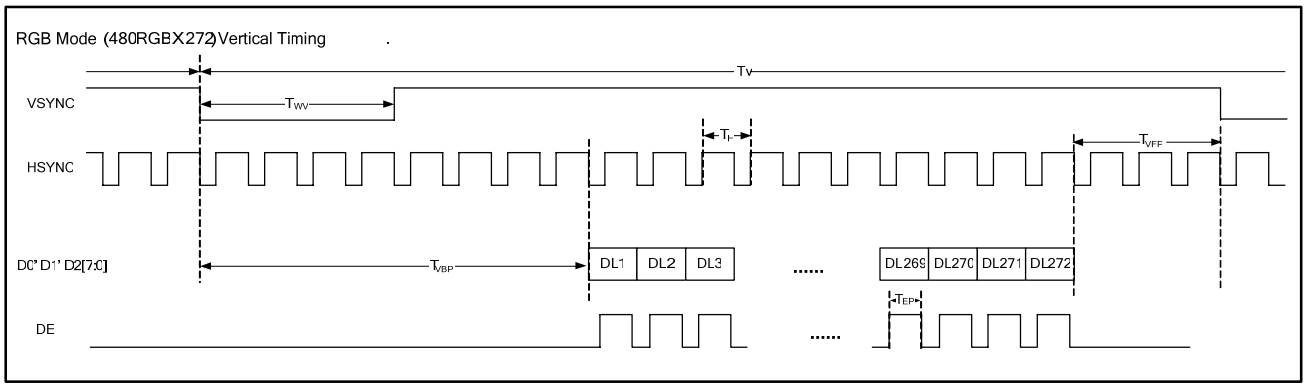
Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
System power supply pins of the logic block(VCC=IOVCC)	VCC	-	1.5	-	3.6	V
Booster Reference Supply Voltage Range	VCI	-	3.0	-	3.6	V

5.2 AC Characteristics

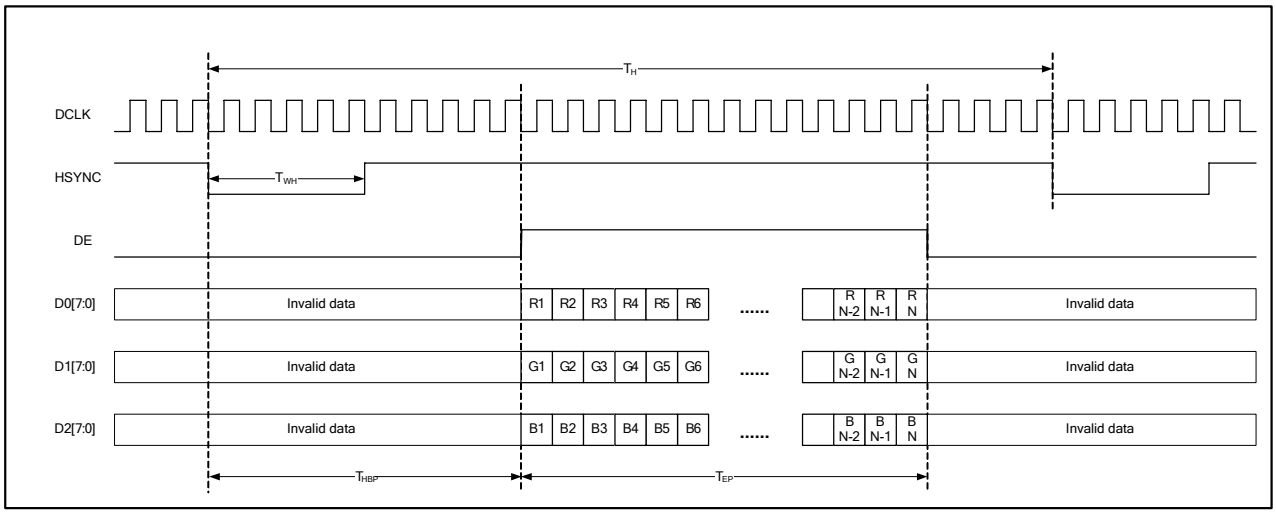
5.2.1 AC Electrical Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
HSYNC setup time	T_{hst}	10	-	-	ns
HSYNC hold time	T_{hhd}	10	-	-	ns
VSYNC setup time	T_{vst}	10	-	-	ns
VSYNC hold time	T_{vhd}	10	-	-	ns
Data setup time	T_{dsu}	10	-	-	ns
Data hold time	T_{dhd}	10	-	-	ns
DE setup time	T_{esu}	10	-	-	ns

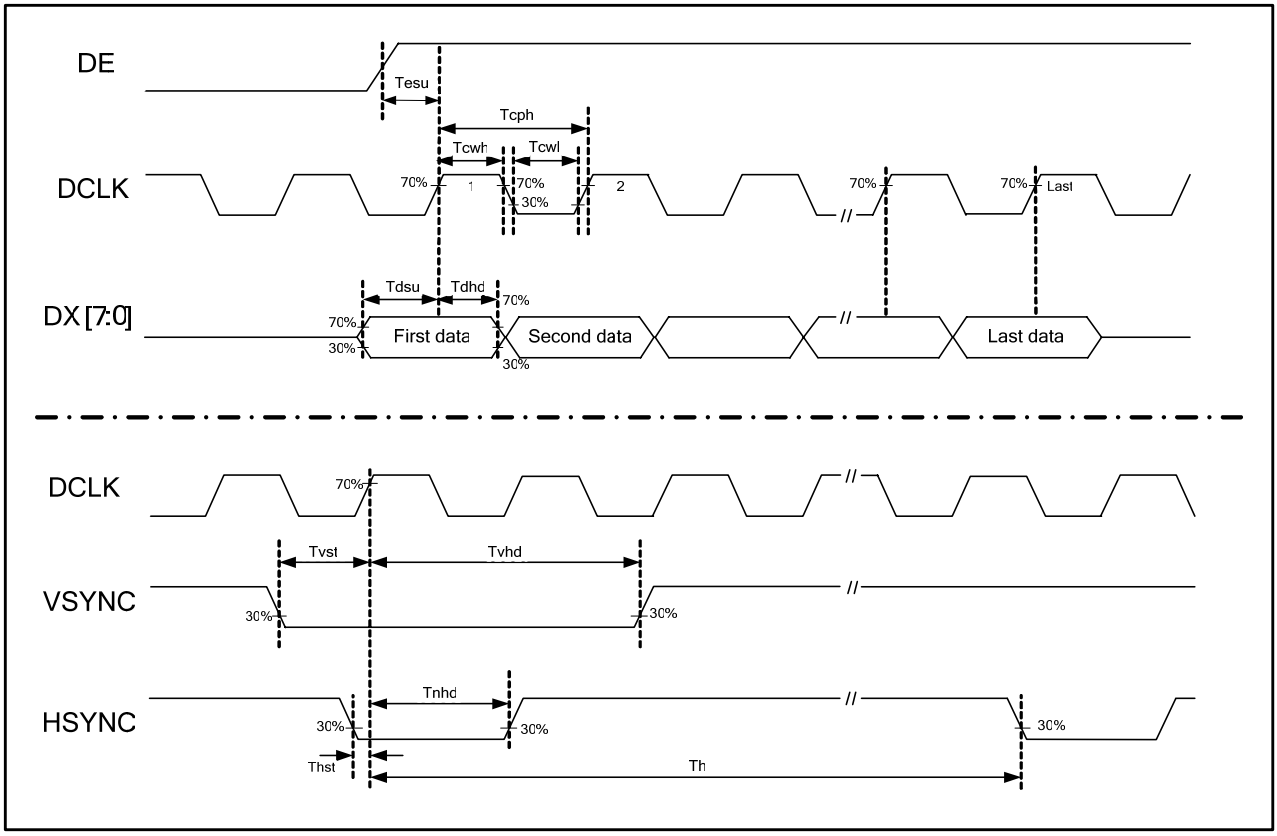
5.2.2 Parallel RGB Vertical Data Format



5.2.3 Parallel RGB Horizontal Data Format



5.2.4 Clock and Data input waveforms



5.2.4 Parallel RGB interface (480RGBx272 resolution)

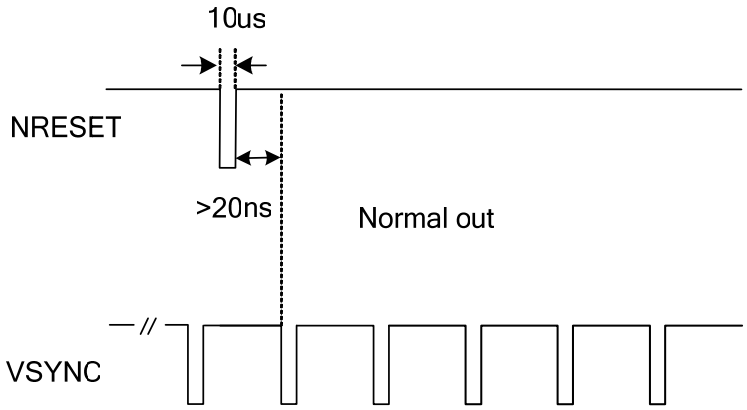
PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPh}	11.1	-	-	MHz
DCLK period	T_{CPh}	-	-	90	ns
DCLK pulse duty	T_{cwh}	40	50	60	%
HSYNC period	T_h	-	612	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	30	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	70	102	133	T_{CPH}
DE pulse width	T_{EP}	-	480	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	302	-	-	T_H

5.2.5 Serial RGB interface (480RGBx272 resolution)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	33.3	-	-	MHz
DCLK period	T_{CPH}	-	-	30	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	1836	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	90	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	274	306	337	T_{CPH}
DE pulse width	T_{EP}	-	1440	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	302	-	-	T_H

6. Reset Circuit

This block is integrated into the Interface Logic which includes Power on Reset circuitry and the hardware reset pin, NRESET. Both of these having the same reset function. Once the NRESET pin receives a negative reset pulse, all internal circuitry will start to initialize and output pin will normal operating after the next VSYNC falling edge. The NRESET minimum pulse width for completing the reset sequence is 10us.

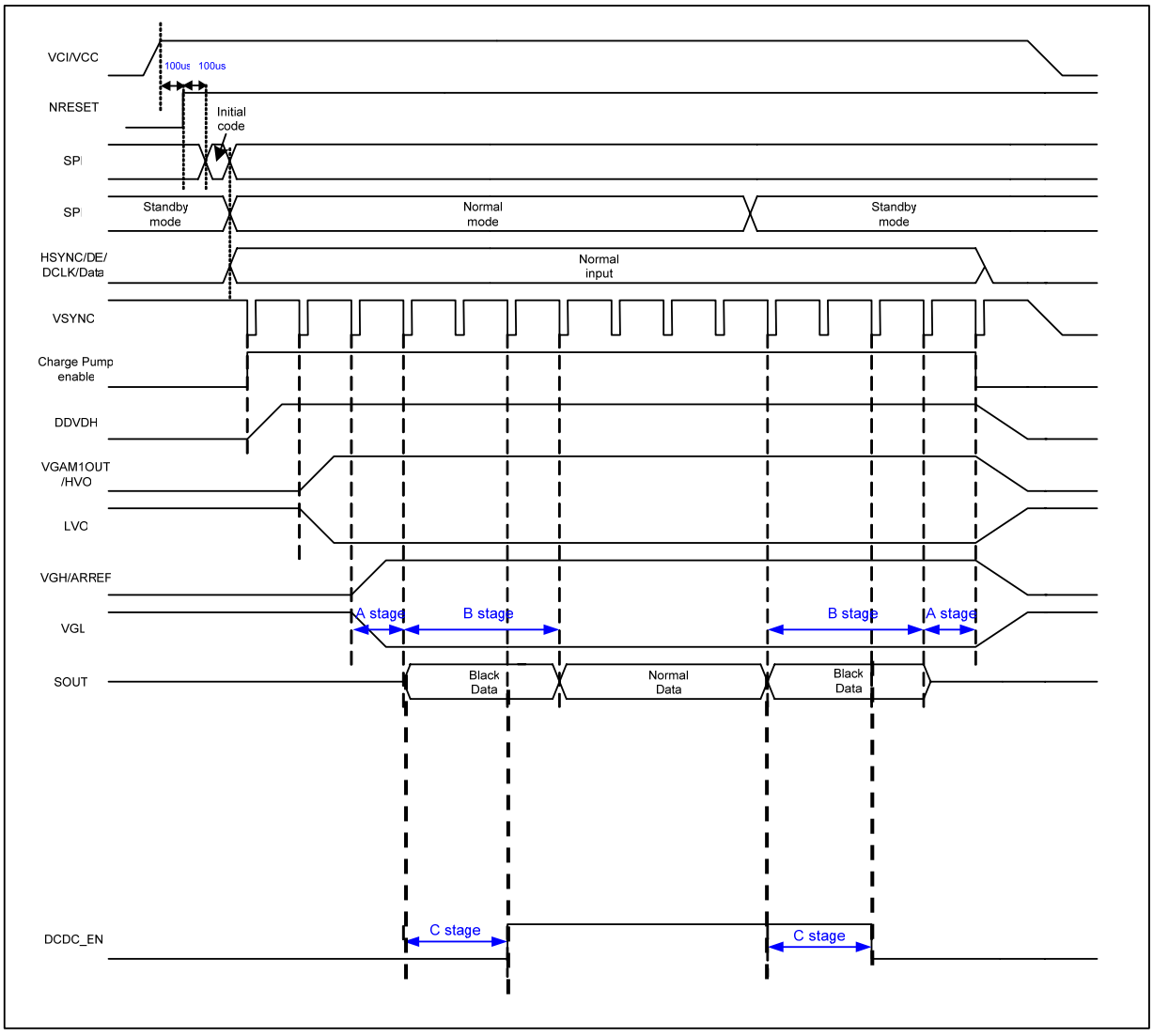


7. Power on/off Sequence

When power on/off HX5116-A, please follow the sequence:

Power ON: VCI/VCC -> NRESET -> Normal mode

Power OFF: Standby mode -> wait A+B stage -> power off VCI/VCC



8. Brightness control

TBD

9. Power IC

Application Circuit

TBD