

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

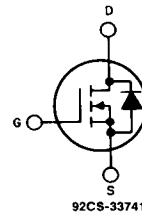
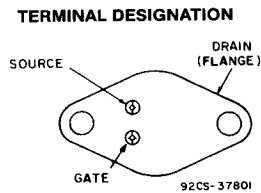
4.5A and 5.5A, 350V-400V

 $r_{DS(on)} = 1.0\ \Omega$ and $1.5\ \Omega$ **Features:**

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRF330, IRF331, IRF332 and IRF333 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

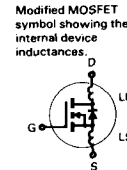
N-CHANNEL ENHANCEMENT MODE**TERMINAL DIAGRAM****JEDEC TO-204AA****Absolute Maximum Ratings**

Parameter	IRF330	IRF331	IRF332	IRF333	Units
V_{DS} Drain - Source Voltage ①	400	350	400	350	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	400	350	400	350	V
$I_D @ T_C = 25^\circ C$ Continuous Drain Current	5.5	5.5	4.5	4.5	A
$I_D @ T_C = 100^\circ C$ Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM} Pulsed Drain Current ③	22	22	18	18	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ C$ Max. Power Dissipation	75 (See Fig. 14)				W
Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\ \mu H$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				°C
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF330, IRF331, IRF332, IRF333

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	IRF330 IRF332	400	—	—	V	V _{GS} = 0V I _D = 250 μ A
	IRF331 IRF333	350	—	—	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} ; I _D = 250 μ A
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	100	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μ A	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μ A	V _{DS} = Max. Rating $\times$ 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	IRF330 IRF331	5.5	—	—	A	V _{DS} > I _{D(on)} $\times$ R _{DS(on)} max.; V _{GS} = 10V
	IRF332 IRF333	4.5	—	—	A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRF330 IRF331	—	0.8	1.0	Ω	V _{GS} = 10V, I _D = 3.0A
	IRF332 IRF333	—	1.0	1.5	Ω	
g _{fs} Forward Transconductance ②	ALL	3.0	4.0	—	S (Ω)	V _{DS} > I _{D(on)} $\times$ R _{DS(on)} max.; I _D = 3.0A
C _{iss} Input Capacitance	ALL	—	700	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	—	150	—	pF	
C _{rss} Reverse Transfer Capacitance	ALL	—	40	—	pF	V _{DD} = 175V, I _D = 3.0A, Z _o = 15 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t _{d(on)} Turn-On Delay Time	ALL	—	—	30	ns	
t _r Rise Time	ALL	—	—	35	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	—	55	ns	
t _f Fall Time	ALL	—	—	35	ns	V _{GS} = 10V, I _D = 7.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	
Q _{gs} Gate-Source Charge	ALL	—	11	17	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	7.0	11	nC	
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.



Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	1.67	°C/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF330 IRF331	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF332 IRF333	—	—	4.5	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRF330 IRF331	—	—	22	A	
	IRF332 IRF333	—	—	18	A	
V _{SD} Diode Forward Voltage ②	IRF330 IRF331	—	—	1.6	V	T _C = 25°C, I _S = 5.5A, V _{GS} = 0V
	IRF332 IRF333	—	—	1.5	V	T _C = 25°C, I _S = 4.5A, V _{GS} = 0V
t _{rr} Reverse Recovery Time	ALL	—	600	—	ns	T _J = 150°C, I _F = 5.5A, dI _F /dt = 100A/ μ s
Q _{RR} Reverse Recovered Charge	ALL	—	4.0	—	μ C	T _J = 150°C, I _F = 5.5A, dI _F /dt = 100A/ μ s
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C.② Pulse Test: Pulse width $\leq$ 300 μ s, Duty Cycle $\leq$ 2%.

③ Repetitive Rating: Pulse width limited

by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

IRF330, IRF331, IRF332, IRF333

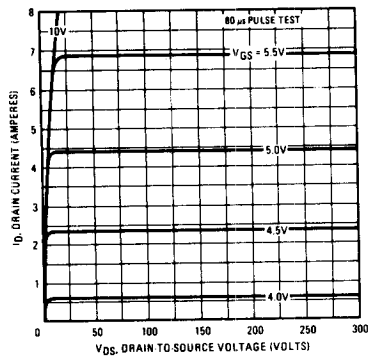


Fig. 1 – Typical Output Characteristics

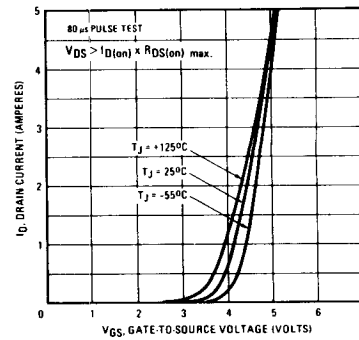


Fig. 2 – Typical Transfer Characteristics

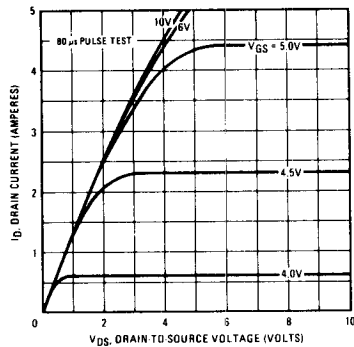


Fig. 3 – Typical Saturation Characteristics

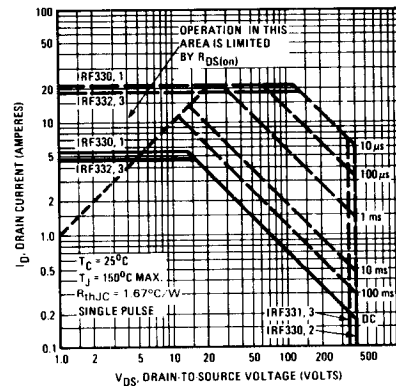


Fig. 4 – Maximum Safe Operating Area

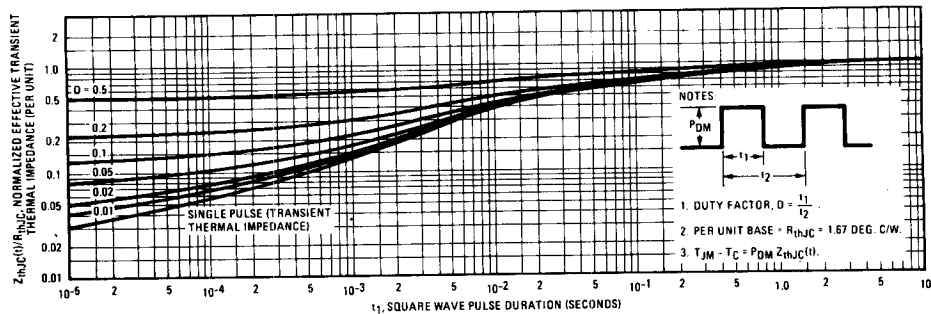


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF330, IRF331, IRF332, IRF333

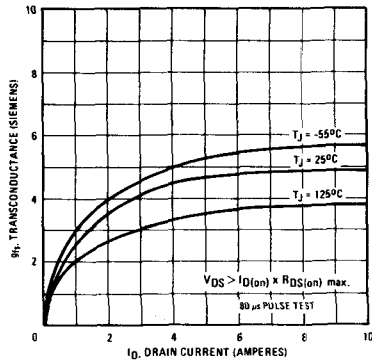


Fig. 6 - Typical Transconductance Vs. Drain Current

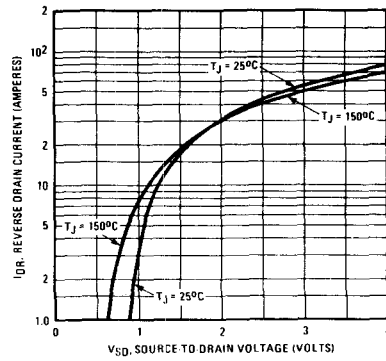


Fig. 7 - Typical Source-Drain Diode Forward Voltage

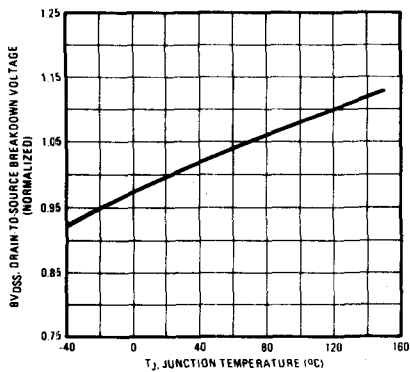


Fig. 8 - Breakdown Voltage Vs. Temperature

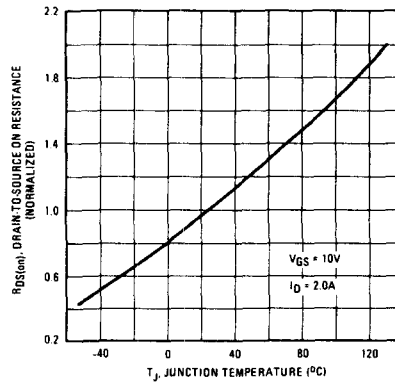


Fig. 9 - Normalized On-Resistance Vs. Temperature

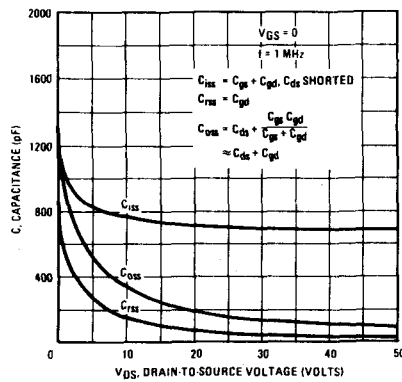


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

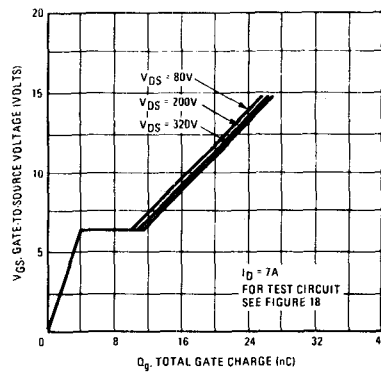


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

IRF330, IRF331, IRF332, IRF333

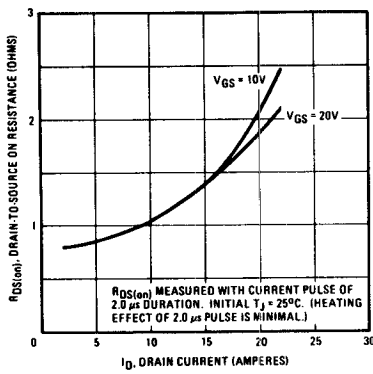


Fig. 12 - Typical On-Resistance Vs. Drain Current

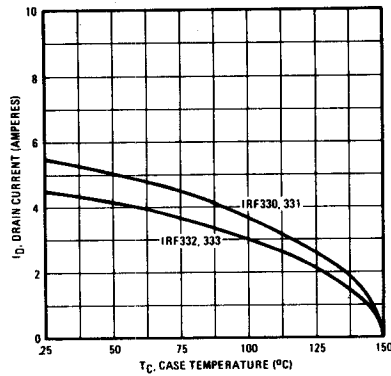


Fig. 13 - Maximum Drain Current Vs. Case Temperature

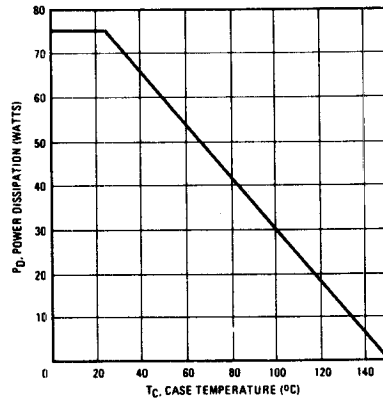


Fig. 14 - Power Vs. Temperature Derating Curve

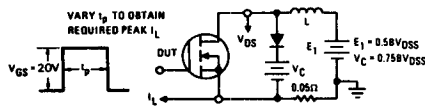


Fig. 15 - Clamped Inductive Test Circuit

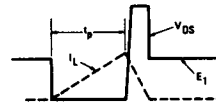


Fig. 16 - Clamped Inductive Waveforms

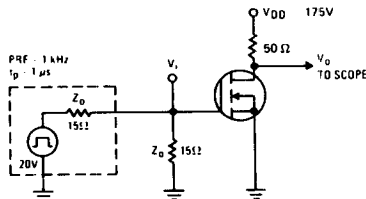


Fig. 17 - Switching Time Test Circuit

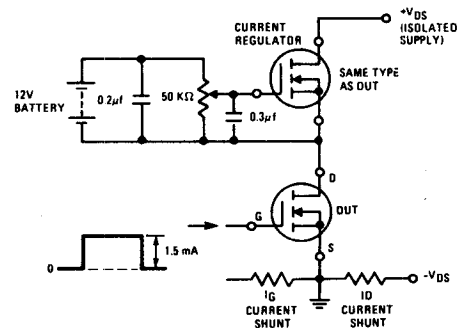


Fig. 18 - Gate Charge Test Circuit