FAIRCHILD SEMICONDUCTOR®

April 2008

# FDMS5352

## N-Channel Power Trench® MOSFET

### 60V, 49A, 6.7mΩ

### Features

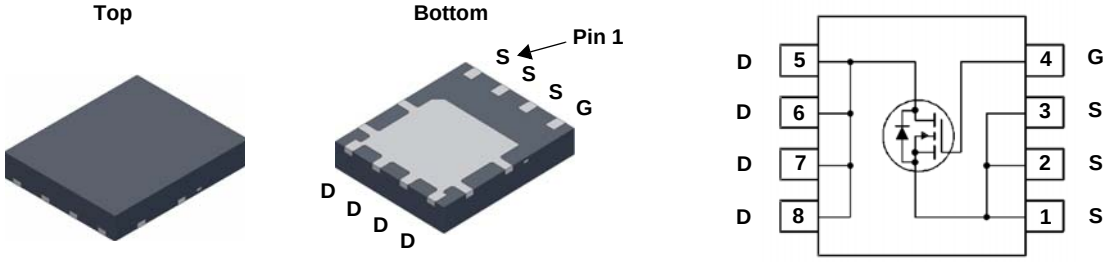
- Max $r_{DS(on)}$ = 6.7mΩ at $V_{GS}$ = 10V, $I_D$ = 13.6A
- Max $r_{DS(on)}$ = 8.2mΩ at $V_{GS}$ = 4.5V, $I_D$ = 12.3A
- Advanced Package and Silicon combination for low $r_{DS(on)}$
- MSL1 robust package design
- 100% UIL Tested
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC - DC Conversion




Power 56

## MOSFET Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 60 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current -Continuous (Package limited) | $T_C$ = 25°C | | 49 | A |
| | -Continuous (Silicon limited) | $T_C$ = 25°C | | 88 | |
| | -Continuous | $T_A$ = 25°C | (Note 1a) | 13.6 | |
| | -Pulsed | | | 100 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 600 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25°C | | 104 | W |
| | Power Dissipation | $T_A$ = 25°C | (Note 1a) | 2.5 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 1.2 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 50 | |

### Package Marking and Ordering Information

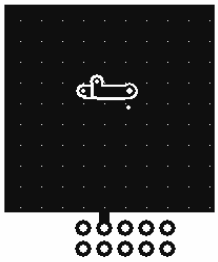
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMS5352 | FDMS5352 | Power 56 | 13" | 12mm | 3000 units |

## Electrical Characteristics $T_J$ = 25°C unless otherwise noted

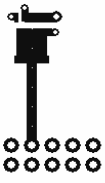
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250μA, $V_{GS}$ = 0V | 60 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250μA, referenced to 25°C | | 57 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{GS}$ = 0V, $V_{DS}$ = 48V, | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | | | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 1.0 | 1.8 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250μA, referenced to 25°C | | -6.6 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10V, $I_D$ = 13.6A | | 5.6 | 6.7 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 12.3A | | 6.7 | 8.2 | |
| | | $V_{GS}$ = 10V, $I_D$ = 13.6A, $T_J$ = 125°C | | 9.7 | 11.6 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5V, $I_D$ = 13.6A | | 76 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 30V, $V_{GS}$ = 0V, f = 1MHz | | 5220 | 6940 | pF |
| $C_{oss}$ | Output Capacitance | | | 410 | 545 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 225 | 335 | pF |
| $R_g$ | Gate Resistance | f = 1MHz | | 1.3 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 30V, $I_D$ = 13.6A, $V_{GS}$ = 10V, $R_{GEN}$ = 6Ω | | 19 | 34 | ns |
| $t_r$ | Rise Time | | | 11 | 21 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 58 | 93 | ns |
| $t_f$ | Fall Time | | | 7 | 15 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$=0Vto10V, $V_{DD}$ = 30V, $I_D$ = 13.6A | | 93 | 131 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0V to 5V, $V_{DD}$ = 30V, $I_D$ = 13.6A | | 48 | 67 | nC |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 30V, $I_D$ = 13.6A | | 14 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 30V, $I_D$ = 13.6A | | 17 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = 13.6A (Note 2) | | 0.8 | 1.3 | V |
| | | $V_{GS}$ = 0V, $I_S$ = 2.1A (Note 2) | | 0.7 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 13.6A, di/dt = 100A/μs | | 39 | 63 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 48 | 77 | nC |

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in$^2$ pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25°C, L = 3mH, $I_{AS}$ = 20A, $V_{DD}$ = 60V, $V_{GS}$ = 10V

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

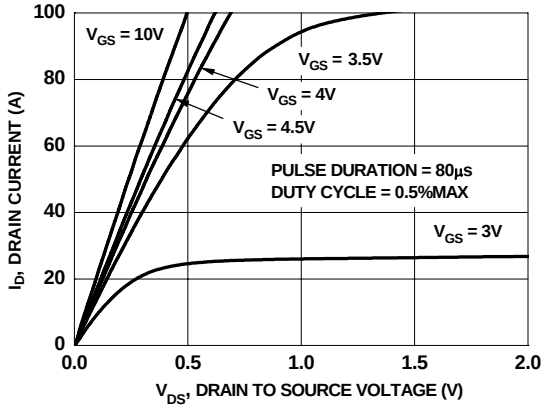



**Figure 1. On-Region Characteristics**

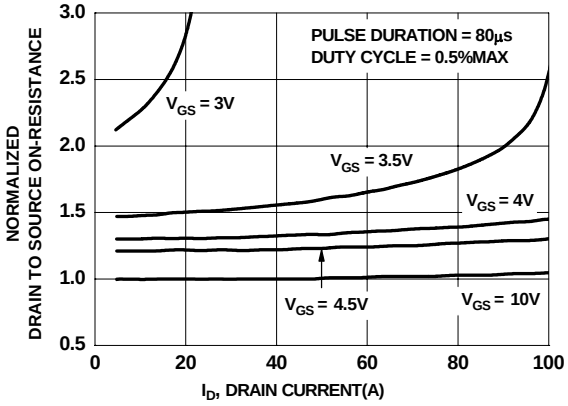



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

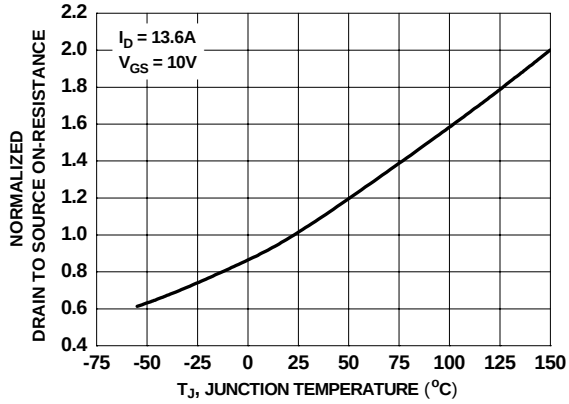



**Figure 3. Normalized On-Resistance vs Junction Temperature**

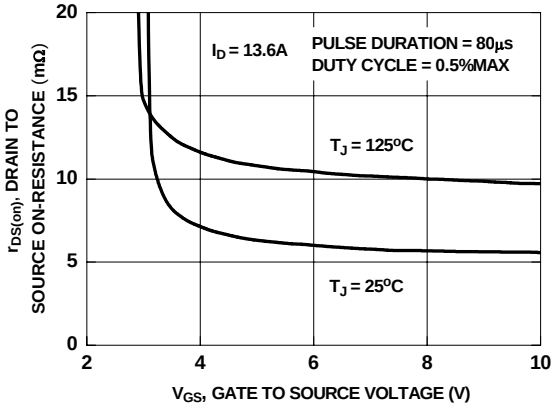



**Figure 4. On-Resistance vs Gate to Source Voltage**

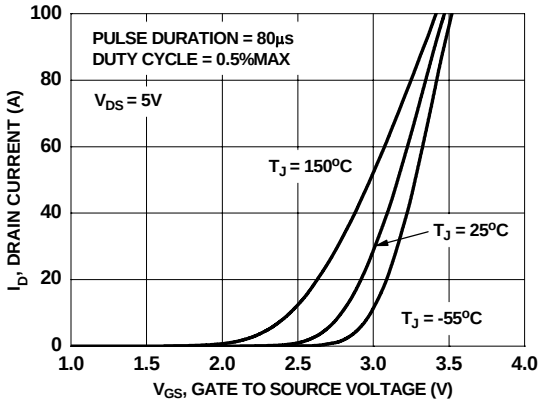



**Figure 5. Transfer Characteristics**

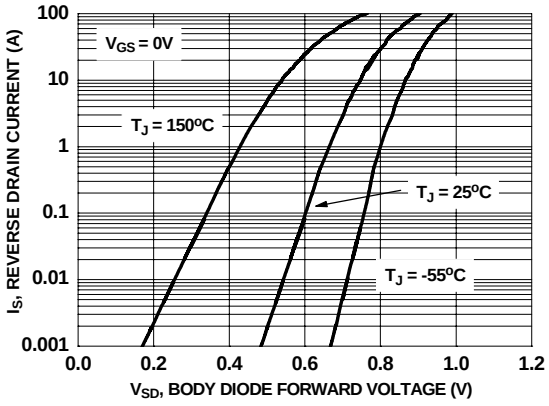



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

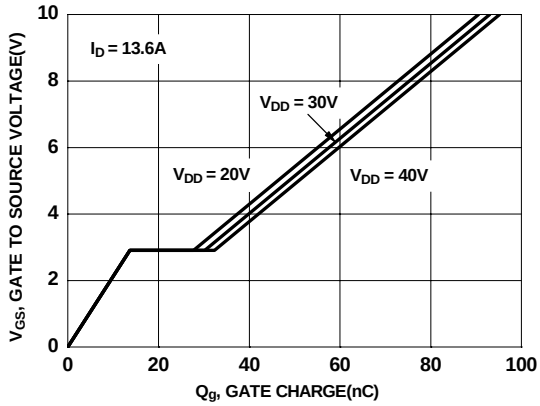



**Figure 7. Gate Charge Characteristics**

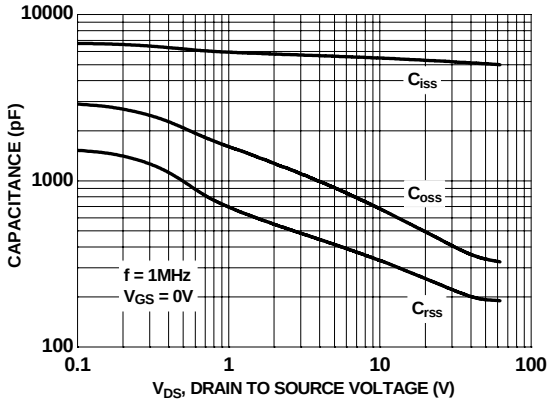



**Figure 8. Capacitance vs Drain to Source Voltage**

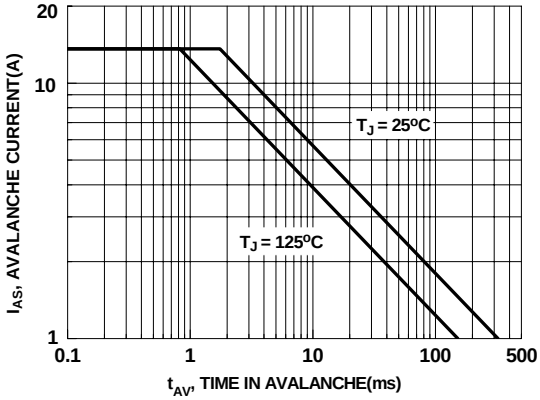



**Figure 9. Unclamped Inductive Switching Capability**

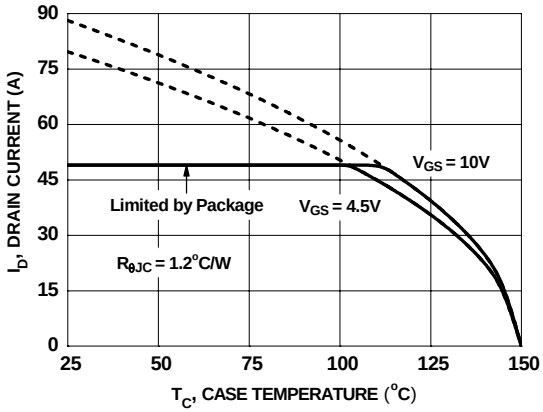



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

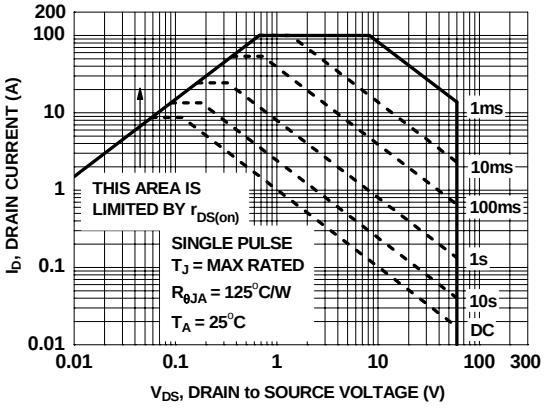



**Figure 11. Forward Bias Safe Operating Area**

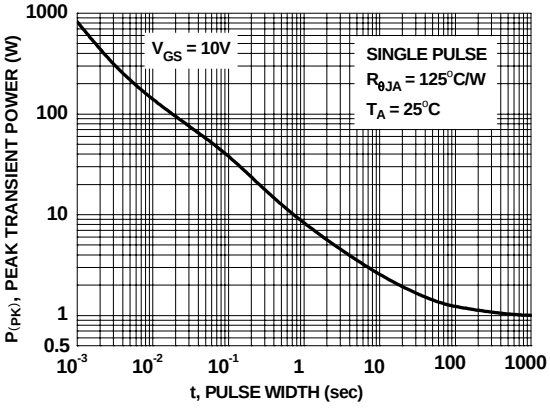



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

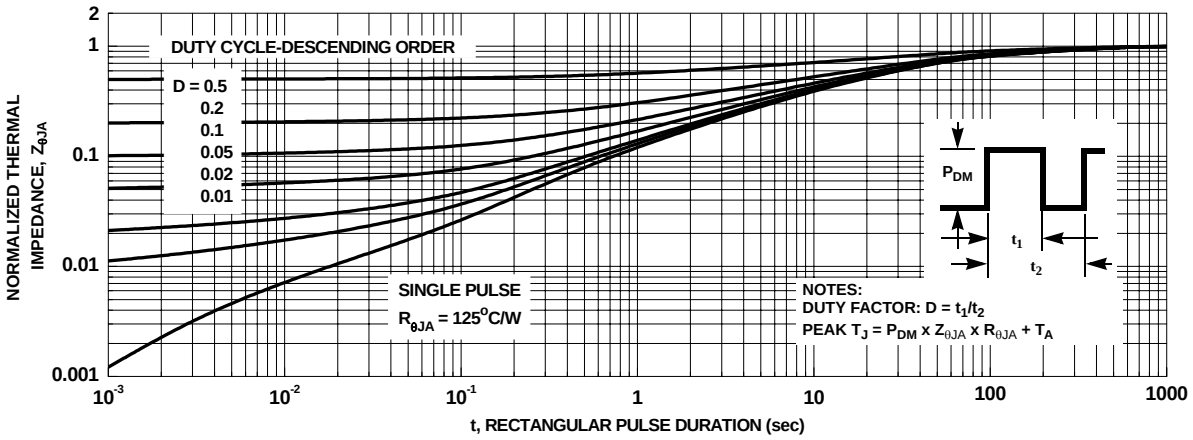
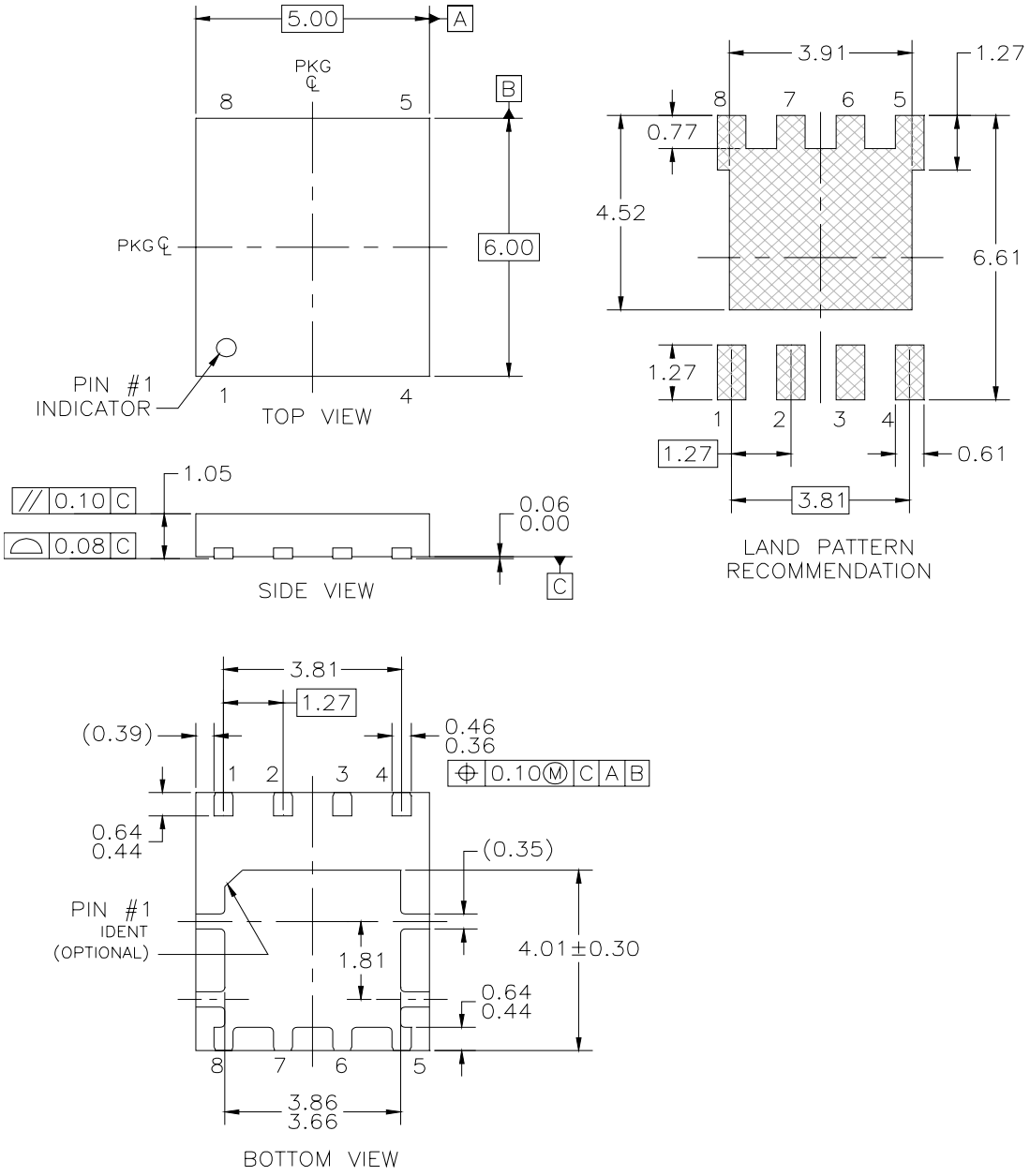



**Figure 13. Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout




NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) NO JEDEC REFERENCE AS OF FEBRUARY 2006

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994

PQFN08AREVA

FAIRCHILD SEMICONDUCTOR®

## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidianries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CorePOWER™
*CROSSVOLT*™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficentMax™
EZSWITCH™ *
™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter® *
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world 1mW at a time™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SuperMOS™
SYSTEM GENERAL ®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |

Rev. I34