Arria V Device Datasheet

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AV-51002

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Arria V GX, GT, SX, and ST Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –C4 (fastest), –C5, and –C6 speed grades. Industrial grade devices are offered in the –I3 and –I5 speed grades.

For more information about the densities and packages of devices in the Arria V family, refer to the *Arria V Device Overview*.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

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Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

Conditions outside the range listed in Table 1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1. Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	–0.50	1.43	V
V_{CCP}	Periphery circuitry, PCIe® hard IP block, and transceiver physical coding sublayer (PCS) power supply	–0.50	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.50	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.50	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.50	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO}	I/O power supply	–0.50	3.90	V
V_{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	–0.50	1.80	V
V_{CCA_FPLL}	PLL analog power supply	–0.50	3.25	V
V_{CCA_GXB}	Transceiver high voltage power	–0.50	3.25	V
V_{CCH_GXB}	Transmitter output buffer power	–0.50	1.80	V
V_{CCR_GXB}	Receiver power	–0.50	1.50	V
V_{CCT_GXB}	Transmitter power	–0.50	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.50	1.50	V
V_I	DC input voltage	–0.50	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.50	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.50	3.90	V
$V_{CCRSTCLK_HPS}$	HPS reset and clock input pins power supply	–0.50	3.90	V
V_{CCPLL_HPS}	HPS PLL analog power supply	–0.50	3.25	V
$V_{CC_AUX_SHARED}$	HPS and FPGA shared auxiliary power supply	–0.50	3.25	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (No bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 2 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Table 2. Maximum Allowed Overshoot During Transitions for Arria V Devices

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Table 3 lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 3. Recommended Operating Conditions for Arria V Devices (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCP}	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCPGM}	Configuration pins (3.3 V) power supply	—	3.135	3.3	3.465	V
	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCBAT} (1)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_{CCPD} (2)	I/O pre-driver (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.418	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C

Table 3. Recommended Operating Conditions for Arria V Devices (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
t_{RAMP} (3)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Notes to Table 3:

(1) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.

(2) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

(3) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Table 4 lists recommended operating conditions for Arria V transceiver power supplies.

Table 4. Transceiver Power Supply Operating Conditions for Arria V Devices

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_GXBL}	Transceiver high voltage power (left side)	2.375	2.500	2.625	V
V_{CCA_GXBR}	Transceiver high voltage power (right side)				
V_{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1.1/1.15 (1)	1.14/1.18	V
V_{CCR_GXBR}	GX and SX speed grades—receiver power (right side)				
V_{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1.17	1.20	1.23	V
V_{CCR_GXBR}	GT and ST speed grades—receiver power (right side)				
V_{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1.1/1.15 (1)	1.14/1.18	V
V_{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)				
V_{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1.17	1.20	1.23	V
V_{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)				
V_{CCH_GXBL}	Transmitter output buffer power (left side)	1.425	1.500	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power (right side)				
V_{CCL_GXBL}	GX and SX speed grades—clock network power (left side)	1.08/1.12	1.1/1.15 (1)	1.14/1.18	V
V_{CCL_GXBR}	GX and SX speed grades—clock network power (right side)				
V_{CCL_GXBL}	GT and ST speed grades—clock network power (left side)	1.17	1.20	1.23	V
V_{CCL_GXBR}	GT and ST speed grades—clock network power (right side)				

Note to Table 4:

(1) For data rate <=3.2 Gbps, connect $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, or $V_{CCL_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, or $V_{CCL_GXBL/R}$ to a 1.15-V power supply. For details, refer to the *Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines*.

Table 5 lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus.

Table 5. HPS Power Supply Operating Conditions for Arria V SX and ST Devices *(1)*

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CC_HPS}	HPS Core voltage and periphery circuitry power supply	1.07	1.1	1.13	V
V_{CCPD_HPS} *(2)*	HPS I/O pre-driver (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O pre-driver (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O pre-driver (2.5 V) power supply	2.375	2.5	2.625	V
V_{CCIO_HPS}	HPS I/O buffers (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O buffers (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O buffers (2.5 V) power supply	2.375	2.5	2.625	V
	HPS I/O buffers (1.8 V) power supply	1.71	1.8	1.89	V
	HPS I/O buffers (1.5 V) power supply	1.425	1.5	1.575	V
	HPS I/O buffers (1.35 V) power supply *(3)*	1.283	1.35	1.418	V
	HPS I/O buffers (1.2 V) power supply	1.14	1.2	1.26	V
$V_{CCRSTCLK_HPS}$	HPS reset and clock input pins (3.3 V) power supply	3.135	3.3	3.465	V
	HPS reset and clock input pins (3.0 V) power supply	2.85	3.0	3.15	V
	HPS reset and clock input pins (2.5 V) power supply	2.375	2.5	2.625	V
	HPS reset and clock input pins (1.8 V) power supply	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	2.375	2.5	2.625	V
$V_{CC_AUX_SHARED}$	HPS and FPGA shared auxiliary power supply	2.375	2.5	2.625	V

Notes to Table 5:

(1) Refer to Table 3 for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

(2) V_{CCPD_HPS} must be 2.5 V when V_{CCIO_HPS} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD_HPS} must be 3.0 V when V_{CCIO_HPS} is 3.0 V. V_{CCPD_HPS} must be 3.3 V when V_{CCIO_HPS} is 3.3 V.

(3) V_{CCIO_HPS} 1.35 V is supported for HPS row I/O bank only.

DC Characteristics

This section lists the following specifications:

- Supply Current and Power Consumption
- I/O Pin Leakage Current
- Bus Hold Specifications
- OCT Specifications
- Pin Capacitance
- Hot Socketing

Supply Current and Power Consumption

Standby current is the current drawn from the respective power rails used for power budgeting.

Altera offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus® II PowerPlay Power Analyzer feature.

Use the Excel-based Early Power Estimator (EPE) before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 6 lists the Arria V I/O pin leakage current specifications.

Table 6. I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 7 lists the Arria V device bus hold specifications. The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 7. Bus Hold Parameters for Arria V Devices

Parameter	Symbol	Conditions	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max.)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min.)	–8	—	–12	—	–30	—	–50	—	–70	—	-70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-125	—	-175	—	-200	—	-300	—	-500	—	-500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 8 lists the Arria V OCT termination calibration accuracy specifications. The OCT calibration accuracy is valid at the time of calibration only.

Table 8. OCT Calibration Accuracy Specifications for Arria V Devices

Symbol	Description	Conditions (V)	Calibration Accuracy			Unit
			I3, C4	I5, C5	C6	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω $R_{S_left_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S_left_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 9 lists the Arria V OCT without calibration resistance tolerance to PVT changes.

Table 9. OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices

Symbol	Description	Conditions (V)	Resistance Tolerance			Unit
			I3, C4	I5, C5	C6	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0 and 2.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5	±25	±40	±40	%

Use Table 10 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration *(1), (2), (3), (4), (5), (6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle\right)$$

Notes to Equation 1:

(1) The R_{OCT} value calculated from Equation 1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 10 lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of ±5% and a temperature range of 0° to 85°C.

Table 10. OCT Variation after Power-Up Calibration for Arria V Devices

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

Pin Capacitance

Table 11 lists the Arria V pin capacitance.

Table 11. Pin Capacitance for Arria V Devices

Symbol	Description	Value	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	6	pF
C_{IOLR}	Input capacitance on left/right I/O pins	6	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	6	pF
C_{IOVREF}	Input capacitance on V_{REF} pins	48	pF

Hot Socketing

Table 12 lists the hot socketing specifications for Arria V devices.

Table 12. Hot Socketing Specifications for Arria V Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter (TX) pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver (RX) pin	50 mA

Note to Table 12:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 13 lists the weak pull-up resistor values for Arria V devices.

All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. For more information about the pins that support internal weak pull-up and internal weak pull-down features, refer to the *Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines*.

Table 13. Internal Weak Pull-Up Resistor Values for Arria V Devices

Symbol	Description	Conditions (V) (1)	Value (2)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.3 ±5%	25	kΩ
		V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Notes to Table 13:

(1) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(2) Valid with ±10% tolerances to cover changes over PVT.

I/O Standard Specifications

Table 14 through Table 19 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria V devices.

For an explanation of terms used in Table 14 through Table 19, refer to "Glossary" on page 1–64.

Table 14. Single-Ended I/O Standards for Arria V Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (1) (mA)	I_{OH} (1) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
3.0-V PCI	2.85	3	3.15	—	0.3 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2

Table 14. Single-Ended I/O Standards for Arria V Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (1) (mA)	I_{OH} (1) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.2 V	1.14	1.2	1.26	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2

Note to Table 14:

(1) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTL** specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

Table 15. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{TT}(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 x V_{CCIO}	0.5 x V_{CCIO}	0.53 x V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	—	—	—

Table 16. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V Devices (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OI} (1) (mA)	I_{OH} (1) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} –0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} –0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	16	–16

Table 16. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V Devices (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (1) (mA)	I_{oh} (1) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 x V_{CCIO}	0.8 x V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 x V_{CCIO}	0.8 x V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 x V_{CCIO}	0.9 x V_{CCIO}	—	—

Note to Table 16:

(1) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **SSTL15CI** specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

Table 17. Differential SSTL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	(1)	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$
SSTL-125	1.19	1.25	1.31	0.18	(1)	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$

Note to Table 17:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 18. Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 x V_{CCIO}	—	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 x V_{CCIO} – 0.12	0.5 x V_{CCIO}	0.5 x V_{CCIO} +0.12	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.44	0.44

Table 19. Differential I/O Standard Specifications for Arria V Devices

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (1)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (2)			V_{OCM} (V) (2), (7)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the **PCML** I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 20 and Table 21.														
2.5 V LVDS (3)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	D_{MAX} ≤1.25 Gbps	1.80	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D_{MAX} >1.25 Gbps	1.55						
RSDS (HIO) (4)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (5)	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4
LVPECL (6)	2.375	2.5	2.625	300	—	—	0.60	D_{MAX} ≤700 Mbps	1.80	—	—	—	—	—	—
							1.00	D_{MAX} >700 Mbps	1.60						

Notes to Table 19:

(1) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(2) R_L range: 90 ≤ R_L ≤ 110 Ω

(3) For optimized **LVDS** receiver performance, the receiver voltage input range must be within 1.0V to 1.6V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.

(4) For optimized **RSDS** receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

(5) For optimized **Mini-LVDS** receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.

(6) For optimized **LVPECL** receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

(7) This applies to default pre-emphasis setting only.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks for commercial grade devices.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 20 and Table 21 list the Arria V transceiver specifications.

Table 20. Transceiver Specifications for Arria V GX and SX Devices (Part 1 of 4)

Symbol/ Description	Conditions	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	**1.2 V PCML, 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL** (2), **HCSL**, and **LVDS**							
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	MHz
Rise time	20% to 80% of rising clock edge	—	—	400	—	—	400	ps
Fall time	80% to 20% of falling clock edge	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300/ 2000 (3)	200	—	300/ 2000 (3)	mV
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.1/1.15 (4)	—	—	1.1/1.15 (4)	—	V
V_{ICM} (DC coupled)	**HCSL** I/O standard for the PCIe reference clock	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (1)	10 Hz	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	dBc/Hz
	≥1 MHz	—	—	-130	—	—	-130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

Table 20. Transceiver Specifications for Arria V GX and SX Devices (Part 2 of 4)

Symbol/ Description	Conditions	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Transceiver Clocks								
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	125	75	—	125	MHz
Receiver								
Supported I/O Standards	**1.5 V PCML, 2.5 V PCML, LVPECL**, and **LVDS**							
Data rate *(14)*	—	611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin *(5)*	—	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins *(6)*	—	85	—	—	85	—	—	mV
V_{ICM} (AC coupled)	—	—	650/800 *(7)*	—	—	650/800 *(7)*	—	mV
V_{ICM} (DC coupled)	≤ 3.2 Gbps *(8)*	670	700	730	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	Ω
t_{LTR} *(9)*	—	—	—	10	—	—	10	µs
t_{LTD} *(10)*	—	4	—	—	4	—	—	µs
t_{LTD_manual} *(11)*	—	4	—	—	4	—	—	µs
$t_{LTR_LTD_manual}$ *(12)*	—	15	—	—	15	—	—	µs
Programmable ppm detector *(13)*	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000						ppm
Run Length	—	—	—	200	—	—	200	UI

Table 20. Transceiver Specifications for Arria V GX and SX Devices (Part 3 of 4)

Symbol/ Description	Conditions	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Programmable equalization (AC) and DC gain	AC gain setting = 0 to 3 (16) DC gain setting = 0 to 1	Refer to Figure 1 and Figure 2						dB
Transmitter								
Supported I/O standards	**1.5 V PCML**							
Data rate	—	611	—	6553.6	611	—	3125	Mbps
V_{OCM} (AC coupled)	—	—	650	—	—	650	—	mV
V_{OCM} (DC coupled)	≤ 3.2 Gbps (8)	670	700	730	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	Ω
Intra-differential pair skew	TX VCM = 0.65 V (AC coupled) and slew rate of 15 ps	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode	—	—	180	—	—	180	ps
Inter-transceiver block transmitter channel-to-channel skew (15)	x*N* PMA bonded mode	—	—	500	—	—	500	ps
CMU PLL								
Supported data range	—	611	—	6553.6	611	—	3125	Mbps
fPLL supported data range	—	611	—	3125	611	—	3125	Mbps
Transceiver-FPGA Fabric Interface								
Interface speed (single-width mode)	—	25	—	187.5	25	—	187.5	MHz

Table 20. Transceiver Specifications for Arria V GX and SX Devices (Part 4 of 4)

Symbol/ Description	Conditions	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Interface speed (double-width mode)	—	25	—	163.84	25	—	163.84	MHz

Notes to Table 20:

(1) The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10^{-12}.

(2) Differential **LVPECL** signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(3) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

(4) For data rate <=3.2 Gbps, connect $V_{CCR_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR_GXBL/R}$ to a 1.15-V power supply. For details, refer to the *Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines*.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) The AC coupled V_{ICM} is 650 mV for PCIe mode only.

(8) For standard protocol compliance, use AC coupling.

(9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(13) The rate match FIFO supports only up to ±300 parts per million (ppm).

(14) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

(15) This specification is only applicable to channels on one side of the device across two transceiver banks.

(16) The Quartus II software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

Table 21. Transceiver Specifications for Arria V GT and ST Devices (Part 1 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Reference Clock					
Supported I/O Standards	**1.2 V PCML**, **1.4 V PCML**, **1.5 V PCML**, **2.5 V PCML**, **Differential LVPECL** *(2)*, **HCSL**, and **LVDS**				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Rise time	20% to 80% of rising clock edge	—	—	400	ps
Fall time	80% to 20% of falling clock edge	—	—	400	ps
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300/2000 *(3)*	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.2	—	V
V_{ICM} (DC coupled)	**HCSL** I/O standard for the PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise *(1)*	10 Hz	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	dBc/Hz
	≥1 MHz	—	—	-130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	Ω
Transceiver Clocks					
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency	—	75	—	125	MHz
Receiver					
Supported I/O Standards	**1.5 V PCML**, **2.5 V PCML**, **LVPECL**, and **LVDS**				
Data rate (6-Gbps Transceiver) *(15)*	—	611	—	6553.6	Mbps
Data rate (10-Gbps transceiver) *(15)*	—	0.611	—	10.3125	Gbps
Absolute V_{MAX} for a receiver pin *(4)*	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	V

Table 21. Transceiver Specifications for Arria V GT and ST Devices (Part 2 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins (5)	—	85	—	—	mV
V_{ICM} (AC coupled)	—	—	650/800 (6)	—	mV
V_{ICM} (DC coupled)	≤ 3.2 Gbps (7)	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	85			Ω
	100-Ω setting	100			Ω
	120-Ω setting	120			Ω
	150-Ω setting	150			Ω
t_{LTR} (8)	—	—	—	10	µs
t_{LTD} (9)	—	4	—	—	µs
t_{LTD_manual} (10)	—	4	—	—	µs
$t_{LTR_LTD_manual}$ (11)	—	15	—	—	µs
Programmable ppm detector (12)	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000			ppm
Run Length	—	—	—	200	UI
Programmable equalization (AC) and DC gain	AC gain setting = 0 to 3 (17) DC gain setting = 0 to 1	Refer to Figure 1 and Figure 2			
Transmitter					
Supported I/O Standards	**1.5 V PCML**				
Data rate (6-Gbps transceiver)	—	611	—	6553.6	Mbps
Data rate (10-Gbps transceiver)	—	0.611	—	10.3125	Gbps
V_{OCM} (AC coupled)	—	—	650	—	mV
V_{OCM} (DC coupled)	≤3.2 Gbps (7)	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Intra-differential pair skew	TX VCM = 0.65 V (AC coupled) and slew rate of 15 ps	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode	—	—	180	ps
Inter-transceiver block transmitter channel-to-channel skew (16)	x*N* PMA bonded mode	—	—	500	ps

Table 21. Transceiver Specifications for Arria V GT and ST Devices (Part 3 of 3)

Symbol/ Description	Conditions	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
CMU PLL					
Supported data range	—	0.611	—	10.3125	Gbps
fPLL supported data range	—	611	—	3125	Mbps
Transceiver-FPGA Fabric Interface					
Interface speed (PMA direct mode)	—	50	—	153.6 (13), 161 (14)	MHz
Interface speed (single-width mode)	—	25	—	187.5	MHz
Interface speed (double-width mode)	—	25	—	163.84	MHz

Notes to Table 21:

(1) The transmitter REFCLK phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

(2) Differential **LVPECL** signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(3) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

(4) The device cannot tolerate prolonged operation at this absolute maximum.

(5) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(6) The AC coupled V_{ICM} is 650 mV for PCIe mode only.

(7) For standard protocol compliance, use AC coupling.

(8) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(9) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(10) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(11) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(12) The rate match FIFO supports only up to ±300 ppm.

(13) The maximum frequency when core transceiver local routing is selected.

(14) The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

(15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

(16) This specification is only applicable to channels on one side of the device across two transceiver banks.

(17) The Quartus II software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

Figure 1 shows the continuous time-linear equalizer (CTLE) response at data rates > 3.25 Gbps across supported AC gain and DC gain settings for Arria V GX, GT, SX, and ST devices.

Figure 1. CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices

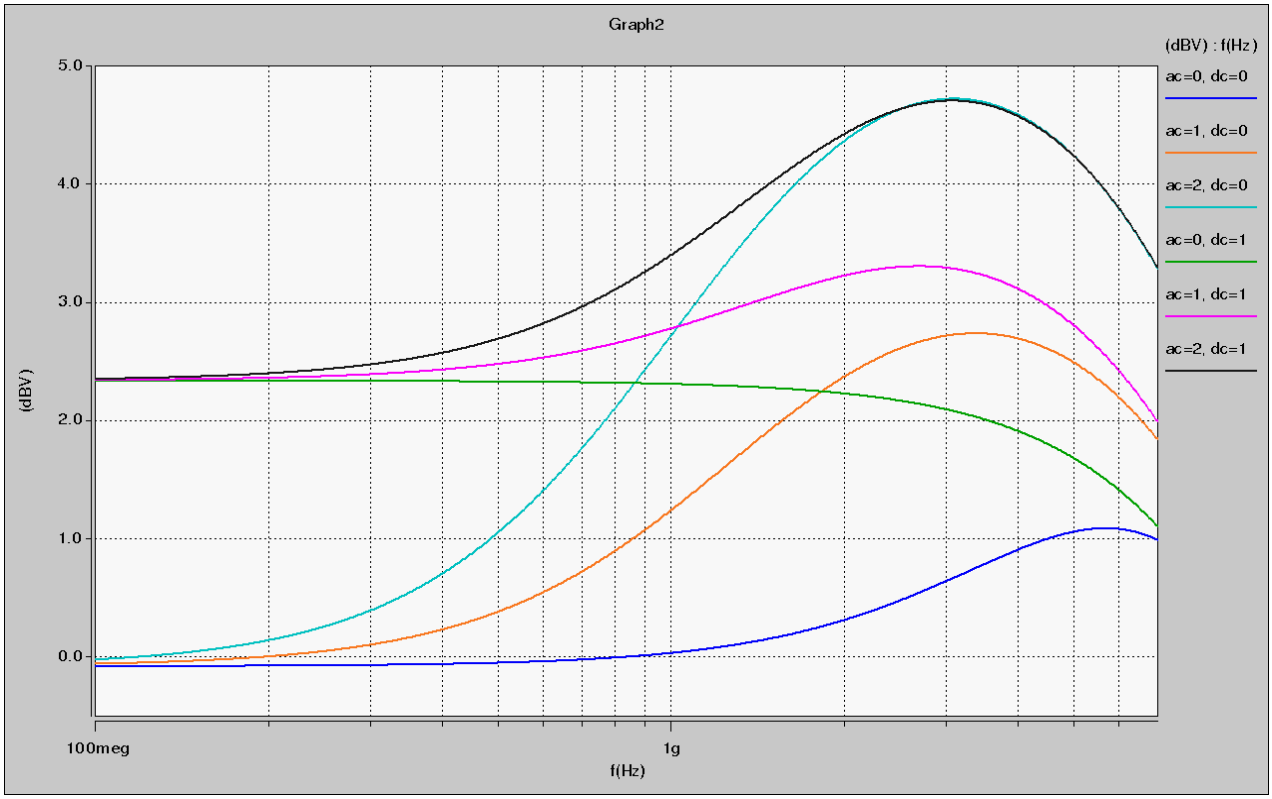


Figure 2 shows the CTLE response at data rates ≤3.25 Gbps across supported AC gain and DC gain settings for Arria V GX, GT, SX, and ST devices.

Figure 2. CTLE Response at Data Rates ≤3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices

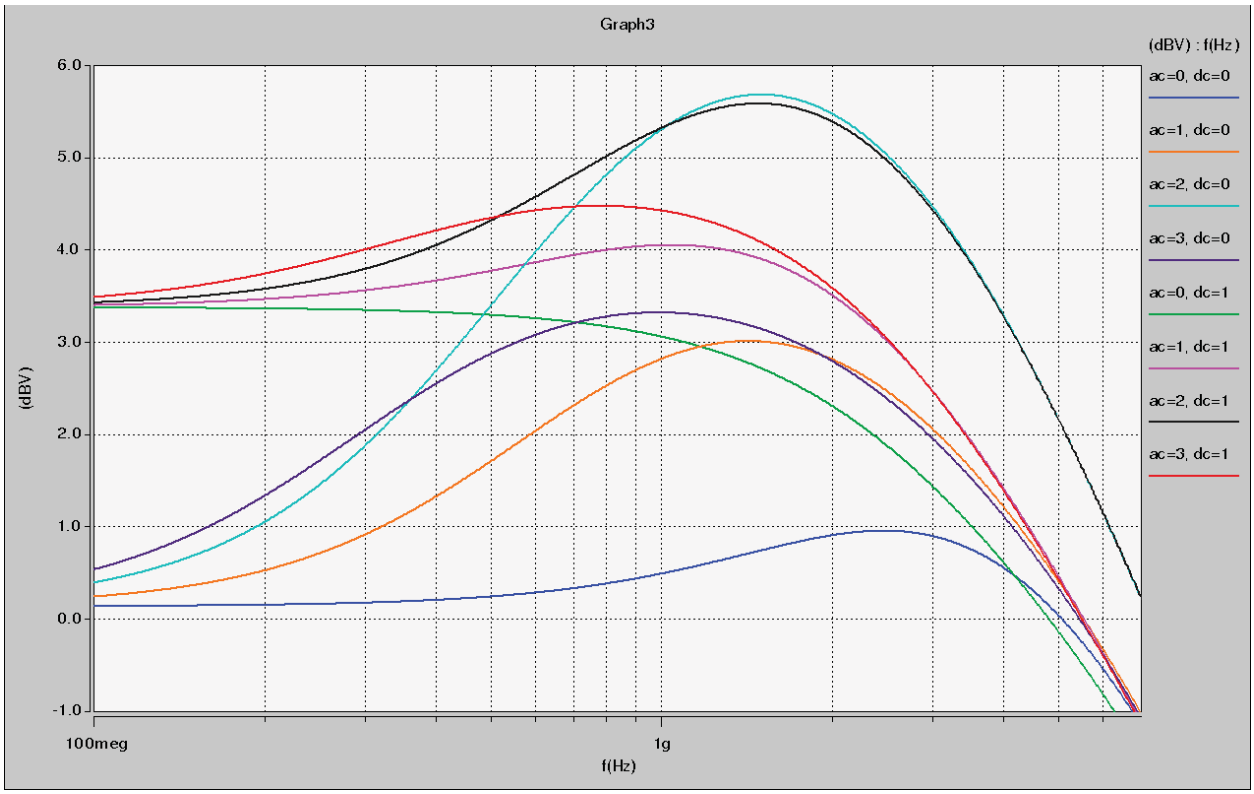


Table 22 lists the TX V_{OD} settings for Arria V transceiver channels.

Table 22. Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Symbol	V_{OD} Setting (1)	V_{OD} Value (mV)	V_{OD} Setting (1)	V_{OD} Value (mV)
V_{OD} differential peak to peak typical	6 (2)	120	34	680
	7 (2)	140	35	700
	8 (2)	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Notes to Table 22:

(1) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

(2) Only valid for data rates ≤ 5 Gbps.

Table 23 lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- low-frequency data pattern—five 1s and five 0s
- data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

Exception for PCIe Gen2 design:

V_{OD} setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis –6dB setting (`pipe_txdeemp` = **1'b0**) using Altera PCIe Hard IP and PIPE megafunctions.

For example, when V_{OD} = 800 mV, the corresponding V_{OD} value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is a valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

Table 23. Transmitter Pre-Emphasis Levels for Arria V Devices (Part 1 of 2)

Quartus II 1st Post Tap Pre-Emphasis Setting	Quartus II V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB

Table 23. Transmitter Pre-Emphasis Levels for Arria V Devices (Part 2 of 2)

Quartus II 1st Post Tap Pre-Emphasis Setting	Quartus II V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Table 24 lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Table 24. Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices (Part 1 of 2)

Protocol	Sub-protocol	Data Rate (Mbps)
PCIe	PCIe Gen1	2,500
	PCIe Gen2	5,000
	PCIe Cable	2,500
XAUI	XAUI 2135	3,125
Serial RapidIO® (SRIO)	SRIO 1250 SR	1,250
	SRIO 1250 LR	1,250
	SRIO 2500 SR	2,500
	SRIO 2500 LR	2,500
	SRIO 3125 SR	3,125
	SRIO 3125 LR	3,125
	SRIO 5000 SR	5,000
	SRIO 5000 MR	5,000
	SRIO 5000 LR	5,000
	SRIO_6250_SR	6,250
	SRIO_6250_MR	6,250
	SRIO_6250_LR	6,250
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII	4,915.2
	CPRI E60LVII	6,144
	CPRI E96LVIII (1)	9,830.4
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
	OBSAI 6144	6,144

Table 24. Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices (Part 2 of 2)

Protocol	Sub-protocol	Data Rate (Mbps)
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970
SONET	SONET 155	155.52
	SONET 622	622.08
	SONET 2488	2,488.32
Gigabit-capable passive optical network (GPON)	GPON 155	155.52
	GPON 622	622.08
	GPON 1244	1,244.16
	GPON 2488	2,488.32
QSGMII	QSGMII 5000	5,000

Note to Table 24:

(1) You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks and temperature sensing diode specifications.

Clock Tree Specifications

Table 25 lists the clock tree specifications for Arria V devices.

Table 25. Clock Tree Performance for Arria V Devices

Parameter	Performance			Unit
	–I3, –C4	–I5, –C5	–C6	
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 26 lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.

Table 26. PLL Specifications for Arria V Devices (Part 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–3 speed grade)	5	—	800 (1)	MHz
	Input clock frequency (–4 speed grade)	5	—	800 (1)	MHz
	Input clock frequency (–5 speed grade)	5	—	750 (1)	MHz
	Input clock frequency (–6 speed grade)	5	—	625 (1)	MHz
f_{INPFD}	Integer input clock frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	50	—	160	MHz
f_{VCO} (2)	PLL VCO operating range (–3 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–4 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–5 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–6 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (–3 speed grade)	—	—	500 (3)	MHz
	Output frequency for internal global or regional clock (–4 speed grade)	—	—	500 (3)	MHz
	Output frequency for internal global or regional clock (–5 speed grade)	—	—	500 (3)	MHz
	Output frequency for internal global or regional clock (–6 speed grade)	—	—	400 (3)	MHz
f_{OUT_EXT}	Output frequency for external clock output (–3 speed grade)	—	—	670 (3)	MHz
	Output frequency for external clock output (–4 speed grade)	—	—	670 (3)	MHz
	Output frequency for external clock output (–5 speed grade)	—	—	622 (3)	MHz
	Output frequency for external clock output (–6 speed grade)	—	—	500 (3)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%

Table 26. PLL Specifications for Arria V Devices (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (8)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} (4), (5)	Input clock cycle-to-cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} (6)	Period jitter for dedicated clock output in integer PLL ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period jitter for dedicated clock output in integer PLL ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{FOUTPJ_DC} (6)	Period jitter for dedicated clock output in fractional PLL ($F_{OUT} \geq 100$ MHz)	—	—	250 (10), 175 (11)	ps (p-p)
	Period jitter for dedicated clock output in fractional PLL ($F_{OUT} < 100$ MHz)	—	—	25 (10), 17.5 (11)	mUI (p-p)
t_{OUTCCJ_DC} (6)	Cycle-to-cycle jitter for dedicated clock output in integer PLL ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-cycle jitter for dedicated clock output in integer PLL ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{FOUTCCJ_DC}$ (6)	Cycle-to-cycle jitter for dedicated clock output in fractional PLL ($F_{OUT} \geq 100$ MHz)	—	—	250 (10), 175 (11)	ps (p-p)
	Cycle-to-cycle jitter for dedicated clock output in fractional PLL ($F_{OUT} < 100$ MHz)	—	—	25 (10), 17.5 (11)	mUI (p-p)
t_{OUTPJ_IO} (6), (9)	Period jitter for clock output on a regular I/O in integer PLL ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period jitter for clock output on a regular I/O in integer PLL ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{FOUTPJ_IO} (6), (9), (10)	Period jitter for clock output on a regular I/O in fractional PLL ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period jitter for clock output on a regular I/O in fractional PLL ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (6), (9)	Cycle-to-cycle jitter for clock output on a regular I/O in integer PLL ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle jitter for clock output on a regular I/O in integer PLL ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)

Table 26. PLL Specifications for Arria V Devices (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{FOUTCCJ_IO}$ *(6), (9), (10)*	Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC_OUTPJ_DC}$ *(6), (7)*	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	bits
k_{VALUE}	Numerator of fraction	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency (f_{INPFD} =100 MHz)	390625	5.96	0.023	Hz

Notes to Table 26:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) The voltage-controlled oscillator (VCO) frequency reported by the Quartus II software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(3) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

(4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(5) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 35 on page 1–39.

(7) The cascaded PLL specification is only applicable with the following conditions:
a. Upstream PLL: 0.59 MHz ≤Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(8) High bandwidth PLL settings are not supported in external feedback mode.

(9) External memory interface clock output jitter specifications use a different measurement method, which are available in Table 35 on page 1–39.

(10) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(11) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

DSP Block Specifications

Table 27 lists the Arria V DSP block performance specifications.

Table 27. DSP Block Performance Specifications for Arria V Devices (Part 1 of 2)

Mode	Performance			Unit
	–I3, –C4	–I5, –C5	–C6	
Modes using One DSP Block				
Independent 9 x 9 Multiplication	370	310	220	MHz
Independent 18 x 19 Multiplication	370	310	220	MHz
Independent 18 x 25 Multiplication	370	310	220	MHz
Independent 20 x 24 Multiplication	370	310	220	MHz
Independent 27 x 27 Multiplication	310	250	200	MHz
Two 18 x 19 Multiplier Adder Mode	370	310	220	MHz
18 x 18 Multiplier Added Summed with 36-bit Input	370	310	220	MHz

Table 27. DSP Block Performance Specifications for Arria V Devices (Part 2 of 2)

Mode	Performance			Unit
	–I3, –C4	–I5, –C5	–C6	
Modes using Two DSP Blocks				
Complex 18 x 19 multiplication	370	310	220	MHz

Memory Block Specifications

Table 28 lists the Arria V memory block specifications.

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Quartus II software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 28. Memory Block Performance Specifications for Arria V Devices

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–I3, –C4	–I5, –C5	–C6	
MLAB	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	—	—	500	450	400	MHz
M10K Block	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz

Temperature Sensing Diode Specifications

Table 29 lists the specifications for the Arria V internal temperature sensing diode.

Table 29. Internal Temperature Sensing Diode Specifications for Arria V Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40 to 100°C	±8°C	No	Frequency: 1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 30 lists high-speed I/O timing for Arria V devices.

Table 30. High-Speed I/O Specifications for Arria V Devices (1), (2), (3) (Part 1 of 3)

Symbol	Conditions	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (6)	5	—	800	5	—	750	5	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (4)	Clock boost factor W = 1 to 40 (6)	5	—	625	5	—	625	5	—	500	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (5)	Clock boost factor W = 1 to 40 (6)	5	—	420	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	625 (7)	5	—	625 (7)	5	—	500 (7)	MHz
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (8)	(9)	—	1250	(9)	—	1250	(9)	—	1050	Mbps
	SERDES factor J ≥ 8 (8), (10) LVDS TX with RX DPA	(9)	—	1600	(9)	—	1500	(9)	—	1250	Mbps
	SERDES factor J = 1 to 2 Uses DDR Registers	(9)	—	(11)	(9)	—	(11)	(9)	—	(11)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate) (12)	SERDES factor J = 4 to 10	(9)	—	945	(9)	—	945	(9)	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate) (12)	SERDES factor J = 4 to 10	(9)	—	200	(9)	—	200	(9)	—	200	Mbps

Table 30. High-Speed I/O Specifications for Arria V Devices (1), (2), (3) (Part 2 of 3)

Symbol	Conditions	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate, 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate, 600 Mbps – 1.25 Gbps	—	—	260	—	—	300	—	—	350	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.16	—	—	0.18	—	—	0.21	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with One External Output Resistor Network	—	—	—	0.15	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards (13)	—	—	160	—	—	180	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Network	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor Network	—	—	500	—	—	500	—	—	500	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver											
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 (8)	150	—	1250	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 8 with DPA (8), (10)	150	—	1600	150	—	1500	150	—	1250	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(9)	—	(14)	(9)	—	(14)	(9)	—	(14)	Mbps
	SERDES factor J = 1 to 2 Uses DDR Registers	(9)	—	(11)	(9)	—	(11)	(9)	—	(11)	Mbps
DPA Mode											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode											
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	± ppm

Table 30. High-Speed I/O Specifications for Arria V Devices (1), (2), (3) (Part 3 of 3)

Symbol	Conditions	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Non DPA Mode											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

Notes to Table 30:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) For LVDS applications, you must use the PLLs in integer PLL mode.

(4) This applies to DPA and soft-CDR modes only.

(5) This applies to non-DPA mode only.

(6) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(7) This is achieved by using the LVDS clock network.

(8) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(9) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(10) The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.

(11) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.

(12) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

(13) This applies to default pre-emphasis and V_{OD} settings only.

(14) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Figure 3 shows the DPA lock time specifications with the DPA PLL calibration option enabled.

Figure 3. DPA Lock Time Specification with DPA PLL Calibration Enabled

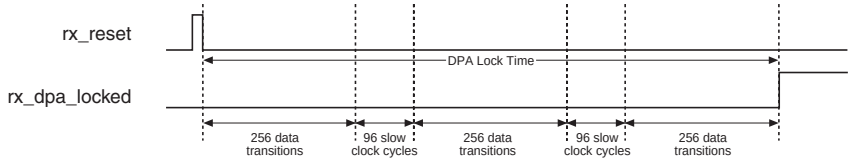


Table 31 lists the DPA lock time specifications for Arria V devices, which are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Table 31. DPA Lock Time Specifications for Arria V Devices

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (1)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

Note to Table 31:

(1) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 4 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.25 Gbps.

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

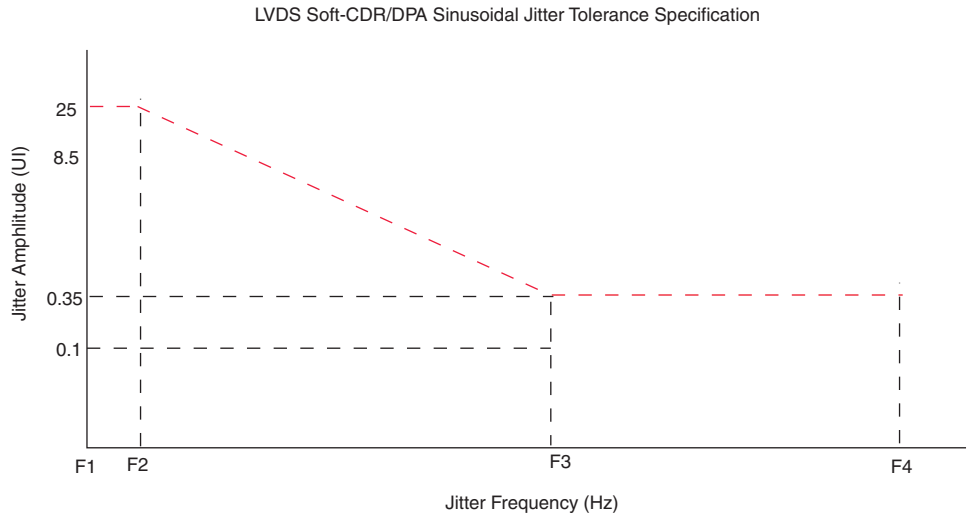


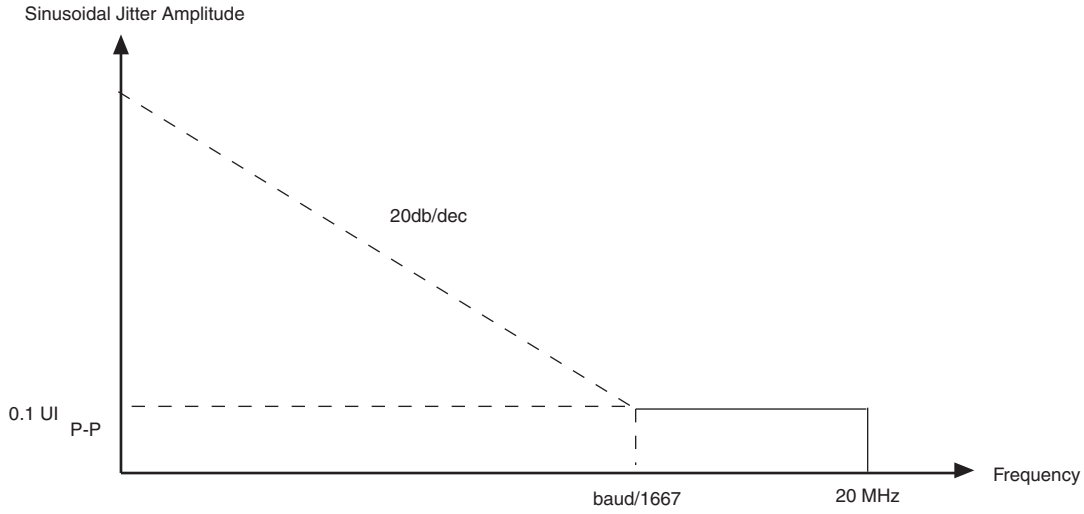
Table 32 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.25 Gbps.

Table 32. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate less than 1.25 Gbps.

Figure 5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 33 lists the DLL frequency range specifications for Arria V devices.

Table 33. DLL Frequency Range Specifications for Arria V Devices

Parameter	–I3, –C4	–I5, –C5	–C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

Table 34 lists the DQS phase shift error for Arria V devices. This error specification is the absolute maximum and minimum error.

Table 34. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V Devices

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	–C6	Unit
2	40	80	80	ps

Table 35 lists the memory output clock jitter specifications for Arria V devices.

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Table 35. Memory Output Clock Jitter Specification for Arria V Devices

Parameter	Clock Network	Symbol	–I3, –C4		–I5, –C5		–C6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	–41	41	–50	50	–55	55	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	63		90		94		ps

OCT Calibration Block Specifications

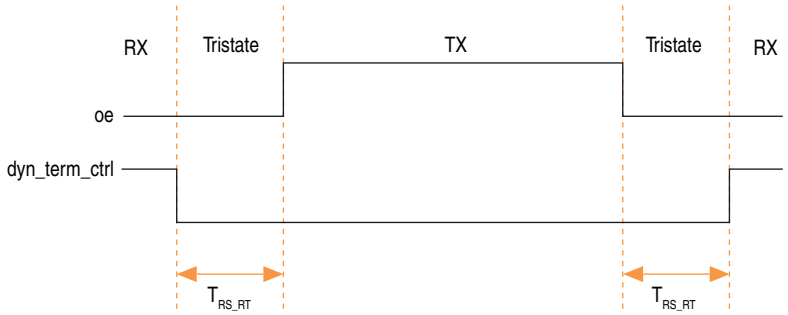
Table 36 lists the OCT calibration block specifications for Arria V devices.

Table 36. OCT Calibration Block Specifications for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 6 shows the T_{RS_RT} for `oe` and `dyn_term_ctrl` signals.

Figure 6. Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 37 lists the worst-case DCD for Arria V devices. The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

Table 37. Worst-Case DCD on Arria V I/O Pins

Symbol	–I3, –C4		–C5,–I5		–C6		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

HPS Clock Performance

Table 38 lists the HPS clock performance for Arria V devices.

Table 38. HPS Clock Performance for Arria V Devices

Symbol/Description	–I3	–C4	–C5, –I5	–C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	525	462	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 39 lists the HPS PLL VCO frequency range for Arria V devices. This specification applies to all speed grade.

Table 39. HPS PLL VCO Frequency Range for Arria V Devices

Description	Minimum	Maximum	Unit
VCO range	320	1,600	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz.

For more information about the clock range for different values of clock select (CSEL), refer to the *Booting and Configuration* chapter.

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate.

Maximum input jitter = Input clock period x Divide value (NR) x 0.02

Table 40 shows the examples of the maximum input jitter calculated with the equation.

Table 40. Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (NR)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

QSPI Timing Characteristics

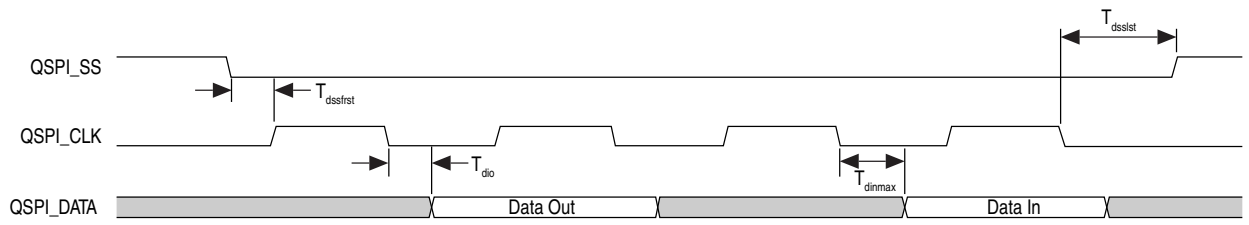
Table 41 lists the queued serial peripheral interface (QSPI) timing characteristics for Arria V devices.

Table 41. QSPI Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	CLK clock frequency	—	—	108	MHz
$T_{dutycycle}$	QSPI_CLK duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of QSPI_CLK	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	IO Data output delay	–1	—	1	ns
T_{dinmax}	Maximum data input delay from falling edge of QSPI_CLK to data arrival at SoC. The delay field of the `qspiregs.rddatacap` register can be programmed to adjust the capture logic of the incoming data.	—	—	—	—

Figure 7 shows the timing diagram for QSPI timing characteristics. This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.

Figure 7. QSPI Timing Diagram



SPI Timing Characteristics

Table 42 lists the serial peripheral interface (SPI) master timing characteristics for Arria V devices. The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Table 42. SPI Master Timing Requirements for Arria V Devices

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	—	16.67	ns
$T_{dutycycle}$	SPI_CLK duty cycle	45	55	%
$T_{dssfrst}$	Output delay SPI_SS valid before first clock edge	8	—	ns
T_{dsslst}	Output delay SPI_SS valid after last clock edge	8	—	ns
T_{dio}	Master-out slave-in (MOSI) output delay	–1	1	ns
T_{dinmax}	Maximum data input delay from falling edge of SPI_CLK to data arrival at SoC. The RX sample delay register can be programmed to control the capture of input data.	—	500	ns
—	Slave select pulse width (Texas Instruments SSP mode)	—	16.67	ns

Figure 8 shows the timing diagram for SPI master timing characteristics.

Figure 8. SPI Master Timing Diagram

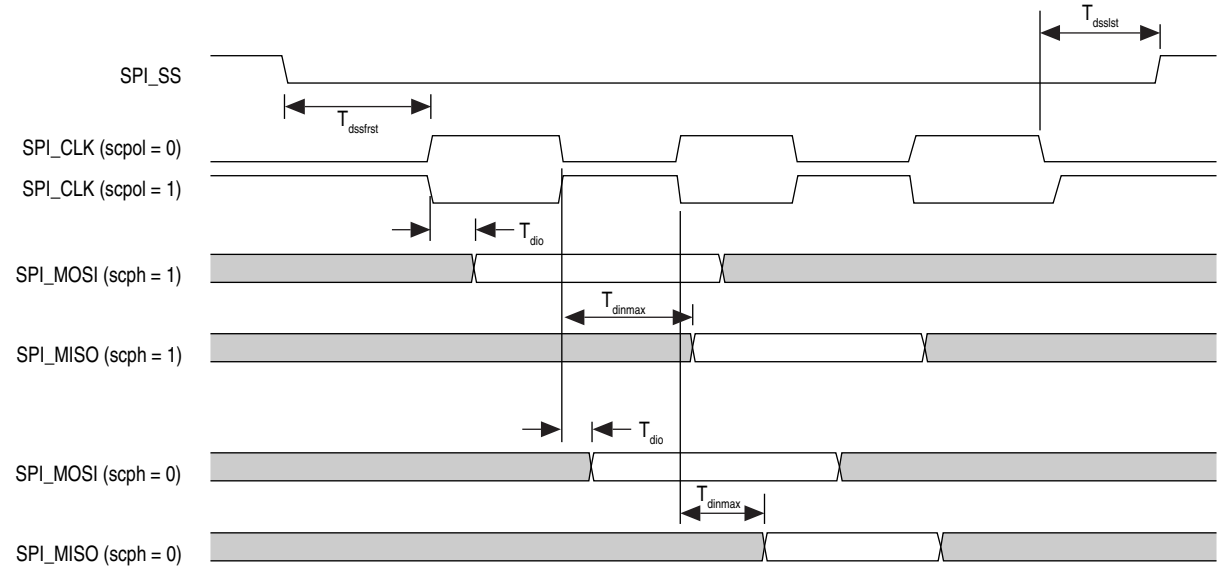


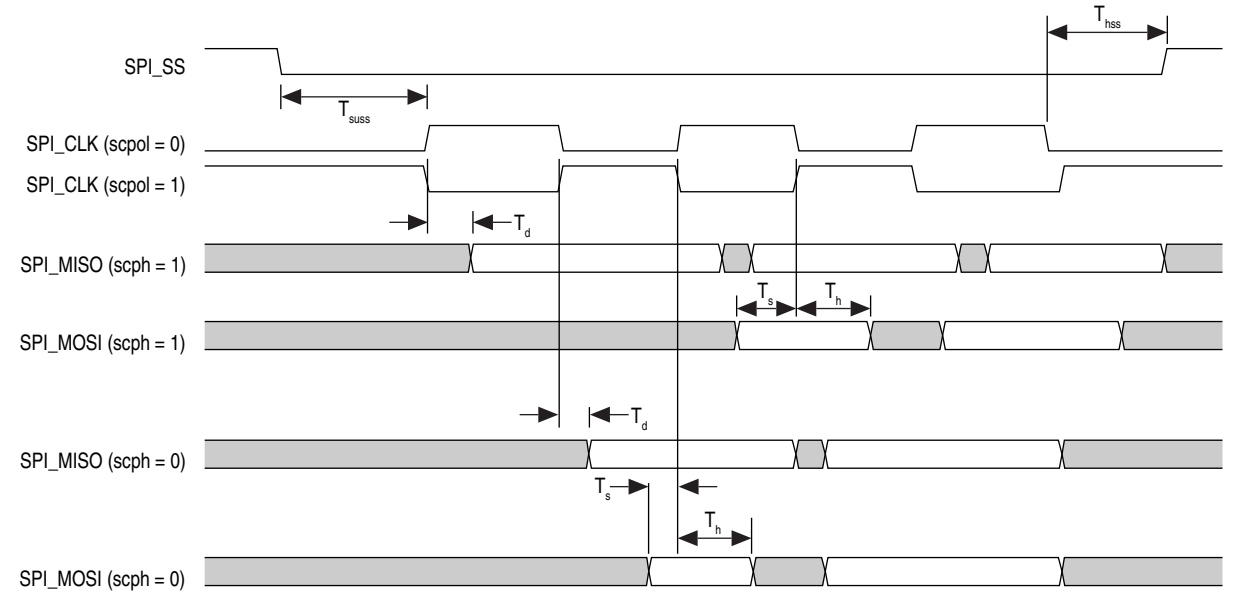
Table 43 lists the SPI slave timing characteristics for Arria V devices. The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Table 43. SPI Slave Timing Requirements for Arria V Devices

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	20	—	ns
T_s	MOSI Setup time	5	—	ns
T_h	MOSI Hold time	5	—	ns
T_{suss}	Setup time SPI_SS valid before first clock edge	8	—	ns
T_{hss}	Hold time SPI_SS valid after last clock edge	8	—	ns
T_d	Master-in slave-out (MISO) output delay	—	6	ns
—	Slave select pulse width (Texas Instruments SSP mode)	20	—	ns

Figure 9 shows the timing diagram for SPI slave timing characteristics.

Figure 9. SPI Slave Timing Diagram



SD/MMC Timing Characteristics

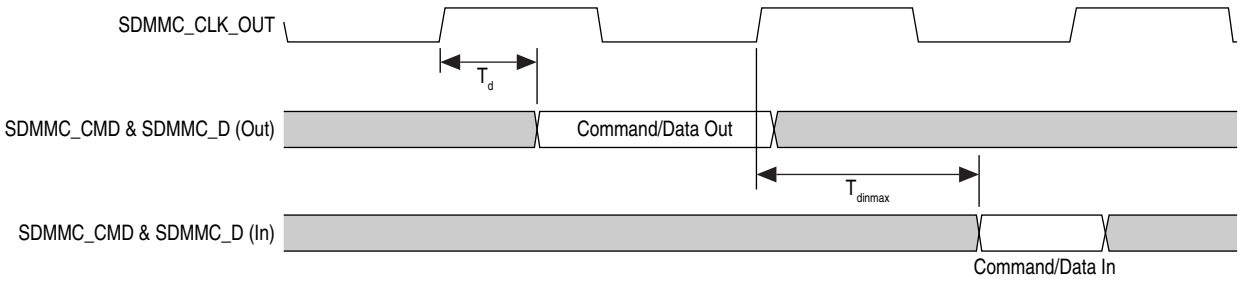
Table 44 lists the secure digital (SD)/MultiMediaCard (MMC) timing characteristics for Arria V devices.

Table 44. SD/MMC Timing Requirements for Arria V Devices

Symbol	Description	Min	Max	Unit
T_{clk}	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
$T_{dutycycle}$	SDMMC_CLK_OUT duty cycle	45	55	%
T_d	SDMMC_CMD/SDMMC_D output delay	—	6	ns
T_{dinmax}	Maximum input delay from rising edge of SDMMC_CLK to data arrival at SoC	—	25	ns

Figure 10 shows the timing diagram for SD/MMC timing characteristics.

Figure 10. SD/MMC Timing Diagram



USB Timing Characteristics

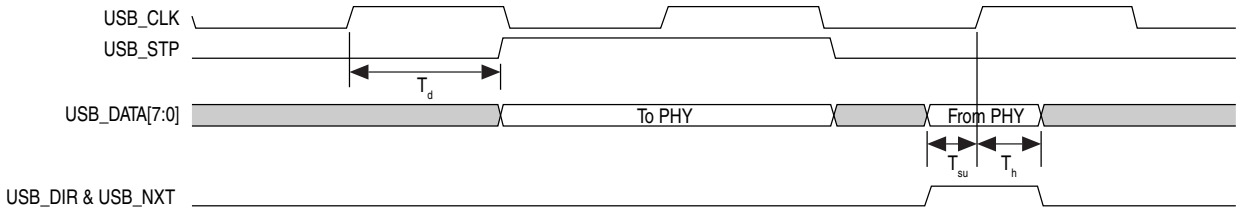
Table 45 lists the USB timing characteristics for Arria V devices.

Table 45. USB Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	—	16.67	—	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	7.5	—	11	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	2.5	—	—	ns

Figure 11 shows the timing diagram for USB timing characteristics.

Figure 11. USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 46 lists the reduced gigabit media independent interface (RGMII) TX timing characteristics for Arria V devices.

Table 46. RGMII TX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$	TX_CLK duty cycle	45	—	55	%
T_d	TX_CLK to TXD/TX_CTL output data delay	–0.85	—	0.15	ns

Figure 12 shows the timing diagram for RGMII TX timing characteristics.

Figure 12. RGMII TX Timing Diagram

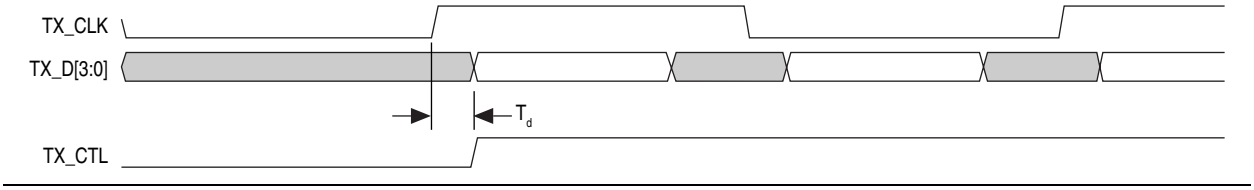


Table 47 lists the RGMII RX timing characteristics for Arria V devices.

Table 47. RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	ns
T_{su}	RX_D/RX_CTL setup time	1	—	ns

Figure 13 shows the timing diagram for RGMII RX timing characteristics.

Figure 13. RGMII RX Timing Diagram

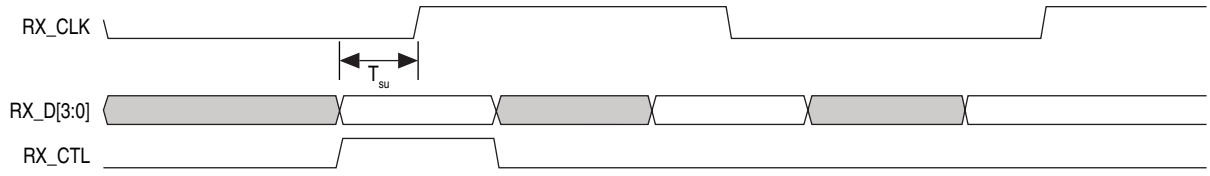


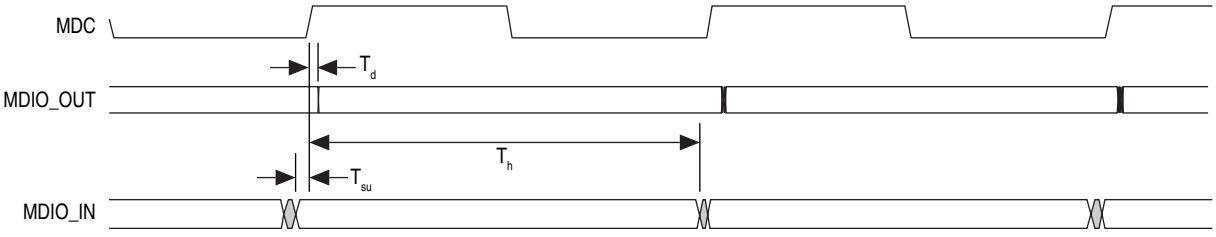
Table 48 lists the management data input/output (MDIO) timing characteristics for Arria V devices.

Table 48. MDIO Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Unit
T_{clk}	MDC clock period	—	400	ns
T_d	MDC to MDIO output data delay	10	—	ns
T_s	Setup time for MDIO data	10	—	ns
T_h	Hold time for MDIO data	0	—	ns

Figure 14 shows the timing diagram for MDIO timing characteristics.

Figure 14. MDIO Timing Diagram



I²C Timing Characteristics

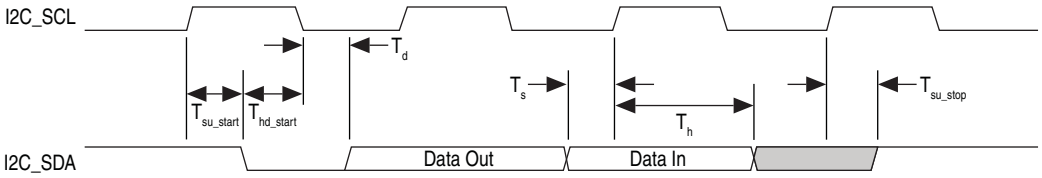
Table 49 lists the I²C timing characteristics for Arria V devices.

Table 49. I²C Timing Requirements for Arria V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	—	10	—	2.5	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

Figure 15 shows the timing diagram for I²C timing characteristics.

Figure 15. I²C Timing Diagram



NAND Timing Characteristics

Table 50 lists the NAND timing characteristics for Arria V devices.

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. The following table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Table 50. NAND ONFI 1.0 Timing Requirements for Arria V Devices (Part 1 of 2)

Symbol	Description	Min	Max	Unit
T_{wp} (1)	Write enable pulse width	10	—	ns
T_{wh} (1)	Write enable hold time	7	—	ns
T_{rp} (1)	Read Enable pulse width	10	—	ns
T_{reh} (1)	Read enable hold time	7	—	ns
T_{clesu} (1)	Command latch enable to write enable setup time	10	—	ns
T_{cleh} (1)	Command latch enable to write enable hold time	5	—	ns
T_{cesu} (1)	Chip enable to write enable setup time	15	—	ns

Table 50. NAND ONFI 1.0 Timing Requirements for Arria V Devices (Part 2 of 2)

Symbol	Description	Min	Max	Unit
T_{ceh} (1)	Chip enable to write enable hold time	5	—	ns
T_{alesu} (1)	Address latch enable to write enable setup time	10	—	ns
T_{aleh} (1)	Address latch enable to write enable hold time	5	—	ns
T_{dsu} (1)	Data to write enable setup time	10	—	ns
T_{dh} (1)	Data to write enable hold time	5	—	ns
T_{cea}	Chip enable to data access time	—	25	ns
T_{rea}	Read enable to data access time	—	16	ns
T_{rhz}	Read enable to data high impedance	—	100	ns
T_{rr}	Ready to read enable low	20	—	ns

Note to Table 50:

(1) Timing of the NAND interface is controlled through the NAND Configuration registers.

Figure 16 shows the timing diagram for NAND command latch timing characteristics.

Figure 16. NAND Command Latch Timing Diagram

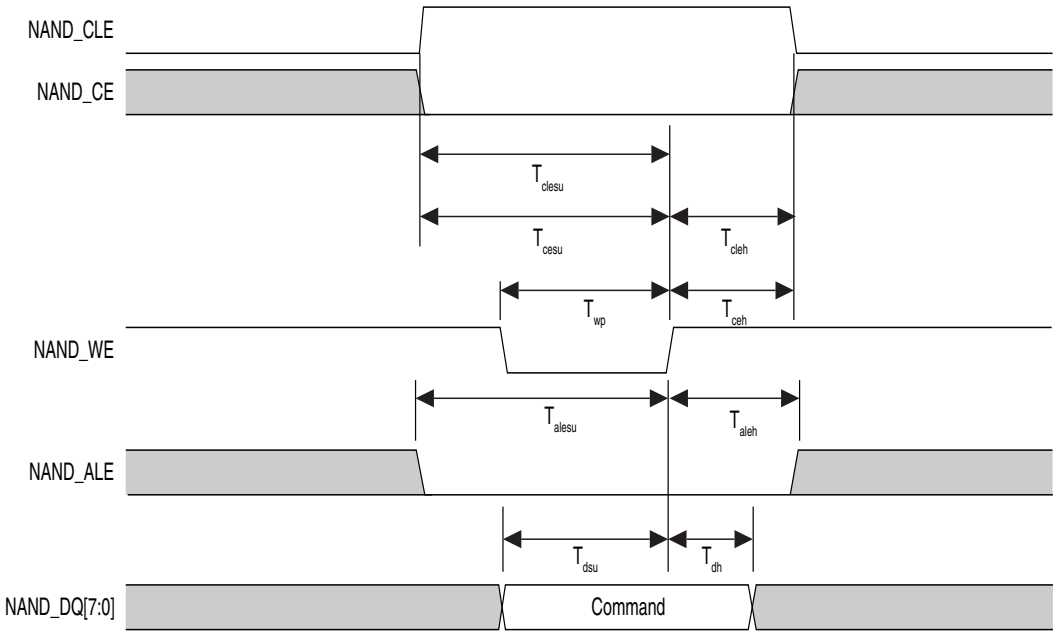


Figure 17 shows the timing diagram for NAND address latch timing characteristics.

Figure 17. NAND Address Latch Timing Diagram

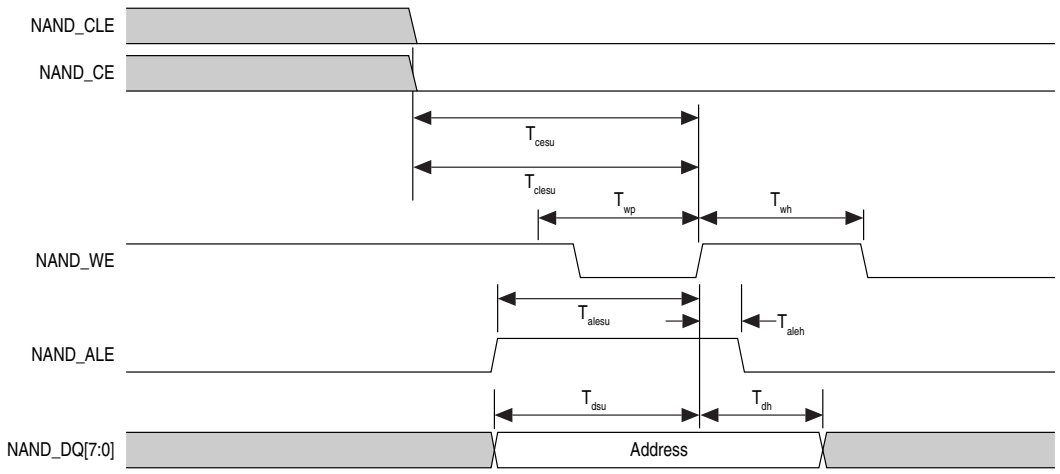


Figure 18 shows the timing diagram for NAND data write timing characteristics.

Figure 18. NAND Data Write Timing Diagram

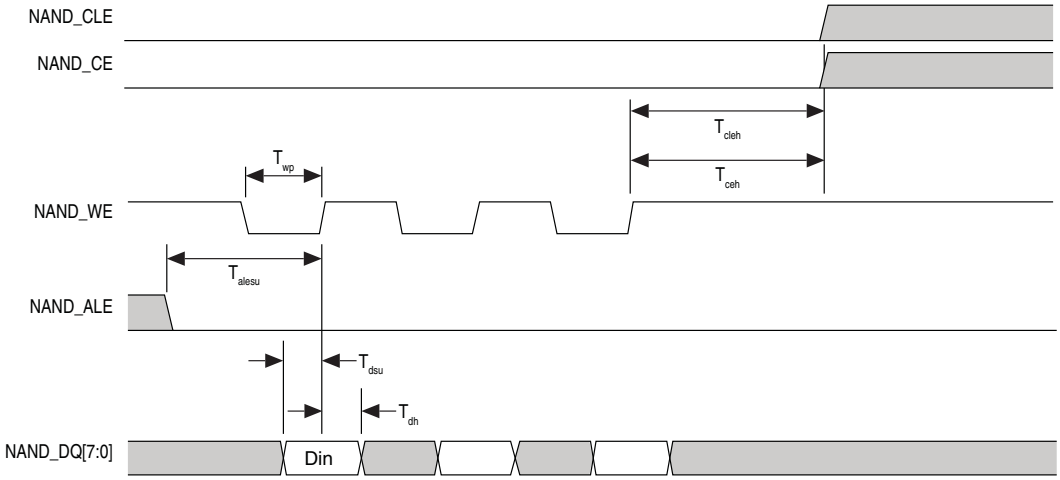
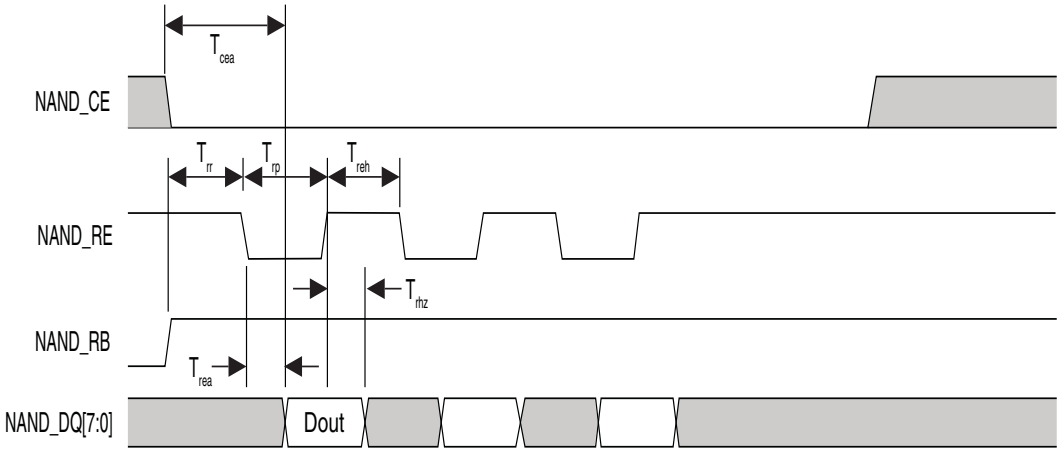


Figure 19 shows the timing diagram for NAND data read timing characteristics.

Figure 19. NAND Data Read Timing Diagram



ARM Trace Timing Characteristics

Table 51 lists the ARM trace timing characteristics for Arria V devices.

Most debugging tools have a mechanism to adjust the capture point of trace data.

Table 51. ARM Trace Timing Requirements for Arria V Devices

Description	Min	Max	Unit
CLK clock period	12.5	—	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	–1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 µs. The pulse width is based on a debounce clock frequency of 1 MHz.

Configuration Specification

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 52 lists the specifications for fast and standard POR for Arria V devices.

Table 52. Fast and Standard POR Delay Specification for Arria V Devices (1)

POR Delay	Minimum	Maximum	Unit
Fast	4	12 (2)	ms
Standard	100	300	ms

Notes to Table 52:

(1) Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(2) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

JTAG Configuration Timing

Table 53 lists the JTAG timing parameters and values for Arria V devices.

Table 53. JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCP}	TCK clock period	167 (1)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12 (2)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (2)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (2)	ns

Notes to Table 53:

(1) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

(2) A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

FPP Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Arria V devices.

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP x16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Table 54 lists the DCLK-to-DATA[] ratio for each combination.

Table 54. DCLK-to-DATA[] Ratio for Arria V Devices

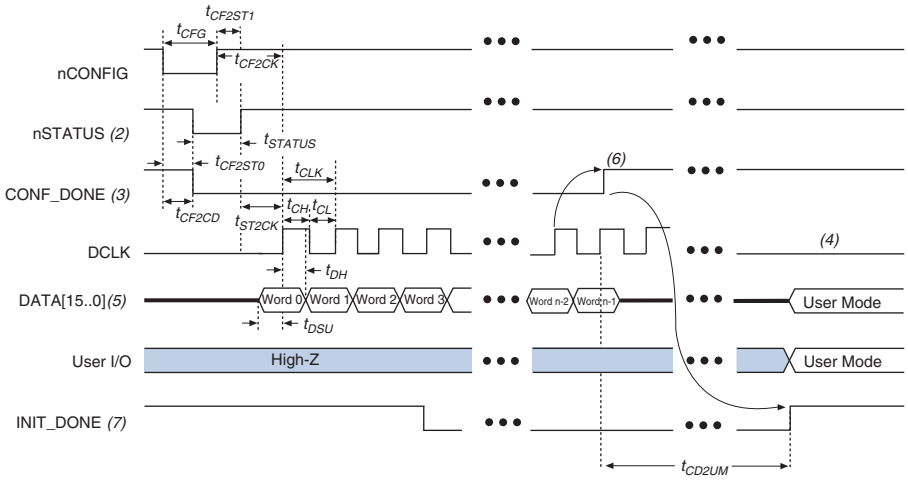
Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 20 shows the timing waveform for a FPP configuration when using a MAX® II device as an external host. This timing waveform shows timing when the DCLK-to-DATA[] ratio is 1.

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP x8 and FPP x16. For the respective DCLK-to-DATA[] ratio, refer to Table 54.

Figure 20. DCLK-to-DATA[] FPP Configuration Timing Waveform When the Ratio is 1 *(1)*



Notes to Figure 20:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Arria V device holds nSTATUS low for the time of the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) For FPP x16, use DATA[15..0]. For FPP x8, use DATA[7..0]. DATA[15..5] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(6) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high when the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 55 lists the timing parameters for Arria V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 55. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is 1

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (2)	µs
t_{CF2CK} (3)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK} (3)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	s
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP x8/ x16)	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (4)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 55:

(1) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

(2) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

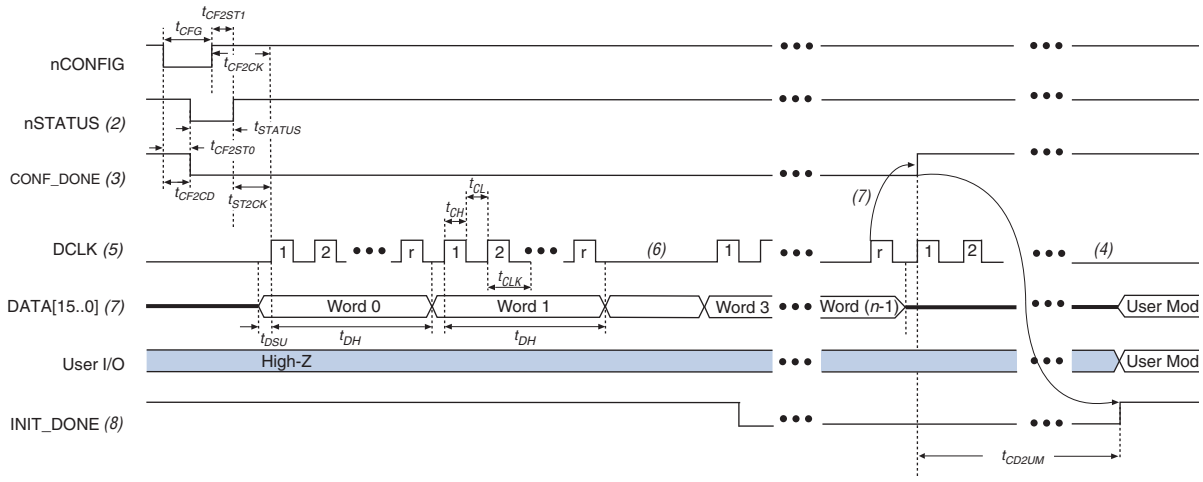
(3) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 21 shows the timing waveform for a FPP configuration when using a MAX II device or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

Figure 21. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 *(1)*



Notes to Figure 21:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Arria V device holds nSTATUS low for the time as specified by the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 54 on page 1–52.

(6) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[15..0] pins prior to sending the first DCLK rising edge.

(7) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high after the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 56 lists the timing parameters for Arria V devices when the DCLK-to-DATA[] ratio is more than 1.

Table 56. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is >1 (1)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (2)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (3)	µs
t_{CF2CK} (4)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK} (4)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	N – $1/f_{DCLK}$ (5)	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	s
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP x8/ x16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (6)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

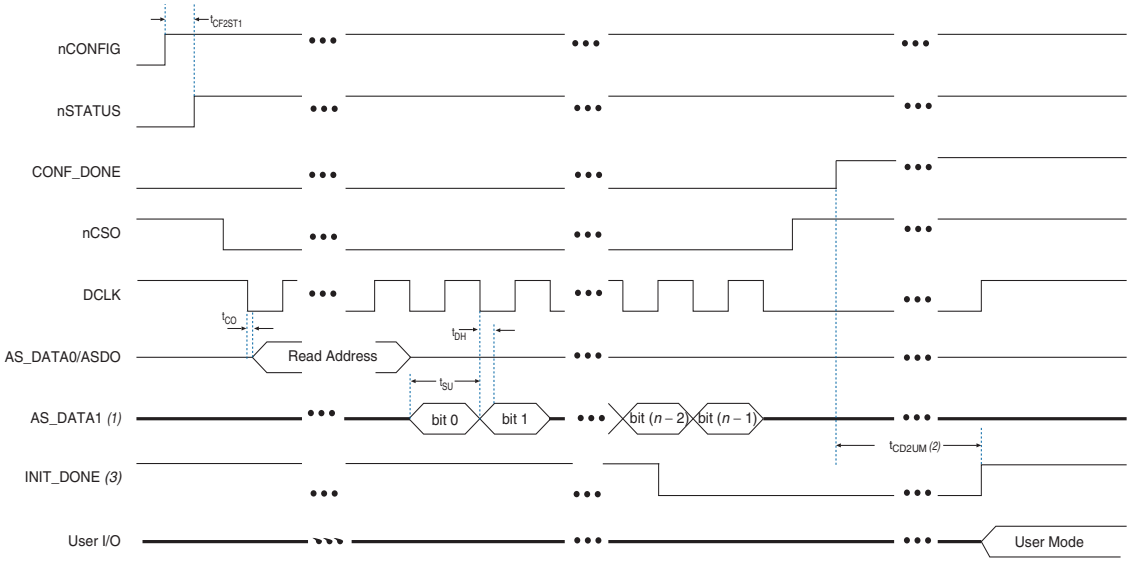
Notes to Table 56:

(1) Use these timing parameters when you use decompression and the design security features.
(2) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(3) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.
(4) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(5) N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.
(6) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

AS Configuration Timing

Figure 22 shows the timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Figure 22. AS Configuration Timing Waveform



Notes to Figure 22:

(1) If you are using AS x4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
(2) The initialization clock can be from the internal oscillator or CLKUSR pin.
(3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 57 lists the timing parameters for AS x1 and AS x4 configurations in Arria V devices.

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in Table 59 on page 1–59. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Table 57. AS Timing Parameters for AS x1 and x4 Configurations in Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	4	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}	Data hold time after the falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Table 58 lists the internal clock frequency specification for the AS configuration scheme.

The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

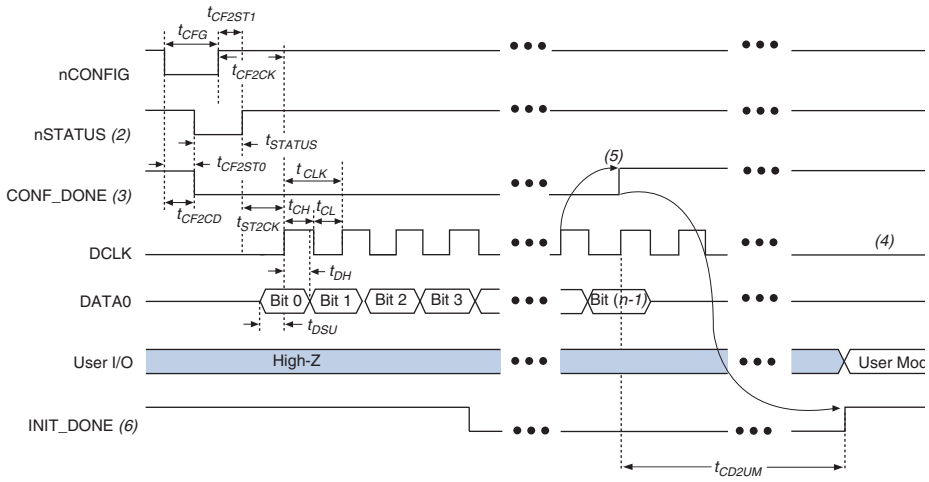
Table 58. DCLK Frequency Specification in the AS Configuration Scheme

Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	5.3	7.9	12.5	MHz
	10.6	15.7	25.0	MHz
	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz
Remote update only in AS mode	—	—	12.5	MHz

PS Configuration Timing

Figure 23 shows the timing waveform for a PS configuration when using a MAX II device or microprocessor as an external host.

Figure 23. PS Configuration Timing Waveform *(1)*



Notes to Figure 23:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Arria V device holds nSTATUS low for the time of the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high after the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(6) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 59 lists the PS timing parameter for Arria V devices.

Table 59. PS Timing Parameters for Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (2)	µs
t_{CF2CK} (3)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK} (3)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	s
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (4)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 59:

(1) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(2) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.
(3) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Initialization

Table 60 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency for Arria V devices.

Table 60. Initialization Clock Source Option and the Maximum Frequency for Arria V Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	T_{init}
CLKUSR (1)	PS and FPP	125	
	AS	100	

Note to Table 60:

(1) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Configuration Files

Use Table 61 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (**.hex**) or tabular text file (**.ttf**) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

Table 61 lists the uncompressed raw binary file (**.rbf**) sizes for Arria V devices.

Table 61. Uncompressed .rbf Sizes for Arria V Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GX	A1	71,015,552	439,960
	A3	71,015,552	439,960
	A5	101,740,640	446,360
	A7	101,740,640	446,360
	B1	137,784,928	457,368
	B3	137,784,928	457,368
	B5	185,915,648	463,128
	B7	185,915,648	463,128
Arria V GT	C3	71,015,552	439,960
	C7	101,740,640	446,360
	D3	137,784,928	457,368
	D7	185,915,648	463,128
Arria V SX	B3	185,903,520	450,968
	B5	185,903,520	450,968
Arria V ST	D3	185,903,520	450,968
	D5	185,903,520	450,968

Table 62 lists the minimum configuration time estimation for Arria V devices. The estimated values are based on the configuration **.rbf** sizes in Table 61.

Table 62. Minimum Configuration Time Estimation for Arria V Devices

Variant	Member Code	Active Serial (1)			Fast Passive Parallel (2)		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria V GX	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
	A7	4	100	255	16	125	51
	B1	4	100	344	16	125	69
	B3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
Arria V GT	C3	4	100	178	16	125	36
	C7	4	100	255	16	125	51
	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SX	B3	4	100	465	16	125	93
	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
	D5	4	100	465	16	125	93

Notes to Table 62:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Remote System Upgrades Circuitry Timing Specification

Table 63 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 63. Remote System Upgrade Circuitry Timing Specification (Part 1 of 2)

Parameter	Minimum	Maximum	Unit
$t_{MAX_RU_CLK}$ (1)	—	40	MHz
$t_{RU_nCONFIG}$ (2)	250	—	ns

Table 63. Remote System Upgrade Circuitry Timing Specification (Part 2 of 2)

Parameter	Minimum	Maximum	Unit
$t_{RU_nRSTIMER}$ (3)	250	—	ns

Notes to Table 63:

(1) This clock is user-supplied to the remote system upgrade circuitry. If you are using the ALTREMOTE_UPDATE megafunction, the clock user-supplied to the ALTREMOTE_UPDATE megafunction must meet this specification.

(2) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(3) This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

User Watchdog Internal Oscillator Frequency Specification

Table 64 lists the frequency specifications for the user watchdog internal oscillator.

Table 64. User Watchdog Internal Oscillator Frequency Specifications

Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

You can download the Excel-based I/O Timing spreadsheet from the Arria V Devices Documentation webpage.

Programmable IOE Delay

Table 65 lists the Arria V I/O element (IOE) programmable delay settings.

Table 65. IOE Programmable Delay for Arria V Devices

Parameter (1)	Available Settings	Minimum Offset (2)	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C4	–C5	–C6	–I3	–I5	
D1	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns
D3	8	0	1.763	1.795	2.999	3.496	3.571	3.031	3.643	ns
D4	32	0	0.508	0.518	0.869	1.063	1.063	1.063	1.057	ns
D5	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns

Notes to Table 65:

(1) You can set this value in the Quartus II software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 66 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Table 66. Programmable Output Buffer Delay

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Glossary

Table 67 lists the glossary for this datasheet.

Table 67. Glossary Table (Part 1 of 4)

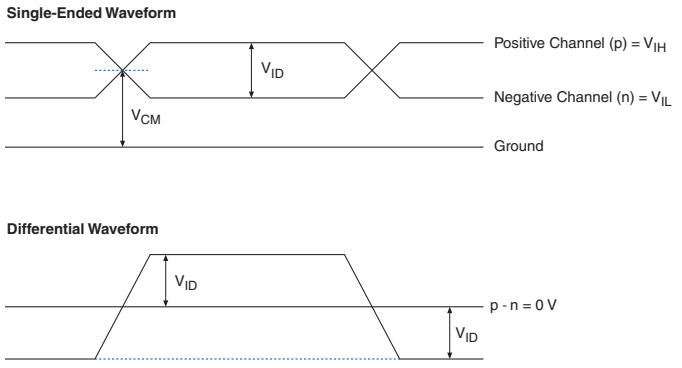
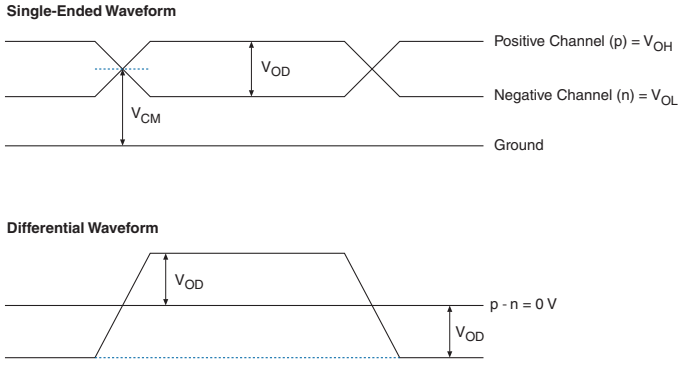
Letter	Subject	Definitions
A B C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms*  *Transmitter Output Waveforms* 
E	—	—
F	f_{HSCLK}	Left/right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G H I	—	—

Table 67. Glossary Table (Part 2 of 4)

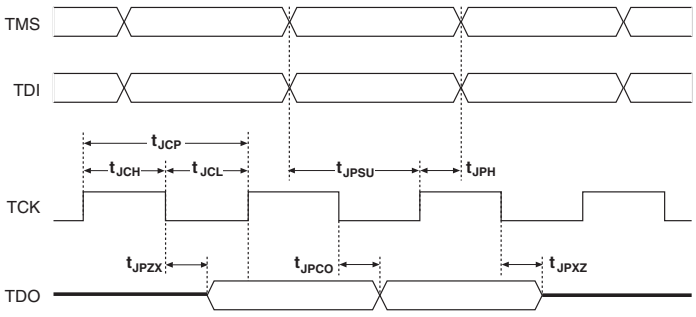
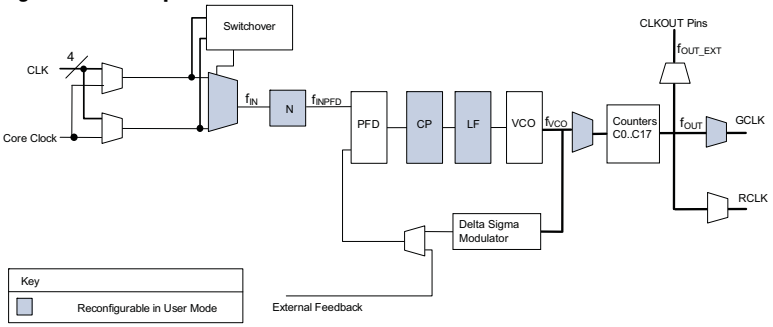
Letter	Subject	Definitions
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	JTAG Timing Specifications: 
K L M N O	—	—
P	**PLL Specifications**	**Diagram of PLL Specifications** *(1)*  **Note:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to the Arria V device).

Table 67. Glossary Table (Part 3 of 4)

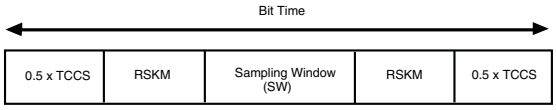
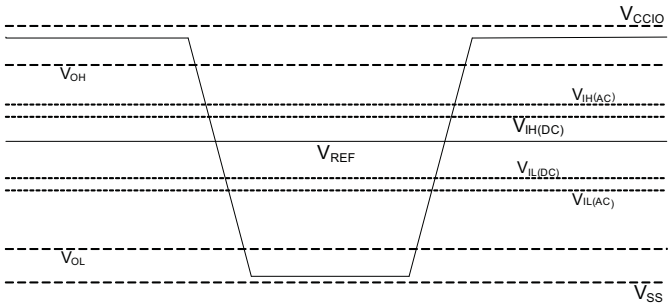
Letter	Subject	Definitions
S	**Sampling window (SW)**	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
	Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table).
	t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80–20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
	t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20–80%)
U	—	—

Table 67. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common mode input voltage.
	V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—Clock Boost Factor
X, Y, Z	—	—

Document Revision History

Table 68 lists the revision history for this document.

Table 68. Document Revision History (Part 1 of 2)

Date	Version	Changes
February 2014	3.7	■ Updated $V_{CCRSTCLK_HPS}$ maximum specification in Table 1. ■ Added $V_{CC_AUX_SHARED}$ specification in Table 1.
December 2013	3.6	■ Added "HPS PLL Specifications". ■ Added Table 24, Table 39, and Table 40. ■ Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. ■ Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. ■ Removed table: GPIO Pulse Width for Arria V Devices.
August 2013	3.5	■ Removed "Pending silicon characterization" note in Table 29. ■ Updated Table 25.
August 2013	3.4	■ Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64. ■ Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29.
June 2013	3.3	Updated Table 20, Table 21, Table 25, and Table 38.
May 2013	3.2	■ Added Table 37. ■ Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23. ■ Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64. ■ Updated industrial junction temperature range for –I3 speed grade in "PLL Specifications" section.
March 2013	3.1	■ Added HPS reset information in the "HPS Specifications" section. ■ Added Table 60. ■ Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59. ■ Updated Figure 21.

November 2012	3.0	■ Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.
		■ Removed table: Transceiver Block Jitter Specifications for Arria V Devices.
		■ Added HPS information:
		  ■ Added "HPS Specifications" section.
		  ■ Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.
		  ■ Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.
		  ■ Updated Table 3 and Table 5.

Table 68. Document Revision History (Part 2 of 2)

Date	Version	Changes
October 2012	2.4	■ Updated Arria V GX $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ minimum and maximum values, and data rate in Table 4. ■ Added receiver VICM (AC coupled) and VICM (DC coupled) values, and transmitter VOCM (AC coupled) and VOCM (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	■ Updated the SERDES factor condition in Table 30.
July 2012	2.2	■ Updated the maximum voltage for V_I (DC input voltage) in Table 1. ■ Updated Table 20 to include the Arria V GX -I3 speed grade. ■ Updated the minimum value of the `fixedclk` clock frequency in Table 20 and Table 21. ■ Updated the SERDES factor condition in Table 30. ■ Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ values in Table 4.
June 2012	2.0	Updated for the Quartus II software v12.0 release: ■ Restructured document. ■ Updated "Supply Current and Power Consumption" section. ■ Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52. ■ Added Table 22, Table 23, and Table 33. ■ Added Figure 1–1 and Figure 1–2. ■ Added "Initialization" and "Configuration Files" sections.
February 2012	1.3	■ Updated Table 2–1. ■ Updated Transceiver-FPGA Fabric Interface rows in Table 2–20. ■ Updated V_{CCP} description.
December 2011	1.2	■ Updated Table 2–1 and Table 2–3.
November 2011	1.1	■ Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. ■ Added Table 2–5. ■ Added Figure 2–4.
August 2011	1.0	Initial release.

Arria V GZ Device Datasheet

This document covers the electrical and switching characteristics for Arria® V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

For information regarding the densities and packages of devices in the Arria V GZ family, refer to the *Arria V Device Overview*.

Electrical Characteristics

The following sections describe the electrical characteristics of Arria V GZ devices.

Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in –3 (fastest) and –4 core speed grades. Industrial devices are offered in –3L and –4 core speed grades. Arria V GZ devices are offered in –2 and –3 transceiver speed grades.

Table 1 lists the industrial and commercial speed grades for the Arria V GZ devices.

Table 1. Commercial and Industrial Speed Grade Offering for Arria V GZ Devices *(1), (2), (3)*

Transceiver Speed Grade	Core Speed Grade			
	C3	C4	I3L	I4
2	Yes	—	Yes	—
3	—	Yes	—	Yes

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.
(2) Lower number refers to faster speed grade.
(3) L = Low power devices.

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Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Conditions other than those listed in Table 2 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2. Absolute Maximum Ratings for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Power supply for core voltage and periphery circuitry	–0.5	1.35	V
V_{CCPT}	Power supply for programmable power technology	–0.5	1.8	V
V_{CCPGM}	Power supply for configuration pins	–0.5	3.9	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	–0.5	3.4	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.9	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.9	V
V_{CCIO}	I/O power supply	–0.5	3.9	V
V_{CCD_FPLL}	PLL digital power supply	–0.5	1.8	V
V_{CCA_FPLL}	PLL analog power supply	–0.5	3.4	V
V_I	DC input voltage	–0.5	3.8	V
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (No bias)	–65	150	°C
I_{OUT}	DC output current per pin	–25	40	mA

Table 3 lists the absolute conditions for the transceiver power supply for Arria V GZ devices.

Table 3. Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	–0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	–0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	–0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	–0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	–0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	–0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	–0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	–0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	–0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	–0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	–0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 4 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 4 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Table 4. Maximum Allowed Overshoot During Transitions for Arria V GZ Devices

Symbol	Description	Condition (V)	Overshoot Duration as % @ T_J = 100°C	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Arria V GZ devices.

Table 5 lists the steady-state voltage and current values expected from Arria V GZ devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 5. Recommended Operating Conditions for Arria V GZ Devices

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply (3)	—	0.82	0.85	0.88	V
V_{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPD} (1)	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V_{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Notes to Table 5:

(1) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

(2) If you do not use the design security feature in Arria V GZ devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V_{CCBAT}. Arria V GZ devices do not exit POR if V_{CCBAT} is not powered up.

(3) The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Table 6 lists the transceiver power supply recommended operating conditions for Arria V GZ devices.

Table 6. Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_GXBL} (1), (3)	Transceiver channel PLL power supply (left side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V_{CCA_GXBR} (1), (3)	Transceiver channel PLL power supply (right side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V
V_{CCR_GXBL} (2)	Receiver analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCR_GXBR} (2)	Receiver analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCT_GXBL} (2)	Transmitter analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCT_GXBR} (2)	Transmitter analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V

Notes to Table 6:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

(3) When using ATX PLLs, the supply must be 3.0 V.

Table 7 shows the transceiver power supply voltage requirements for various conditions.

Table 7. Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB (2)	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: ■ Data rate > 10.3 Gbps. ■ DFE is used.	1.05	3.0	1.5	V
If ANY of the following conditions are true (1): ■ ATX PLL is used. ■ Data rate > 6.5Gbps. ■ DFE (data rate ≤10.3 Gbps), AEQ, or EyeQ feature is used.	1.0			
If ALL of the following conditions are true: ■ ATX PLL is not used. ■ Data rate <= 6.5Gbps. ■ DFE, AEQ, and EyeQ are not used.	0.85	2.5		

Notes to Table 7:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the following specifications:

- Supply Current
- I/O Pin Leakage Current
- Bus Hold Specifications
- On-Chip Termination (OCT) Specifications
- Pin Capacitance
- Hot Socketing

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 8 lists the Arria V GZ I/O pin leakage current specifications.

Table 8. I/O Pin Leakage Current for Arria V GZ Devices (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Note to Table 8:

(1) If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

Bus Hold Specifications

Table 9 lists the Arria V GZ device family bus hold specifications.

Table 9. Bus Hold Parameters for Arria V GZ Devices

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	–22.5	—	–25.0	—	–30.0	—	–50.0	—	–70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	–120	—	–160	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

Table 10 lists the Arria V GZ OCT termination calibration accuracy specifications.

Table 10. OCT Calibration Accuracy Specifications for Arria V GZ Devices (1) (Part 1 of 2)

Symbol	Description	Conditions	Calibration Accuracy		Unit
			C3, I3L	C4, I4	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Table 10. OCT Calibration Accuracy Specifications for Arria V GZ Devices (1) (Part 2 of 2)

Symbol	Description	Conditions	Calibration Accuracy		Unit
			C3, I3L	C4, I4	
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2 V	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25 V	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	%
25-Ω $R_{S_left_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S_left_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Note to Table 10:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 11 lists the Arria V GZ OCT without calibration resistance tolerance to PVT changes.

Table 11. OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R, 50-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5 V	±25	±25	%

Table 12 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 12 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without re-calibration.

Equation 1. OCT Variation Without Re-Calibration for Arria V GZ Devices (1), (2), (3), (4), (5), (6)

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle\right)$$

Notes to Equation 1:

(1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 12 lists the on-chip termination variation after power-up calibration.

Table 12. OCT Variation after Power-Up Calibration for Arria V GZ Devices (1)

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 12:

(1) Valid for a V_{CCIO} range of ±5% and a temperature range of 0° to 85°C.

Pin Capacitance

Table 13 lists the Arria V GZ pin capacitance.

Table 13. Pin Capacitance for Arria V GZ Devices

Symbol	Description	Value	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 14 lists the hot socketing specifications for Arria V GZ devices.

Table 14. Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver pin	50 mA

Note to Table 14:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 15 lists the weak pull-up resistor values for Arria V GZ devices.

Table 15. Internal Weak Pull-Up Resistor for Arria V GZ Devices (1), (2)

Symbol	Description	V_{CCIO} Conditions (V) (3)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 15:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 16 through Table 21 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria V GZ devices. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 16 through Table 21, refer to "Glossary" on page 48.

Table 16. Single-Ended I/O Standards for Arria V GZ Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1

Table 16. Single-Ended I/O Standards for Arria V GZ Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Table 17. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × VCCIO	0.51 × V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × VCCIO	0.51 × V_{CCIO}
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × VCCIO	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V GZ Devices (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{oi} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V GZ Devices (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-125 Class I, II	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-12 Class I, II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Table 19. Differential SSTL I/O Standards for Arria V GZ Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	*(1)*	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	*(1)*	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	2($V_{IH(AC)}$ - V_{REF})	2($V_{IL(AC)}$ - V_{REF})
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	*(1)*	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	2($V_{IH(AC)}$ - V_{REF})	—

Table 19. Differential SSTL I/O Standards for Arria V GZ Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	V_{REF} –0.15	$V_{CCIO}/2$	V_{REF} + 0.15	–0.30	0.30

Notes to Table 19:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 20. Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.44	0.44

Table 21. Differential I/O Standard Specifications for Arria V GZ Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V) (9)			V_{ID} (mV) (7)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (6)			V_{OCM} (V) (6)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 22 on page 15.														
2.5 V LVDS (1)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	$D_{MAX} \leq$ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} >$ 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS (5)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO) (2)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (3)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4

Table 21. Differential I/O Standard Specifications for Arria V GZ Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V) (9)			V_{ID} (mV) (7)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (6)			V_{OCM} (V) (6)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (8), (4)	2.375	2.5	2.625	300	—	—	0.6	$D_{MAX} \leq$ 700 Mbps	1.8	—	—	—	—	—	—
	2.375	2.5	2.625	300	—	—	1	$D_{MAX} >$ 700 Mbps	1.6	—	—	—	—	—	—

Notes to Table 21:

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

(6) RL range: 90 ≤RL ≤110 Ω.

(7) The minimum VID value is applicable over the entire common mode range, VCM.

(8) LVPECL is only supported on dedicated clock input pins.

(9) Differential inputs are powered by VCCPD which requires 2.5 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Arria V GZ core and periphery blocks.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 22 lists the Arria V GZ transceiver specifications.

Table 22. Transceiver Specifications for Arria V GZ Devices (1) (Part 1 of 5)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) (7)	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) (7)	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled)	Dedicated reference clock pin	1000/900/850 (2)			1000/900/850 (2)			mV
	RX reference clock pin	1.0/0.9/0.85 (3)			1.0/0.9/0.85 (3)			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

Table 22. Transceiver Specifications for Arria V GZ Devices (1) (Part 2 of 5)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise (622 MHz) (18)	100 Hz	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) (15)	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	ps (rms)
R_{REF}	—	—	1800 ±1%	—	—	1800 ±1%	—	Ω
Transceiver Clocks								
`fixedclk` clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (`mgmt_clk_clk`) frequency	—	100	—	125	100	—	125	MHz
Receiver								
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (Standard PCS) (8), (19)	—	600	—	9900	600	—	8800	Mbps
Data rate (10G PCS) (8), (19)	—	600	—	12500	600	—	10312.5	Mbps
Absolute V_{MAX} for a receiver pin (4)	—	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (16)	V_{CCR_GXB} = 1.0 V (V_{ICM} = 0.75 V)	—	—	1.8	—	—	1.8	V
	V_{CCR_GXB} = 0.85 V (V_{ICM} = 0.6 V)	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins (5)	—	85	—	—	85	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 30%	—	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	—	100 ± 30%	—	Ω
	120-Ω setting	—	120 ± 30%	—	—	120 ± 30%	—	Ω
	150-Ω setting	—	150 ± 30%	—	—	150 ± 30%	—	Ω

Table 22. Transceiver Specifications for Arria V GZ Devices (1) (Part 3 of 5)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{ICM} (AC and DC coupled)	V_{CCR_GXB} = 0.85 V full bandwidth	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 0.85 V half bandwidth	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 1.0 V full bandwidth	—	700	—	—	700	—	mV
	V_{CCR_GXB} = 1.0 V half bandwidth	—	700	—	—	700	—	mV
t_{LTR} (9)	—	—	—	10	—	—	10	µs
t_{LTD} (10)	—	4	—	—	4	—	—	µs
t_{LTD_manual} (11)	—	4	—	—	4	—	—	µs
$t_{LTR_LTD_manual}$ (12)	—	15	—	—	15	—	—	µs
CDR PPM Tolerance	Data rate: 600 Mbps to 1 Gbps	—	—	300	—	—	100	± PPM
	Data rate: 1 Gbps to 6 Gbps	—	—	300	—	—	100	
	Data rate: ≥ 6 Gbps	—	—	300	—	—	100	
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	dB
Programmable DC gain	DC gain setting = 0	—	0	—	—	0	—	dB
	DC gain setting = 1	—	2	—	—	2	—	dB
	DC gain setting = 2	—	4	—	—	4	—	dB
	DC gain setting = 3	—	6	—	—	6	—	dB
	DC gain setting = 4	—	8	—	—	8	—	dB
Transmitter								
Supported I/O Standards	1.4-V and 1.5-V PCML							
Data rate (Standard PCS)	—	600	—	9900	600	—	8800	Mbps
Data rate (10G PCS)	—	600	—	12500	600	—	10312.5	Mbps
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	—	100 ± 20%	—	Ω
	120-Ω setting	—	120 ± 20%	—	—	120 ± 20%	—	Ω
	150-Ω setting	—	150 ± 20%	—	—	150 ± 20%	—	Ω
V_{OCM} (AC coupled)	0.65-V setting	—	650	—	—	650	—	mV

Table 22. Transceiver Specifications for Arria V GZ Devices (1) (Part 4 of 5)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{OCM} (DC coupled)	<=6.5 Gbps	—	650	—	—	650	—	mV
	>6.5 Gbps	—	650	—	—	650	—	mV
Rise time (6)	—	30	—	160	30	—	160	ps
Fall time (6)	—	30	—	160	30	—	160	ps
Intra-differential pair skew	Tx V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode	—	—	500	—	—	500	ps
CMU PLL								
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{pll_powerdown}$ (13)	—	1	—	—	1	—	—	µs
t_{pll_lock} (14)	—		—	10	—	—	10	µs
ATX PLL								
Supported data range	VCO post-divider L = 2	8000	—	12500	8000	—	10312.5	Mbps
	L = 4	4000	—	6600	4000	—	6600	Mbps
	L = 8 (17)	1000	—	3300	1000	—	3300	Mbps
$t_{pll_powerdown}$ (13)	—	1	—	—	1	—	—	µs
t_{pll_lock} (14)	—	—	—	10	—	—	10	µs
fPLL								
Supported data range	—	600	—	3250	600	—	3250	Mbps
$t_{pll_powerdown}$ (13)	—	1	—	—	1	—	—	µs

Table 22. Transceiver Specifications for Arria V GZ Devices (1) (Part 5 of 5)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} (14)	—	—	—	10		—	10	µs

Notes to Table 22:

(1) Speed grades shown in Table 22 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) This supply follows VCCR_GXB.

(4) The device cannot tolerate prolonged operation at this absolute maximum.

(5) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(6) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(7) The input reference clock frequency options depend on the data rate and the device speed grade.

(8) The line data rate may be limited by PCS-FPGA interface speed grade.

(9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(13) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.

(14) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(17) This clock can be further divided by central or local clock dividers making it possible to use ATX PLL for data rates < 1 Gbps. For more information about ATX PLLs, refer to the *Transceiver Clocking in Arria V Devices* chapter and the *Dynamic Reconfiguration in Arria V Devices* chapter.

(18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(19) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 23 shows the maximum transmitter data rate for the clock network.

Table 23. Clock Network Maximum Data Rate Transmitter Specifications (1) (Part 1 of 2)

Clock Network	ATX PLL			CMU PLL (2)			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 (3)	12.5	—	6	12.5	—	6	3.125	—	3
x6 (3)	—	12.5	6	—	12.5	6	—	3.125	6
x6 PLL Feedback (4)	—	12.5	Side-wide	—	12.5	Side-wide	—	—	—
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—

Table 23. Clock Network Maximum Data Rate Transmitter Specifications (1) (Part 2 of 2)

Clock Network	ATX PLL			CMU PLL (2)			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

Notes to Table 23:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 24 shows the approximate maximum data rate using the standard PCS.

Table 24. Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices (2)

Mode (1)	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	2	C3, I3L core speed grade	9.9	9	7.84	7.2	5.3	4.7	4.24	3.76
	3	C4, I4 core speed grade	8.8	8.2	7.2	6.56	4.8	4.3	3.84	3.44
Register	2	C3, I3L core speed grade	9.9	9	7.92	7.2	4.9	4.,5	3.92	3.6
	3	C4, I4 core speed grade	8.8	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Notes to Table 24:

(1) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(2) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 on page 1 for the transceiver speed grade.

Table 25 shows the approximate maximum data rate using the 10G PCS

Table 25. 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices

Mode (1)	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	64	66/67	50	40	64/66/67	32
FIFO	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92
Register	2	C3,I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92

Note to Table 25:

(1) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 26 shows the VOD settings for the Arria V GZ channel.

Table 26. Typical V_{OD} Setting for Arria V GZ Channel, TX Termination = 100 Ω (2)

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} differential peak to peak typical	0 (1)	0	32	640
	1 (1)	20	33	660
	2 (1)	40	34	680
	3 (1)	60	35	700
	4 (1)	80	36	720
	5 (1)	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

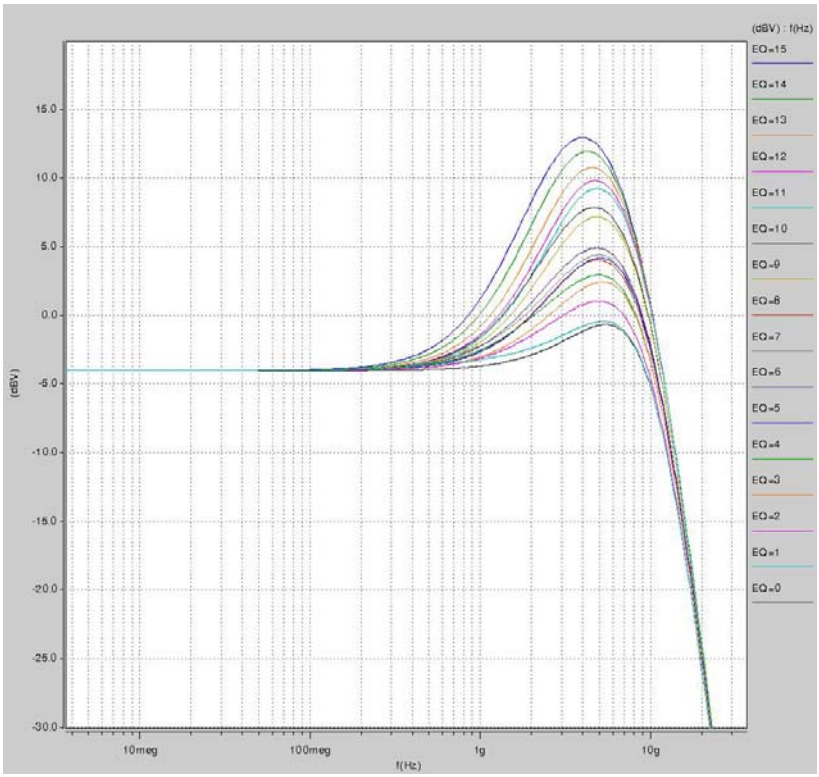
Notes to Table 26:

(1) If TX termination resistance = 100Ω, this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

Figure 1 shows the AC gain curves for Arria V GZ channels.

Figure 1. AC Gain Curves for Arria V GZ Channels (full bandwidth)



Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 27 lists the clock tree specifications for Arria V GZ devices.

Table 27. Clock Tree Performance for Arria V GZ Devices

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

PLL Specifications

Table 28 lists the Arria V GZ PLL block performance specifications.

Table 28. PLL Specifications for Arria V GZ Devices (Part 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} (1)	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
f_{VCO} (9)	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT} (2)	Output frequency for an internal global or regional clock (C3, I3L speed grade)	—	—	650	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grade)	—	—	580	MHz
f_{OUT_EXT} (2)	Output frequency for an external clock output (C3, I3L speed grade)	—	—	667	MHz
	Output frequency for an external clock output (C4, I4 speed grade)	—	—	533	MHz
$t_{OUTDUTY}$	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	100	MHz
t_{LOCK}	Time required to lock from the end-of-device configuration or deassertion of `areset`	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} (3), (4)	Input clock cycle-to-cycle jitter ($f_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($f_{REF} < 100$ MHz)	-750	—	+750	ps (p-p)
t_{OUTPJ_DC} (5)	Period Jitter for dedicated clock output in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output in integer PLL ($f_{OUT} < 100$ Mhz)	—	—	17.5	mUI (p-p)
t_{FOUTPJ_DC} (5)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	250 (10), 175 (11)	ps (p-p)
	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	25 (10), 17.5 (11)	mUI (p-p)

Table 28. PLL Specifications for Arria V GZ Devices (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{OUTCCJ_DC} (5)	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{FOUTCCJ_DC}$ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	250 (10), 175 (11)	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	25 (10), 17.5 (11)	mUI (p-p)
t_{OUTPJ_IO} (5), (8)	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{FOUTPJ_IO} (5), (8), (10)	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (5), (8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{FOUTCCJ_IO}$ (5), (8), (10)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC_OUTPJ_DC}$ (5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLS ($f_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k_{VALUE}	Numerator of Fraction	128	8388608	2147483648	—

Table 28. PLL Specifications for Arria V GZ Devices (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{RES}	Resolution of VCO frequency (f_{INPFD} = 100 MHz)	390625	5.96	0.023	Hz

Notes to Table 28:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(4) The f_{REF} is fIN/N specification applies when N = 1.

(5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 41 on page 35.

(6) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59Mhz ≤Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(7) High bandwidth PLL settings are not supported in external feedback mode.

(8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 39 on page 33.

(9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(10) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(11) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

DSP Block Specifications

Table 29 lists the Arria V GZ DSP block performance specifications.

Table 29. DSP Block Performance Specifications for Arria V GZ Devices (Part 1 of 2)

Mode	Performance			Unit
	C3, I3L	C4	I4	
Modes using One DSP Block				
Three 9 × 9	480	420		MHz
One 18 × 18	480	420	400	MHz
Two partial 18 × 18 (or 16 × 16)	480	420	400	MHz
One 27 × 27	400	350		MHz
One 36 × 18	400	350		MHz
One sum of two 18 × 18 (One sum of two 16 × 16)	400	350		MHz
One sum of square	400	350		MHz
One 18 × 18 plus 36 (a × b) + c	400	350		MHz
Modes using Two DSP Blocks				
Three 18 × 18	400	350		MHz
One sum of four 18 × 18	380	300		MHz
One sum of two 27 × 27	380	300	290	MHz
One sum of two 36 × 18	380	300		MHz
One complex 18 × 18	400	350		MHz
One 36 × 36	380	300		MHz
Modes using Three DSP Blocks				
One complex 18 × 25	340	275	265	MHz

Table 29. DSP Block Performance Specifications for Arria V GZ Devices (Part 2 of 2)

Mode	Performance			Unit
	C3, I3L	C4	I4	
Modes using Four DSP Blocks				
One complex 27 × 27	350	310		MHz

Memory Block Specifications

Table 30 lists the Arria V GZ memory block specifications.

Table 30. Memory Block Performance Specifications for Arria V GZ Devices (1), (2)

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Memory	C3	C4	I3L	I4	
MLAB	Single port, all supported widths	0	1	400	315	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth (3)	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz
M20K Block	Single-port, all supported widths	0	1	650	550	500	450	MHz
	Simple dual-port, all supported widths	0	1	650	550	500	450	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	455	400	455	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	400	350	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	500	450	500	450	MHz
	True dual port, all supported widths	0	1	650	550	500	450	MHz
	ROM, all supported widths	0	1	650	550	500	450	MHz

Notes to Table 30:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 31 lists the internal temperature sensing diode (TSD) specification.

Table 31. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40°C to 100°C	±8°C	No	1 MHz, 500 kHz	< 100 ms	8 bits	8 bits

Table 32 lists the specifications for the Arria V GZ external temperature sensing diode.

Table 32. External Temperature Sensing Diode Specifications for Arria V GZ Devices

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	8	—	200	µA
$V_{bias,}$ voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 33 lists high-speed I/O timing for Arria V GZ devices.

Table 33. High-Speed I/O Specifications for Arria V GZ Devices (1), (2) (Part 1 of 3)

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (4)	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (3)	Clock boost factor W = 1 to 40 (4)	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (4)	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	625 (5)	5	—	525 (5)	MHz

Table 33. High-Speed I/O Specifications for Arria V GZ Devices (1), (2) (Part 2 of 3)

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter								
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (9), (10)	(6)	—	1250	(6)	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16)	(6)	—	1600	(6)	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (11)	SERDES factor J = 4 to 10	(6)	—	840	(6)	—	840	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	ps

Table 33. High-Speed I/O Specifications for Arria V GZ Devices (1), (2) (Part 3 of 3)

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Receiver								
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 (10), (12), (13), (14), (15), (16)	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16)	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(6)	—	(8)	(6)	—	(8)	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	Mbps
DPA Mode								
DPA run length	—	—	—	10000	—	—	10000	UI
Soft CDR mode								
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm
Non DPA Mode								
Sampling Window	—	—	—	300	—	—	300	ps

Notes to Table 33:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(11) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(12) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

(13) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

Figure 2 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 2. DPA Lock Time Specification with DPA PLL Calibration Enabled

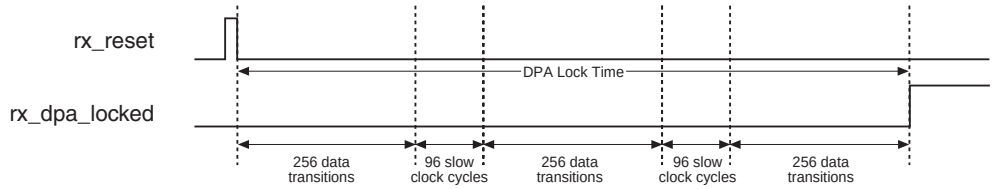


Table 34 lists the DPA lock time specifications for Arria V GZ devices.

Table 34. DPA Lock Time Specifications for Arria V GZ Devices *(1), (2), (3)*

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions *(4)*	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 34:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in this table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 3 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps

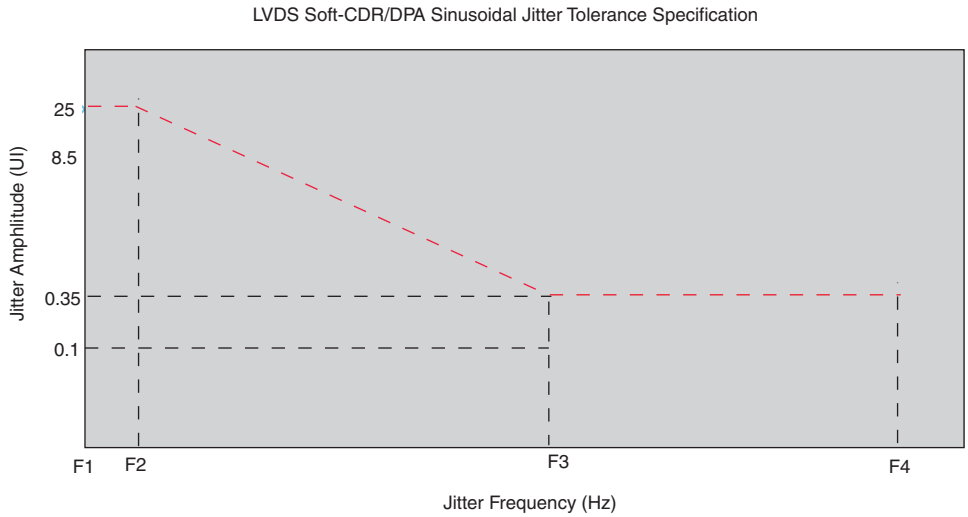


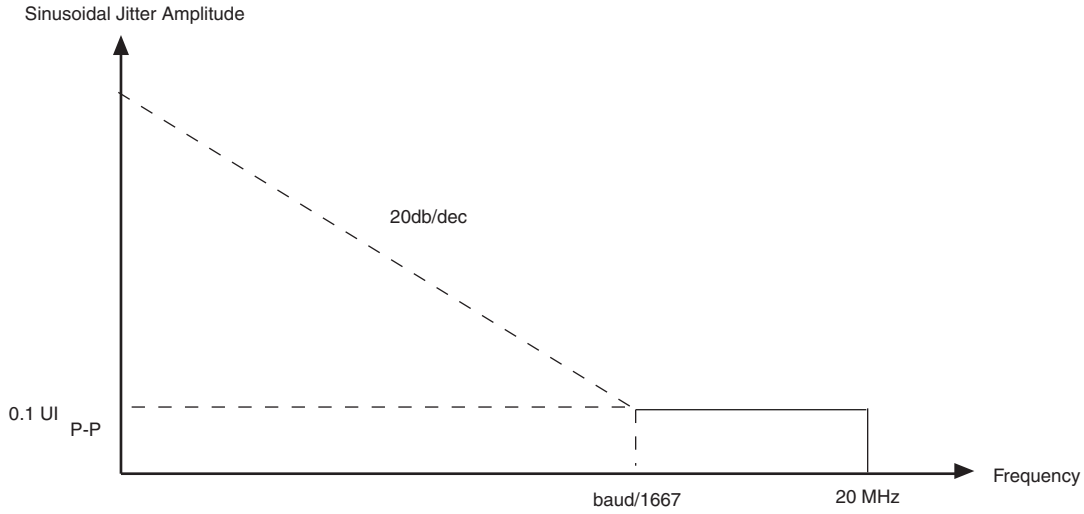
Table 35 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Table 35. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 4 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 36 lists the DLL range specification for Arria V GZ devices. The DLL is always in 8-tap mode in Arria V GZ devices.

Table 36. DLL Range Specifications for Arria V GZ Devices *(1)*

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 – 890	300 – 890	MHz

Note to Table 36:

(1) Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 37 lists the DQS phase offset delay per stage for Arria V GZ devices.

Table 37. DQS Phase Offset Delay Per Setting for Arria V GZ Devices (1), (2)

Speed Grade	Min	Max	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

Notes to Table 37:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 11 ps) ± 20 ps] = 735 ps ± 20 ps.

Table 38 lists the DQS phase shift error for Arria V GZ devices.

Table 38. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V GZ Devices (1)

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps
4	120	128	ps

Note to Table 38:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is ±84 ps or ±42 ps.

Table 39 lists the memory output clock jitter specifications for Arria V GZ devices.

Table 39. Memory Output Clock Jitter Specification for Arria V GZ Devices (1), (2), (3) (Part 1 of 2)

Clock Network	Parameter	Symbol	C3, I3L		C4, I4		Unit
			Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	–55	55	–55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–110	110	–110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–82.5	82.5	–82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	–82.5	82.5	–82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–165	165	–165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–90	90	–90	90	ps

Table 39. Memory Output Clock Jitter Specification for Arria V GZ Devices (1), (2), (3) (Part 2 of 2)

Clock Network	Parameter	Symbol	C3, I3L		C4, I4		Unit
			Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	–30	30	–35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–60	60	–70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–45	45	–56	56	ps

Notes to Table 39:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

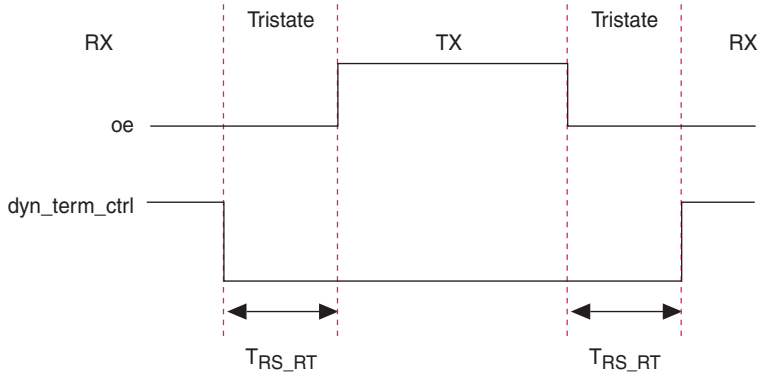
Table 40 lists the OCT calibration block specifications for Arria V GZ devices.

Table 40. OCT Calibration Block Specifications for Arria V GZ Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 5)	—	2.5	—	ns

Figure 5 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

Figure 5. Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 41 lists the worst-case DCD for Arria V GZ devices.

Table 41. Worst-Case DCD on Arria V GZ I/O Pins (1)

Symbol	C3, I3L		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

Note to Table 41:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

This section provides configuration specifications and timing for Arria V GZ devices.

POR Specifications

Table 42 lists the specifications for fast and standard POR for Arria V GZ devices.

Table 42. Fast and Standard POR Delay Specification for Arria V GZ Devices (1)

POR Delay	Minimum (ms)	Maximum (ms)
Fast	4	12 (2)
Standard	100	300

Notes to Table 42:

(1) Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter

(2) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

JTAG Configuration Specifications

Table 43 lists the JTAG timing parameters and values for Arria V GZ devices.

Table 43. JTAG Timing Parameters and Values for Arria V GZ Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCP}	TCK clock period	167 (1)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (2)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (2)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (2)	ns

Notes to Table 43:

(1) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

(2) A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

FPP Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Arria V GZ devices.

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Table 44 lists the DCLK-to-DATA[] ratio for each combination.

Table 44. DCLK-to-DATA[] Ratio for Arria V GZ Devices *(1)*

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4
FPP ×32	Disabled	Disabled	1
	Disabled	Enabled	4
	Enabled	Disabled	8
	Enabled	Enabled	8

Note to Table 44:

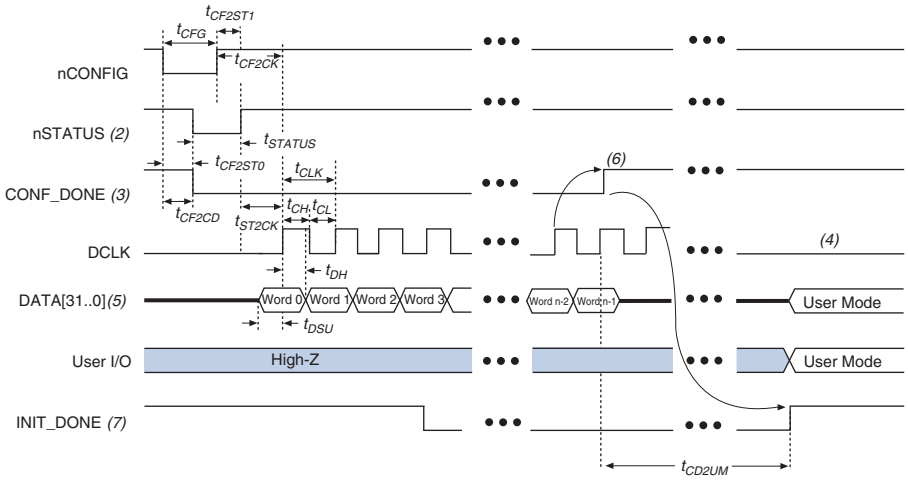
(1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Arria V GZ devices use the additional clock cycles to decrypt and decompress the configuration data.

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 6 shows the timing waveform for FPP configuration when using a MAX® II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.

When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to Table 44.

Figure 6. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 *(1)*



Notes to Figure 6:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.

(3) After power-up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) For FPP ×16, use DATA[15..0]. For FPP ×8, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(6) To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 45 lists the timing parameters for Arria V GZ devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 45. FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1 *(1)*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 *(3)*	µs
t_{CF2CK} *(6)*	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} *(6)*	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode *(4)*	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (17,408 × CLKUSR period) *(5)*	—	—

Notes to Table 45:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

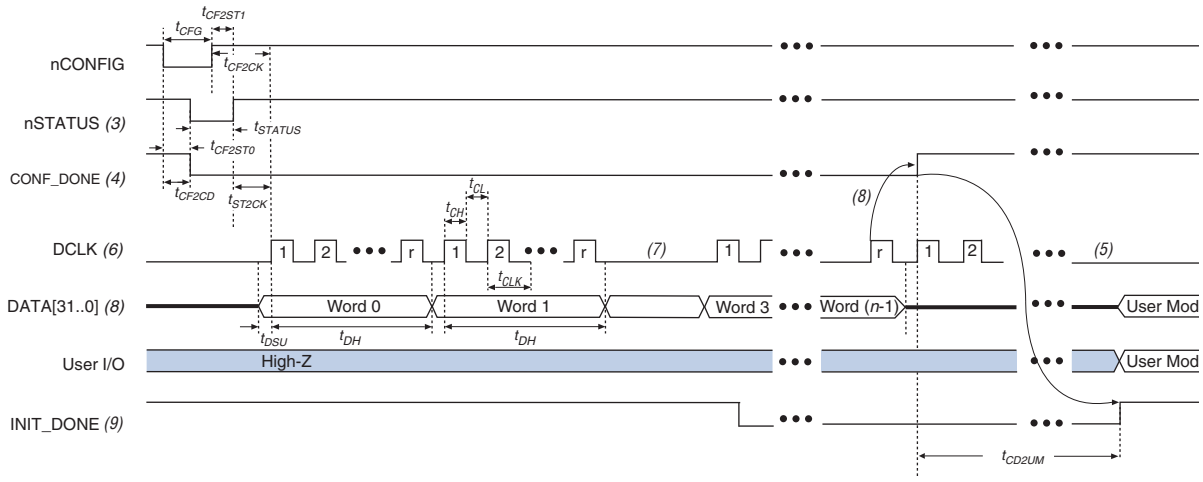
(5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 7 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

Figure 7. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 *(1), (2)*



Notes to Figure 7:

(1) To find out the DCLK-to-DATA[] ratio for your system, refer to Table 44 on page 37.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.

(4) After power-up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 44 on page 37.

(7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.

(8) To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 46 lists the timing parameters for Arria V GZ devices for FPP configuration when the DCLK-to-DATA[] ratio is more than 1.

Table 46. FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1 *(1)*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 *(3)*	µs
t_{CF2CK} *(7)*	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} *(7)*	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	N–1/f_{DCLK} *(4)*	—	s
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode *(5)*	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (17,408 × CLKUSR period) *(6)*	—	—

Notes to Table 46:

(1) Use these timing parameters when you use the decompression and design security features.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(4) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

(5) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

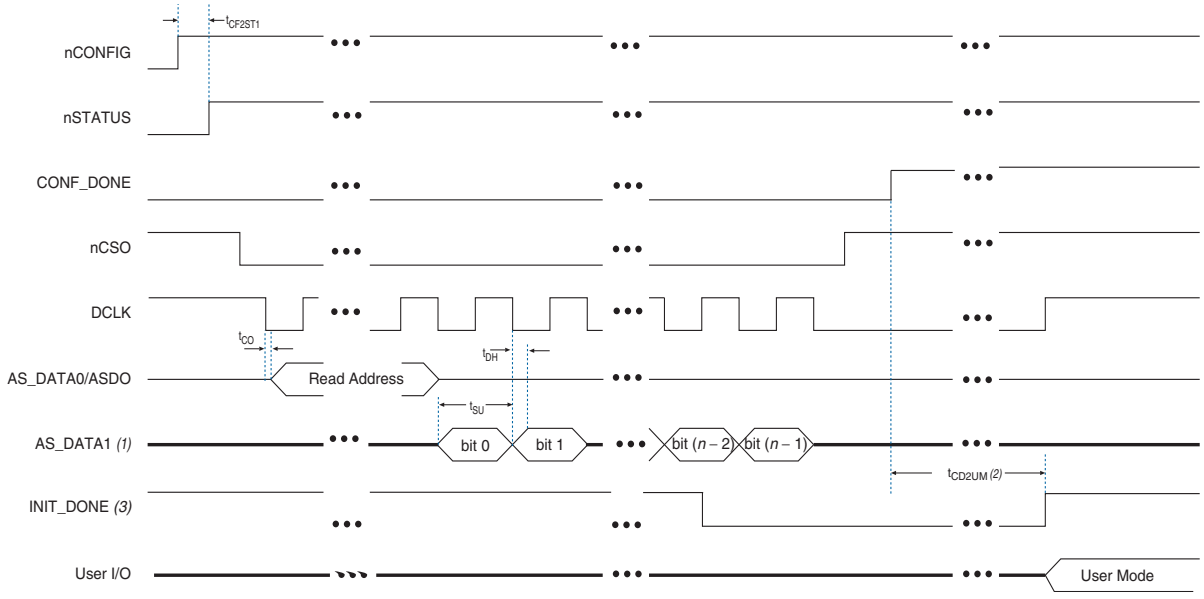
(6) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(7) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Active Serial Configuration Timing

Figure 8 shows the timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Figure 8. AS Configuration Timing



Notes to Figure 8:

(1) If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
(2) The initialization clock can be from internal oscillator or CLKUSR pin.
(3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 47 lists the timing parameters for AS x1 and AS x4 configurations in Arria V GZ devices.

Table 47. AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices (1), (2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	4	ns
t_{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t_{H}	Data hold time after falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (17,408 × CLKUSR period)	—	—

Notes to Table 47:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
(2) t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 49 on page 44.
(3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Table 48 lists the internal clock frequency specification for the AS configuration scheme.

Table 48. DCLK Frequency Specification in the AS Configuration Scheme (1), (2)

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 48:

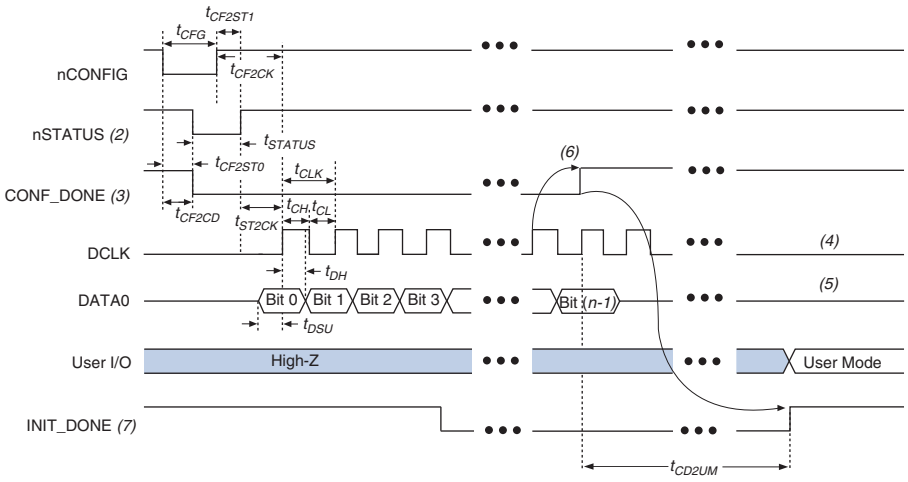
(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Passive Serial Configuration Timing

Figure 9 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 9. PS Configuration Timing Waveform (1)



Notes to Figure 9:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.

(3) After power-up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.

(6) To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 49 lists the PS configuration timing parameters for Arria V GZ devices.

Table 49. PS Timing Parameters for Arria V GZ Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (2)	µs
t_{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (17,408 × CLKUSR period) (4)	—	—

Notes to Table 49:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 50 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 50. Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, FPP	12.5	17,408
CLKUSR (1)	PS, FPP	125	
	AS	100	

Note to Table 50:

(1) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Configuration Files

Use Table 51 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (**.hex**) or tabular text file (**.ttf**) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

Table 51 lists the uncompressed raw binary file (**.rbf**) sizes for Arria V GZ devices.

Table 51. Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GZ	E1	137,598,720	562,208
	E3	137,598,720	562,208
	E5	213,798,720	561,760
	E7	213,798,720	561,760

Table 52 lists the minimum configuration time estimates for Arria V GZ devices.

Table 52. Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial (1)			Fast Passive Parallel (2)		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Notes to Table 52:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Remote System Upgrades Circuitry Timing Specification

Table 53 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 53. Remote System Upgrade Circuitry Timing Specifications (Part 1 of 2)

Parameter	Minimum	Maximum	Unit
$f_{MAX_RU_CLK}$ (1)	—	40	MHz
$t_{RU_nCONFIG}$ (2)	250	—	ns

Table 53. Remote System Upgrade Circuitry Timing Specifications (Part 2 of 2)

Parameter	Minimum	Maximum	Unit
$t_{RU_nRSTIMER}$ (3)	250	—	ns

Notes to Table 53:

(1) This clock is user-supplied to the remote system upgrade circuitry. If you are using the ALTREMOTE_UPDATE megafunction, the clock user-supplied to the ALTREMOTE_UPDATE megafunction must meet this specification.

(2) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(3) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

User Watchdog Internal Oscillator Frequency Specification

Table 54 lists the frequency specifications for the user watchdog internal oscillator.

Table 54. User Watchdog Internal Oscillator Frequency Specifications

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

You can download the Excel-based I/O Timing spreadsheet from the Arria V Devices Documentation webpage.

Programmable IOE Delay

Table 55 lists the Arria V GZ IOE programmable delay settings.

Table 55. IOE Programmable Delay for Arria V GZ Devices (Part 1 of 2)

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model				Unit
			Industrial	Commercial	C3	C4	I3L	I4	
D1	64	0	0.464	0.493	0.924	1.011	0.921	1.006	ns
D2	32	0	0.230	0.244	0.459	0.503	0.456	0.500	ns
D3	8	0	1.587	1.699	2.992	3.192	3.047	3.257	ns
D4	64	0	0.464	0.492	0.924	1.011	0.920	1.006	ns
D5	64	0	0.464	0.493	0.924	1.011	0.921	1.006	ns

Table 55. IOE Programmable Delay for Arria V GZ Devices (Part 2 of 2)

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model				Unit
			Industrial	Commercial	C3	C4	I3L	I4	
D6	32	0	0.229	0.244	0.458	0.503	0.456	0.499	ns

Notes to Table 55:

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 56 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 56. Programmable Output Buffer Delay for Arria V GZ Devices (1)

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Notes to Table 56:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 57 lists the glossary for this chapter.

Table 57. Glossary (Part 1 of 4)

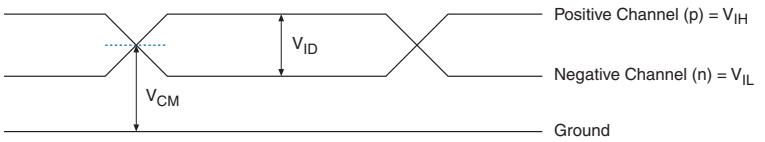
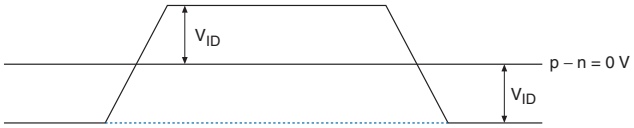
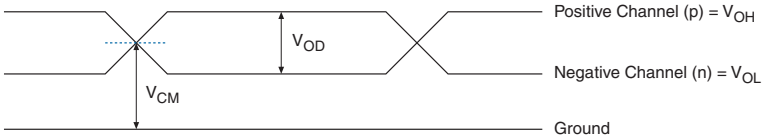
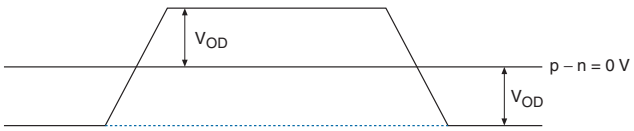
Letter	Subject	Definitions
A B C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—
F	f_{HSCLK}	Left and right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum and minimum **LVDS** data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G H I	—	—

Table 57. Glossary (Part 2 of 4)

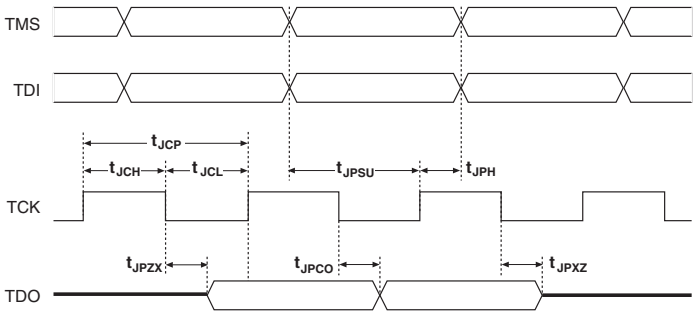
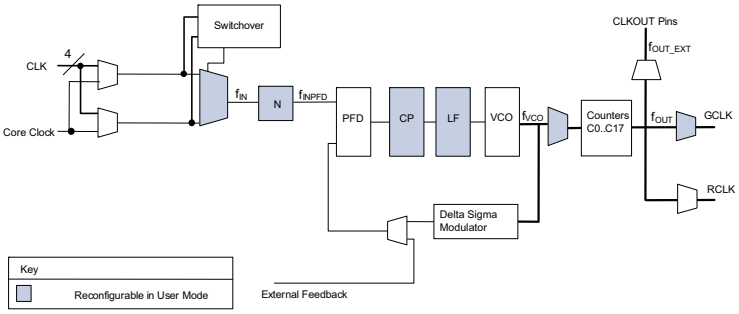
Letter	Subject	Definitions
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	JTAG Timing Specifications: 
K L M N O	—	—
P	**PLL Specifications**	**Diagram of PLL Specifications** *(1)*  **Note:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to the Arria V GZ device).

Table 57. Glossary (Part 3 of 4)

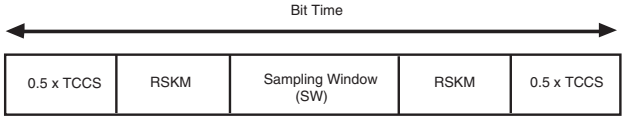
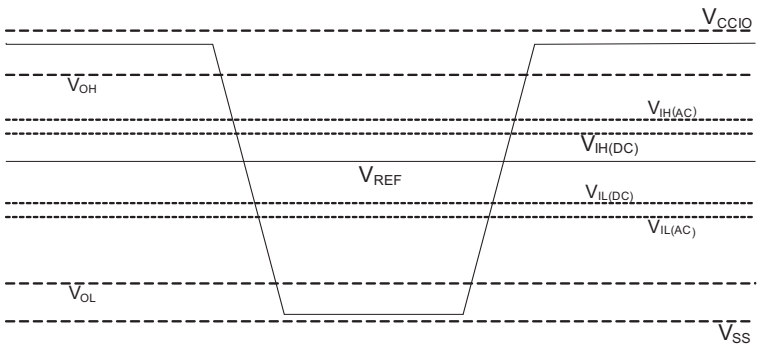
Letter	Subject	Definitions
S	**SW (sampling window)**	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown: 
	Single-ended voltage referenced I/O standard	The JEDEC standard for **SSTL** and **HSTL** I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table).
	t_{DUTY}	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(receiver input clock frequency multiplication factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
	t_{RISE}	Signal low-to-high transition time (20-80%)
U	—	—

Table 57. Glossary (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X Y Z	—	—

Document Revision History

Table 58 lists the revision history for this document.

Table 58. Document Revision History (Part 1 of 2)

Date	Version	Changes
February 2014	3.7	Updated Table 28.
December 2013	3.6	■ Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49 ■ Updated “PLL Specifications”
August 2013	3.5	Updated Table 28.
August 2013	3.4	■ Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54 ■ Updated Table 2 and Table 28
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55

Table 58. Document Revision History (Part 2 of 2)

Date	Version	Changes
May 2013	3.2	Added Table 23 Updated Table 5, Table 22, Table 26, and Table 57 Updated Figure 6, Figure 7, Figure 8, and Figure 9
March 2013	3.1	Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52 Updated “Maximum Allowed Overshoot and Undershoot Voltage”
December 2012	3.0	Initial release.