- **Members of the Texas Instruments Widebus™ Family**
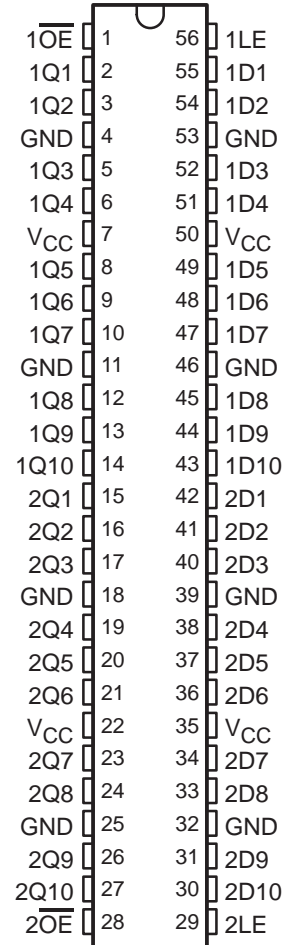
- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 5 V, T_A = 25°C**

- **High-Impedance State During Power Up and Power Down**

- **I_{off} and Power-Up 3-State Support Hot Insertion**

- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

SN54ABT162841 . . . WD PACKAGE
SN74ABT162841 . . . DGG OR DL PACKAGE
(TOP VIEW)

1OE	1		56	1LE
1Q1	2		55	1D1
1Q2	3		54	1D2
GND	4		53	GND
1Q3	5		52	1D3
1Q4	6		51	1D4
V_{CC}	7		50	V_{CC}
1Q5	8		49	1D5
1Q6	9		48	1D6
1Q7	10		47	1D7
GND	11		46	GND
1Q8	12		45	1D8
1Q9	13		44	1D9
1Q10	14		43	1D10
2Q1	15		42	2D1
2Q2	16		41	2D2
2Q3	17		40	2D3
GND	18		39	GND
2Q4	19		38	2D4
2Q5	20		37	2D5
2Q6	21		36	2D6
V_{CC}	22		35	V_{CC}
2Q7	23		34	2D7
2Q8	24		33	2D8
GND	25		32	GND
2Q9	26		31	2D9
2Q10	27		30	2D10
2OE	28		29	2LE

description/ordering information

These 20-bit transparent D-type latches feature noninverting 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT162841 devices can be used as two 10-bit latches or one 20-bit latch. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74ABT162841DL	ABT162841
		Tape and reel	SN74ABT162841DLR	
	TSSOP – DGG	Tape and reel	SN74ABT162841DGGR	ABT162841
−55°C to 125°C	CFP – WD	Tube	SNJ54ABT162841WD	SNJ54ABT162841WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

description/ordering information (continued)

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$ does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.
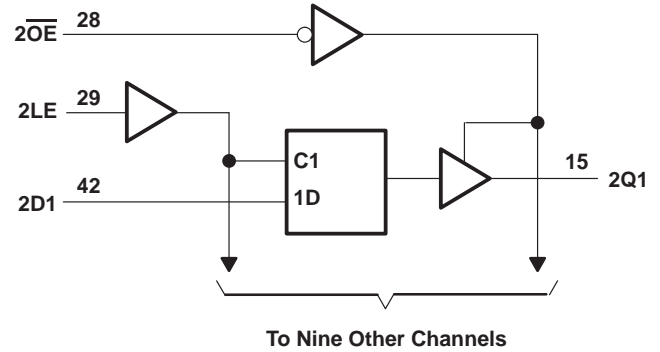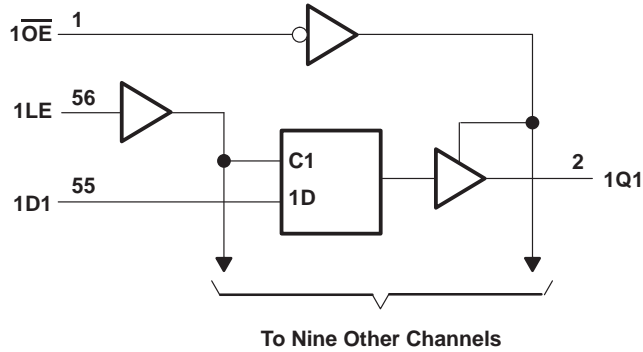
FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)

To Nine Other Channels   **To Nine Other Channels**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O .... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 64°C/W
                                                  DL package .... 56°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54ABT162841		SN74ABT162841		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−3		−12	mA
I_{OL}	Low-level output current			8		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ABT162841		SN74ABT162841		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -1$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = -1$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4			2.4		2.4		
			$I_{OH} = -12$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 8$ mA		0.4			0.8		0.65	V
			$I_{OL} = 12$ mA		0.8*					0.8	
V_{hys}					100						mV
I_I		$V_{CC} = 0$ to 5.5 V, $V_I = V_{CC}$ or GND			±1			±1		±1	µA
I_{OZPU}		$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$			±50			±50		±50	µA
I_{OZPD}		$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$			±50			±50		±50	µA
I_{OZH}		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, $\overline{OE} \geq 2$ V			10			10		10	µA
I_{OZL}		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, $\overline{OE} \geq 2$ V			−10			−10		−10	µA
I_{off}		$V_{CC} = 0$, V_I or $V_O \leq 4.5$ V			±100					±100	µA
I_{CEX}	Outputs high	$V_{CC} = 5.5$ V, $V_O = 5.5$ V			50			50		50	µA
I_O‡		$V_{CC} = 5.5$ V, $V_O = 2.5$ V		−25	−75	−100	−25	−100	−25	−100	mA
I_{CC}	Outputs high	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND			0.5			0.5		0.5	mA
	Outputs low				89			89		89	
	Outputs disabled				0.5			0.5		0.5	
ΔI_{CC}§		$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5			1.5		1.5	mA
C_i		$V_I = 2.5$ V or 0.5 V			3.5						pF
C_o		$V_O = 2.5$ V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5$ V, $T_A = 25°C$		SN54ABT162841		SN74ABT162841		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low	4		4		4		ns
t_{su}	Setup time, data before LE↓	0.8		0.8		0.8		ns
t_h	Hold time, data after LE↓	1.8		1.8		1.8		ns

TEXAS INSTRUMENTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C$_L$ = 50 pF (unless otherwise noted) (see Figure 1)
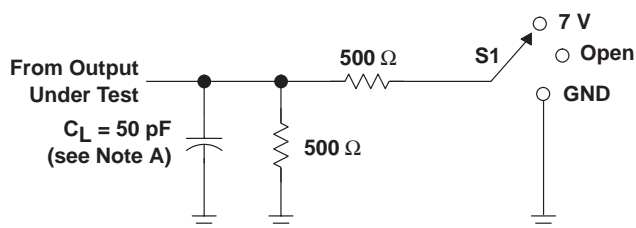
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$ = 5 V, T$_A$ = 25°C			SN54ABT162841		SN74ABT162841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{PLH}$	D	Q	2.1	3.5	4.5	2.1	5.7	2.1	5.2	ns
t$_{PHL}$			3	4.3	5.3	3	6.2	3	6	
t$_{PLH}$	LE	Q	2.1	3.5	4.5	2.1	5.6	2.1	5.4	ns
t$_{PHL}$			2.8	4.1	5.1	2.8	6.1	2.8	5.8	
t$_{PZH}$	$\overline{OE}$	Q	2	3.6	4.7	2	5.8	2	5.7	ns
t$_{PZL}$			3	4.6	5.7	3	6.7	3	6.5	
t$_{PHZ}$	$\overline{OE}$	Q	2.6	4.3	5.7	2.6	6.6	2.6	6.5	ns
t$_{PLZ}$			2.2	3.6	5.8	2.2	8.4	2.2	7.1	

PARAMETER MEASUREMENT INFORMATION

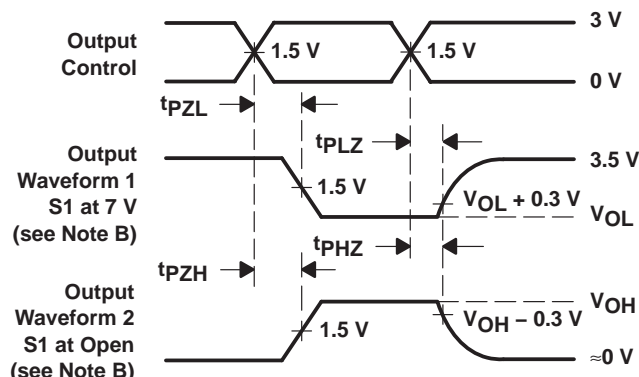| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION
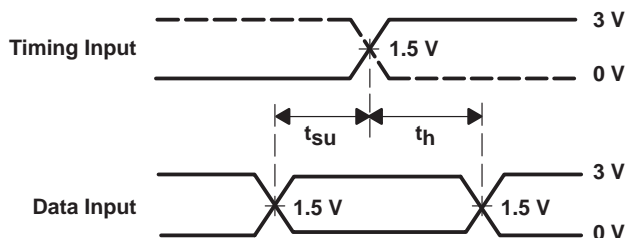
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
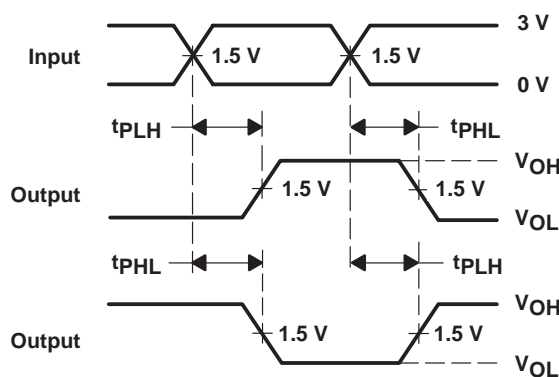
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time, with one transition per measurement.
   E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74ABT162841DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABT162841DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT162841DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT162841DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT162841DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT162841DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

48   25

0.010 (0,25)
0.005 (0,13)

0.299 (7,59)
0.291 (7,39)

0.420 (10,67)
0.395 (10,03)

Gage Plane

0.010 (0,25)

1   24

0°−8°

0.040 (1,02)
0.020 (0,51)

A

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS **	48	56	64
DIM			
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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