

Low-voltage frequency synthesizer for radio telephones

UMA1017M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1017M BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop. The device is designed to

operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at VCO input frequencies up to 1.2 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. $V_{DD} = 3$ V and $V_{CC} = 5$ V for wider tuning range.

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	—	5.5	V
$I_{CC} + I_{DD}$	supply current		—	6.9	—	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		—	12	—	μ A
f_{VCO}	input frequency		50	—	1200	MHz
f_{XTAL}	crystal reference input frequency		3	—	40	MHz
f_{PC}	phase comparator frequency		—	200	—	kHz
T_{amb}	operating ambient temperature		−30	—	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1017M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

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November 1994

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BLOCK DIAGRAM

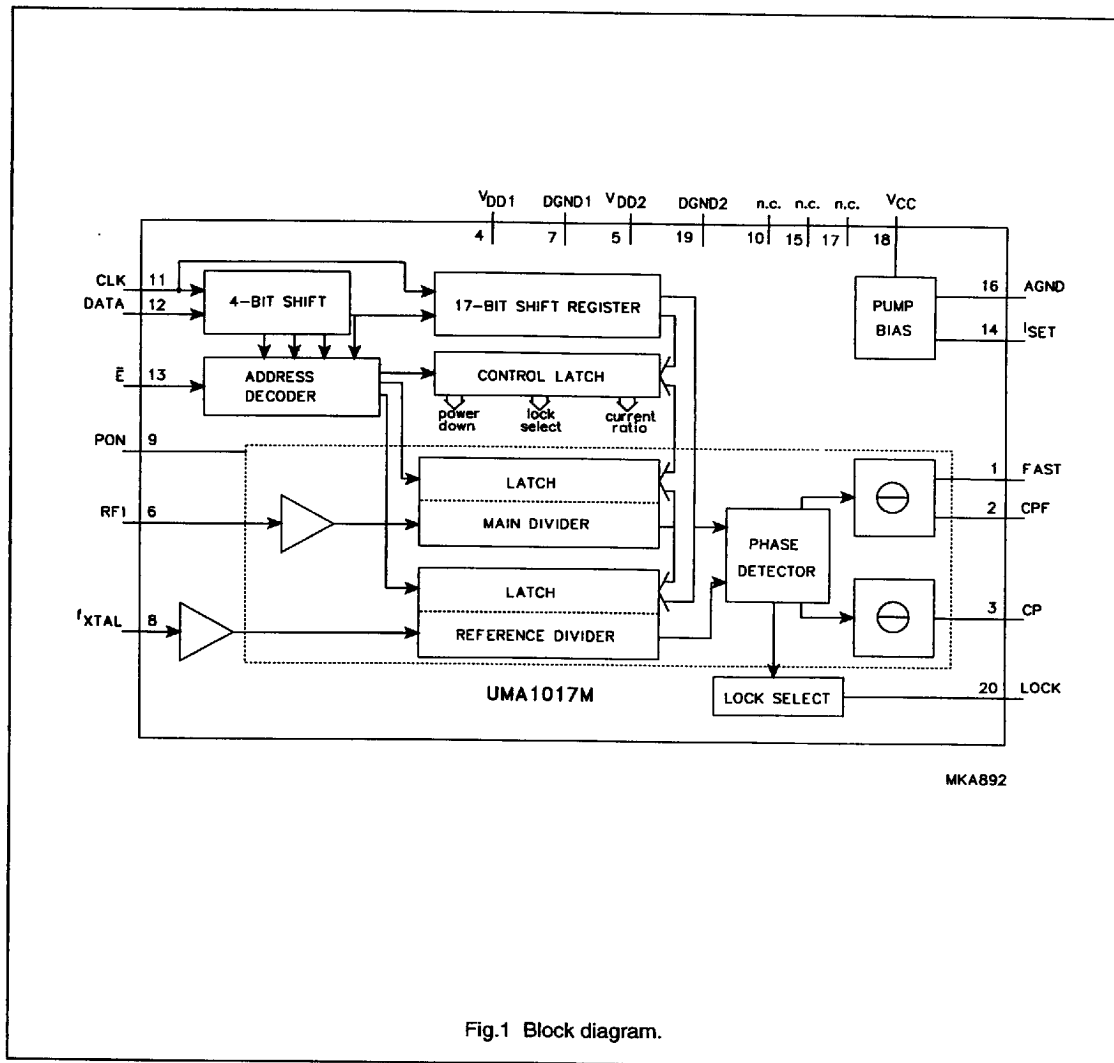


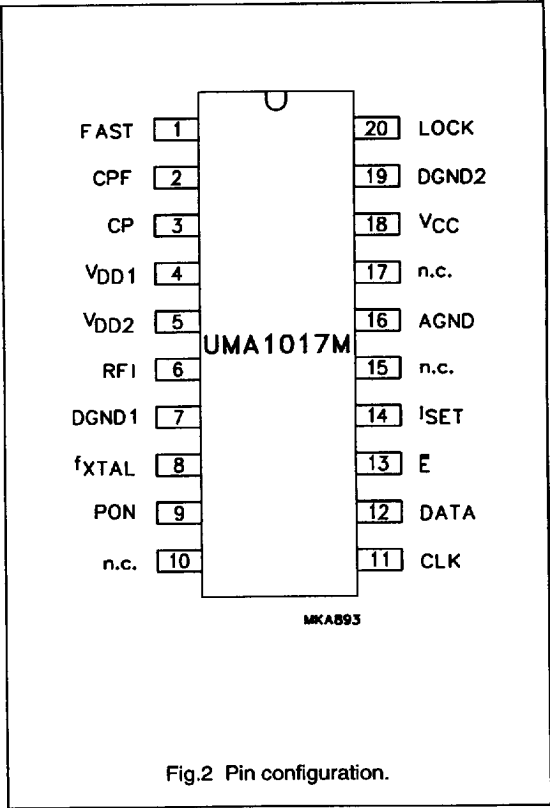
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V _{DD1}	4	digital power supply 1
V _{DD2}	5	digital power supply 2
RFI	6	1 GHz RF divider input
DGND1	7	digital ground 1
f _{XTAL}	8	reference frequency input from crystal oscillator
PON	9	power-on input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
E	13	programming bus enable input (active LOW)
I _{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V _{CC}	18	supply for charge-pump
DGND2	19	digital ground 2
LOCK	20	in-lock detect output; test mode output



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FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 50 mV up to 300 mV (RMS), and at frequencies as high as 1.2 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 1 MHz phase comparison with the 500 MHz inputs, and a 10 kHz phase comparison at 1.2 GHz RF.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μ A. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and \bar{E} (enable). The data sent to the device is loaded in bursts framed by \bar{E} . Programming clock edges and their appropriate data bits are ignored until \bar{E} goes active LOW. The programmed information is loaded into the addressed latch when \bar{E} returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1017M uses 4 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of \bar{E} . This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum \bar{E} pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (PON) or software (sPON). The dividers are on when both PON and sPON are at logic 1.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

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Table 1 Format of programmed data

LAST IN		PROGRAMMING REGISTER BIT USAGE						FIRST IN	
p21	p20	p19	p18	p17	p16	p15	p14	p13	p12
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	DATA2	DATA3	DATA4	DATA5
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB	

Table 2 Bit allocation (note 1)

REGISTER BIT ALLOCATION																					LT			
FT																								
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21				
dt16	dt15	dt14	dt13	dt12								dt4	dt3	dt2	dt1	dt0		ADDRESS						
TEST BITS(2)																								
X	X	X	X	X	OOL	X	CR1	CR0	X	X	SPON	X	X	X	X	X	0	0	0	0				
PM16	MAIN DIVIDER COEFFICIENT																	PM0	0	1	0	0		
X	X	X	X	X	X	PR10						REFERENCE DIVIDER COEFFICIENT					PR0	0	1	0	1			

Notes

1. FT = first, LT = last; sPON = software power-up for synthesizer (1 = ON); OOL = out-of-lock (1 = enabled).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	lcp	lcpf	lcpf : lcp
0	0	4 × lset	16 × lset	4 : 1
0	1	4 × lset	32 × lset	8 : 1
1	0	2 × lset	24 × lset	12 : 1
1	1	2 × lset	32 × lset	16 : 1

Note

Note

1. $I_{\text{SET}} = \frac{V_{14}}{R_{\text{ext}}}$; bias current for charge pumps.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	-0.3	+5.5	V
V_{CC}	analog supply voltage	-0.3	+5.5	V
$\Delta V_{CC-V_{DD}}$	difference in voltage between V_{CC} and V_{DD}	-0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	-0.3	$V_{DD} + 0.3$	V
$V_{2,3}$	voltage at pins 2 and 3	-0.3	$V_{CC} + 0.3$	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	-0.3	+0.3	V
P_{tot}	total power dissipation	—	150	mW
T_{stg}	storage temperature	-55	+125	°C
T_{amb}	operating ambient temperature	-30	+85	°C
T_j	maximum junction temperature	—	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

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CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	6.5	8.5	mA
I_{CC}	charge pumps analog supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ k Ω	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μ A
RF main divider input; pin 6						
f_{VCO}	VCO input frequency	2.7 V < V_{DD} < 4.5 V	50	–	1200	MHz
		2.7 V < V_{DD} < 5.5 V	50	–	1100	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω ; 2.7 V < V_{DD} < 3.5 V; $0.5 < f_{VCO} < 1.2$ GHz	50	–	300	mV
		$R_s = 50$ Ω ; 2.7 V < V_{DD} < 5.5 V; $0.5 < f_{VCO} < 1.1$ GHz	100	–	300	mV
		$R_s = 50$ Ω ; 2.7 V < V_{DD} < 5.5 V; $50 < f_{VCO} < 500$ MHz	150	–	300	mV
Z_i	input impedance (real part)	$f_{VCO} = 1$ GHz	–	1	–	k Ω
C_i	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
f_{PCmin}	minimum loop comparison frequency		–	10	–	kHz
Synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_i	input impedance (real part)	$f_{XTAL} = 30$ MHz	–	2	–	k Ω
C_i	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	k Ω
V_{14}	regulated voltage at pin 14	$R_{ext} = 12$ k Ω	–	1.15	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump outputs; pins 3 and 2; $R_{ext} = 12\text{ k}\Omega$						
I_{Ocp}	charge pump output current error		-25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	± 5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = \frac{1}{2}V_{CC}$	-5	± 1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		-0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	-5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	$I_{sink} = 0.4\text{ mA}$	–	–	0.4	V

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SERIAL BUS TIMING CHARACTERISTICS

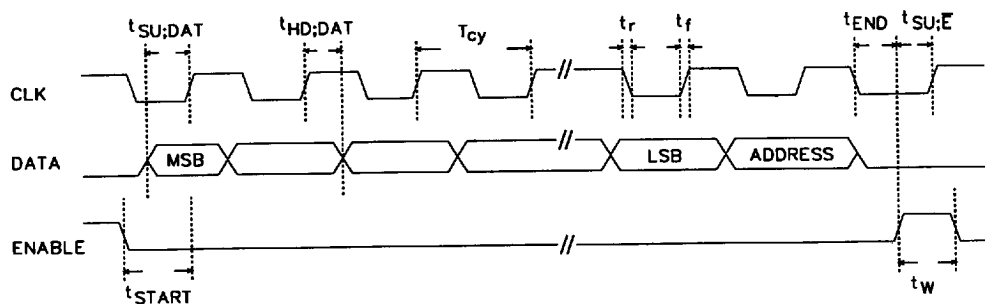
 $V_{DD} = V_{CC} = 3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	—	10	40	ns
t_f	input fall time	—	10	40	ns
T_{cy}	clock period	100	—	—	ns
Enable programming; \bar{E}					
t_{START}	delay to rising clock edge	40	—	—	ns
t_{END}	delay from last falling clock edge	—20	—	—	ns
t_W	minimum inactive pulse width	2000 ⁽¹⁾	—	—	ns
$t_{SU;\bar{E}}$	enable set-up time to next clock edge	20	—	—	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	—	—	ns
$t_{HD;DAT}$	input data to clock hold time	20	—	—	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 μs provided all the following conditions are satisfied:

- Main divider input frequency $f_{VCO} > \frac{256}{t_W}$
- Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$



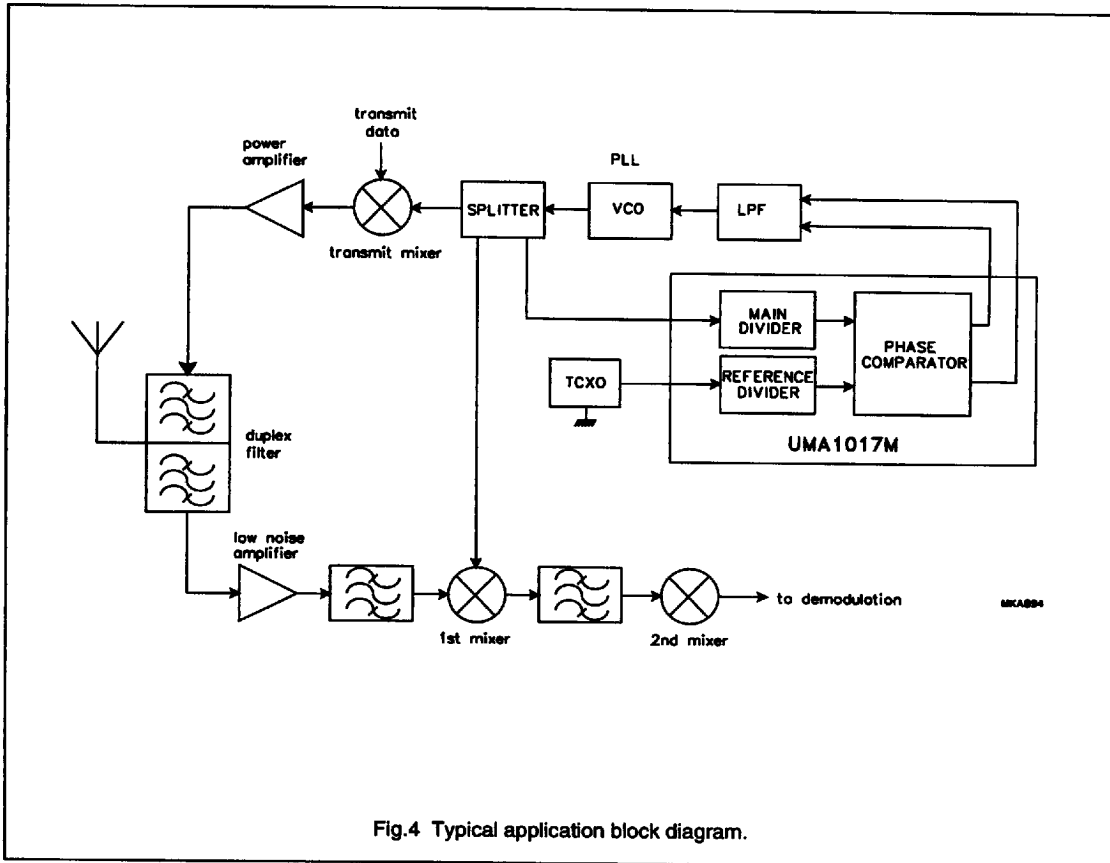
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Fig.3 Serial bus timing diagram.

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APPLICATION INFORMATION



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