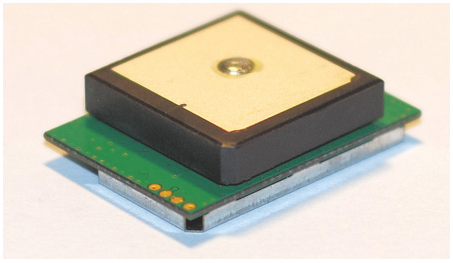

**REV 1.1**

# TECHNICAL DESCRIPTION

## *uPatch300 GPS Receiver*

This document describes the electrical connectivity and main functionality of the uPatch300 hardware.

April 25, 2007

Fastrax Ltd.



Fastrax

TRADEMARKS

# CHANGE LOG

| Rev. | Notes | Date |
|---|---|---|
| 0.1 | First Draft | 2006-10-13 |
| 0.2 | Minor updates | 2006-12-08 |
| 0.3 | Updated specs, minor updates | 2007-01-15 |
| 0.4 | Minor corrections | 2007-02-05 |
| 1.0 | Added chapter 3. Operation. Updated antenna bias threshold to 3mA. Height updated to 7.2mm | 2007-03-30 |
| 1.1 | Updated mechanical drawing | 2007-04-25 |

# CONTENTS

## COMPLEMENTARY READING

The following Fastrax reference documents are complementary reading for this document.

| Ref. # | File name | Document name |
|---|---|---|
| I | GSC3eLP_Datasheet_Aug06.pdf | GSC3e/LP Datasheet |
| II | NMEA Reference Manual.pdf | NMEA Reference Manual |
| III | SiRF Binary Protocol Reference Manual.pdf | SiRF Binary Protocol Reference Manual |
| IV | APNT3008.pdf | SiRF Application Note Power Management Considerations of SiRFstarIII |
| | | |

# 1. GENERAL DESCRIPTION

The uPatch300 is an OEM GPS receiver module, which uses the SiRF single chip receiver GSC3e/LP *(ref 1)* with tiny form factor 19.0 x 27.0mm. The uPatch300 receiver provides very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations. The module operates with the SiRF firmware GSW3 from an internal 8 Mbit flash memory.

The module provides complete signal processing from internal antenna to serial data output in NMEA (or SiRF binary) messages. The module requires a power supply VDD and a back up supply voltage BU for non-volatile RTC & RAM blocks. The uPatch300 module interfaces to the customer's application via one serial port, two control signals and PPS timing signal. Serial data and all I/O signal levels are CMOS compatible.

The antenna input connector supports external active antenna connectivity. Switching from internal patch antenna to an external antenna is handled automatically. uPatch300 provides also internally generated antenna bias supply at the external antenna connector.

## 1.1 Default firmware configuration

uPatch300 default firmware GSW3 configuration:

1. Port A: NMEA 9600 baud (switchable to SiRF binary by host)
2. NMEA output: GGA, RMC, GSV, GSA (all 1 sec interval)
3. Port B: no protocol
4. Track smoothing: disabled
5. Static navigation: enabled
6. DGPS/SBAS: disabled
7. Datum: WGS84

# 2. SPECIFICATIONS

## 2.1 General

**Table 1** General Specifications

| | |
|---|---|
| Receiver | GPS L1 C/A-code, SPS |
| Channels | 20 physical (limited to 12 tracking by firmware) |
| Update rate | 1 Hz default (fix rate configurable) |
| Acquisition Sensitivity (Cold) | -143dBm (1) |
| Navigation Sensitivity | -158dBm (1) |
| Tracking Sensitivity | -158dBm (1) |
| Supply voltage, VDD | +3.0V…+3.6 V |
| Back up supply voltage, BU | +3.0V…+3.6 V (preferably active all the time) |
| Power consumption, VDD | 120 mW typical @ 3.0V (without Antenna bias) |
| Power consumption, BU | 45 uW typical @ 3.0V (during battery backup state) |
| External antenna net gain range | +10…+30 dB |
| External antenna bias voltage | Same as VDD (+3.0V…+3.6V) |
| External antenna bias current | > 3mA (typ.), limited to max 50mA (typ.) |
| External antenna connector type | Hirose RF connector U.FL-R-SMT(01) |
| Operating temperature range | -30ºC…+85ºC |
| Serial port protocol | Port A: NMEA (switchable to SiRF binary) |
| Serial data format | 8 bits, no parity, 1 stop bit |
| Serial data speed (default) | NMEA: 9600 baud |
| I/O signal levels | CMOS compatible: low state 0.0…0.3xVDD; high state 0.7…1.0xVDD |
| I/O sink/source capability | +/- 2 mA max. |
| I/O connector type | JST SM08B-SURS-TF |
| PPS output | +/- 1us accuracy |

Note (1): measured at antenna connector and with an external LNA NF=1.5dB.

## 2.2 Absolute maximum ratings

**Table 2** Absolute maximum ratings

| Item | Min | Max | unit |
|---|---|---|---|
| Operating temperature (1) | -30 | +85 | ºC |
| Storage temperature | -40 | +85 | ºC |
| Power dissipation | - | 500 | mW |
| Supply voltage, VDD | -0.3 | +3.6 | V |
| Supply voltage, VDD_B | -0.3 | +3.6 | V |
| Current output on antenna input | 0 | +100 | mA |
| Input voltage on any input connection | -0.3 | VDD + 0.3 | V |
| RF input level | - | +15 | dBm |

Note (1): Operation at the temperature range -40…-30C accepted but the TTFF may increase.

# 3. OPERATION

## 3.1 Operating modes

After power up the receiver boots from the internal flash memory for normal operation. Modes of operation:

- Navigating mode
- Power management system modes
- Programming mode

## 3.2 Navigating mode

The receiver enters navigating mode after power up. It will start navigation automatically after power up/reset using all (if any) aiding information on GPS time, satellite ephemeris and Last Known Good (LKG) position information provided by the non-volatile back up block (RTC & RAM). The power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as *Full-power state*.

Navigation is available as long as the VDD and BU power supplies are active. Navigation can be stopped by removing the main VDD supply but if possible keep the back up supply BU active for fastest possible TTFF on next power up.

Any configuration settings are valid as long as the back up supply BU is active. When the BU is powered off, the configuration is reset to factory configuration on next power up.

### 3.2.1 Default firmware configuration

Fastrax default SiRF GSW3 firmware configuration:

1. Port A: NMEA 9600 baud (switchable to SiRF binary by host)
2. NMEA output: GGA, RMC, GSV, GSA (all 1 sec interval)
3. Port B: no protocol
4. Track smoothing: disabled
5. Static navigation: enabled
6. DGPS/SBAS: disabled

7. Datum: WGS84

### 3.3 Power management system states

The receiver supports also SiRF operating modes for reduced average power consumption *(ref IV)* like Adaptive TricklePower™, Push-to-Fix™ and Advanced Power Management modes with SiRF firmware. These operating modes are different combinations of the following system states:

1. *Full-power state*: This is the initial state of the receiver where all RF circuitry and the baseband are fully powered. The receiver stays in this state until a position solution is made and estimated to be reliable.

2. *The CPU-only state*: This is the state when the LNA in the RF section is shut off. The other parts of the RF section, including the TCXO and fractional synthesizer are still powered in order to provide a clock to the CPU. This state is entered when the satellite measurements have been collected but the navigation solution still needs to be computed. The RF and DSP processing are no longer needed and can be turned off. Both VDD and BU supplies are active.

3. *Stand-by state (or Trickle state)*: In this state, the internal RF section is completely powered off and the clock to the baseband is stopped. About 1 mA of current is drawn in this state for the internal core regulator, RTC and battery-backed RAM. The receiver enters this state when a position fix has been computed and reported. Typically, before shutting down the RTC wakeup register is programmed to wake up the system sometime in the future. Both VDD and BU supplies are still active.

4. *The Back Up (also Hibernate) state*: This is intended for ultra-low power consuming applications. Both the RF and the baseband are powered off (VDD supply is switched off by the host), leaving only the RTC and battery-backed RAM running (BU is still active). In this state about 15 µA of current is drawn from BU.

The exit from Stand-by and Back Up modes to Navigating mode happens either after

- elapsed time or

- powering VDD supply on by the host

Since the internal RTC keeps the GPS time estimate, the module performs the fastest possible navigation start, depending on the availability of valid satellite/position data.

### 3.4 Programming mode

Re-programming via HW-booting mode is utilized by keeping the UPDATE control input at low state during power up or at system reset. Now the GPS module boots from the serial data Port A and waits for the boot loader commands from the host (an application running on the host, SiRFFlash). It is suggested that all applications should support the HW-booting by access to serial Port A (TX & RX), UPDATE and XRESET signals.

Note that during the flash update process the serial data speed is changed and thus the serial line connection should be a direct line to the host without any transferring utilities that may cause a failure during speed change.

### 3.5 Procedure for re-programming the firmware

1. Connect serial Port A to PC.

2. Set the module to UART boot mode: Power up the module with UPDATE signal low. Alternatively give a XRESET pulse while keeping UPDATE signal low after the power supply is on.

3. Start SiRFFlash application on PC.

4. Browse for the flash *.s file.

5. Check the Communication setting from the SiRFFlash to meet your PC serial port.

6. Press Execute at SiRFFlash. Now the flashing starts.

7. After flashing has finished, boot the receiver normally with UPDATE signal high either by cycling the power supply or by giving a XRESET pulse high-low-high.

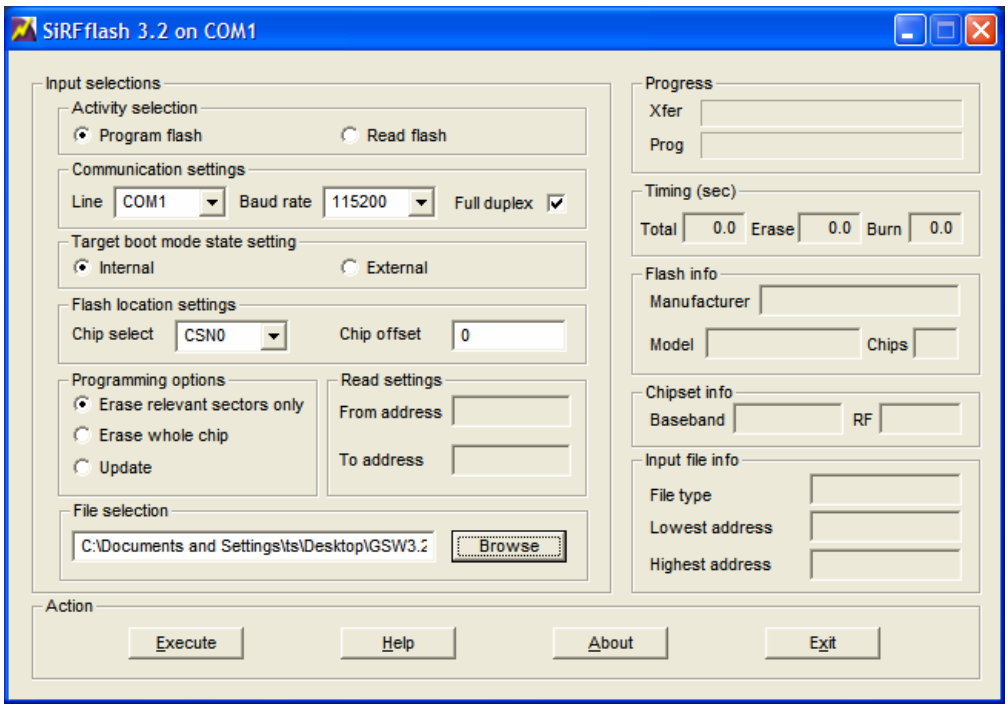


**Figure 1** SiRFFlash default settings.

# 4. CONNECTIVITY

## 4.1 Connection assignments

The I/O connections are available on the 8-pin interface connector. The connector is from JST, type SM08B-SURS-TF. Mating connector is e.g. JST 08SUR-32S.

**Table 3** Connections

| Contact | Signal name | I/O | Alternative signal name | Signal description |
|---|---|---|---|---|
| 1 | TXA | O | - | UART Port A async. Output |
| 2 | RXA | I | - | UART Port A async. Input. Pulled high internally with 100k resistor. |
| 3 | GND | - | - | Ground |
| 4 | VDD | I | - | Main power supply |
| 5 | BU | I | - | Backup supply |
| 6 | XRESET | I | - | Asynchronous system reset, active when low. Pulled high internally with 100k resistor. |
| 7 | UPDATE | I | - | Boot control input 1: 0=UART, 1=Internal flash memory. Pulled high internally with 10k resistor. |
| 8 | 1PPS | O | GPIO9 | 1PPS signal output |

## 4.2 Power supply

The uPatch300 module requires two separate power supplies: BU for non-volatile back up block and the VDD for digital parts and I/O. RF block has internally regulated +2.75V supply. VDD can be switched off when navigation is not needed but if possible keep the back up supply BU active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Back up supply BU draws typically 15uA current in back up state. During navigation (while VDD is active) BU current typically peaks up to 0.2mA.

Main power supply VDD current varies according to the processor load and satellite acquisition. Typical VDD peak current is 60mA during acquisition.

### 4.3 Reset

The reset input XRESET is an active low asynchronous reset. The processor boots after the low-to-high transition (low state >1ms) depending on the state of the UPDATE signal. The XRESET input contains an internal voltage detector to force reset when VDD is below +2.7V during power up. At power down the reset is forced when the VDD drops below 2.6V. The XRESET input is internally pulled high with 100k resistor and for normal operation it can be left unconnected.

### 4.4 Boot Select input (UPDATE)

The boot source is defined using the UPDATE pin. After power up or after system reset the value is read and the boot is processed according the following table.

UPDATE input selects the boot mode (UART or Flash).

**Table 4** Boot select

| UPDATE | Boot source |
|---|---|
| Low | UART |
| High | FLASH (normal operation) |

For re-programming the firmware, the UPDATE pin should be kept low at least 500 ms after power up or reset. The UPDATE pin has an internal 10 kohm pull-up resistor so the UPDATE pin can normally be left unconnected.

### 4.5 Antenna input

The module provides internal passive patch antenna as well as a connector for external active antenna. The antenna input impedance is 50 ohms. During normal (navigating) operation, the input provides also a bias supply which is equal to VDD. When VDD is removed, the antenna bias is switched off. The module switches automatically between the internal and external antenna.

The antenna bias current is limited by hardware to approximately 50mA. In case there is a short circuit on the external antenna input the module will automatically recover when the short is removed.

Antenna sensing is handled automatically. There is a comparator circuitry that monitors load current on the external antenna port. In case there is a suitable DC load, >3mA typ., the internal antenna signal is switched off and the antenna signal is routed to the external antenna connector.

The external antenna input connector is HIROSE UFL series. Mating connector is e.g. Hirose U.FL-LP-066.

### 4.6 UART

The device supports UART communication via Port A. With the standard firmware the Port A is configured by default to NMEA protocol (default 9600 baud). The Port A is used also when the device is booting from the serial port for re-flashing.

I/O levels form the serial ports are CMOS compatible, not RS232 compatible. Use an external level converter to provide RS232 levels when needed.

### 4.7 Mechanical dimensions and contact numbering

Module size is 19.0mm (width) x 27.0mm (length) x 7.2mm. General tolerance is ±0.3mm.

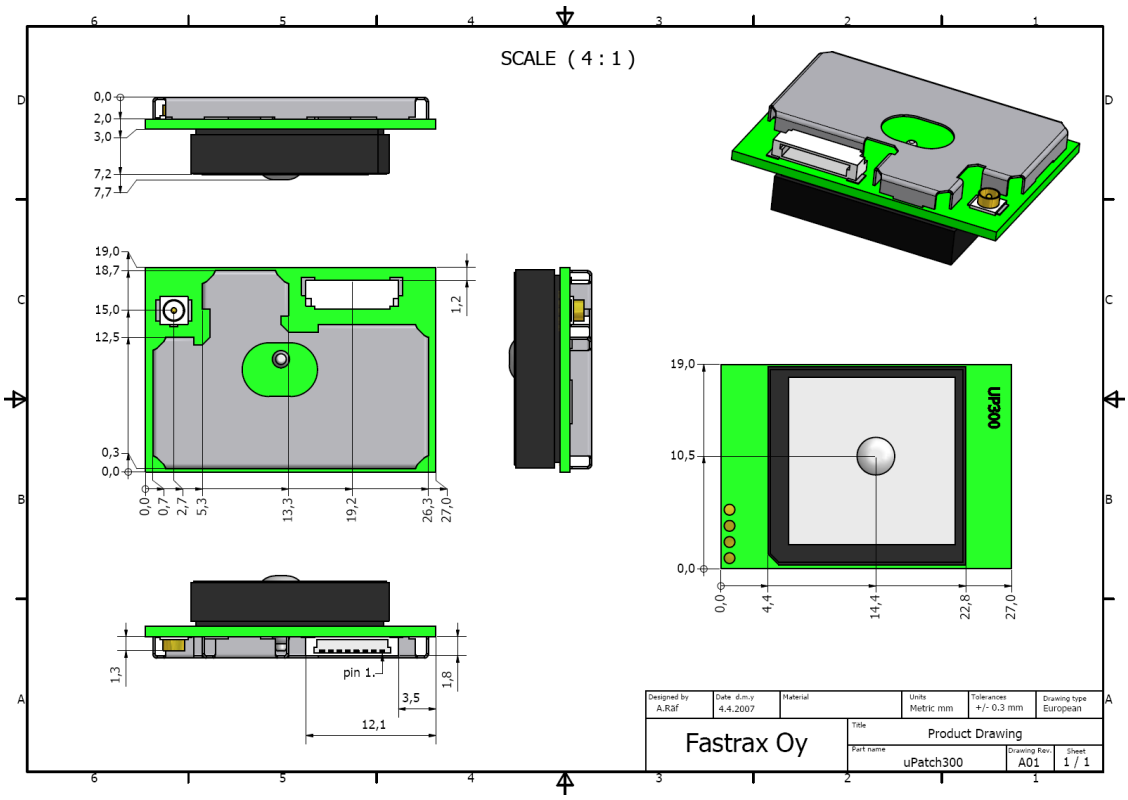


**Figure 2** Mechanical outline.