VNQ7040AY-E

Quad channel high-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data

PowerSSO-36

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per ch)	R_{ON}	40 mΩ
Current limitation (typ)	I_{LIMH}	34 A
Standby current (max)	I_{STBY}	0.5 µA

- General
  - Quad channel smart high-side driver with MultiSense analog feedback
  - LED Mode for channel 0 and 1
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: Load current with high precision proportional current mirror; V_{CC} supply voltage; T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open load detection
  - Output short to V_{CC} detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery through self turn-on
  - Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Turn Indicators (up to P27W or SAE1156 and R5W paralleled or LED Rear Combinations)

Description

The VNQ7040AY-E is a quad channel high-side driver manufactured using the latest ST proprietary VIPower® technology and housed in PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, and to provide protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions such as high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

The device features a dedicated LED Mode.

This is information on a product in full production. www.st.com

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1 Block diagram and pin description

Figure 1. Block diagram

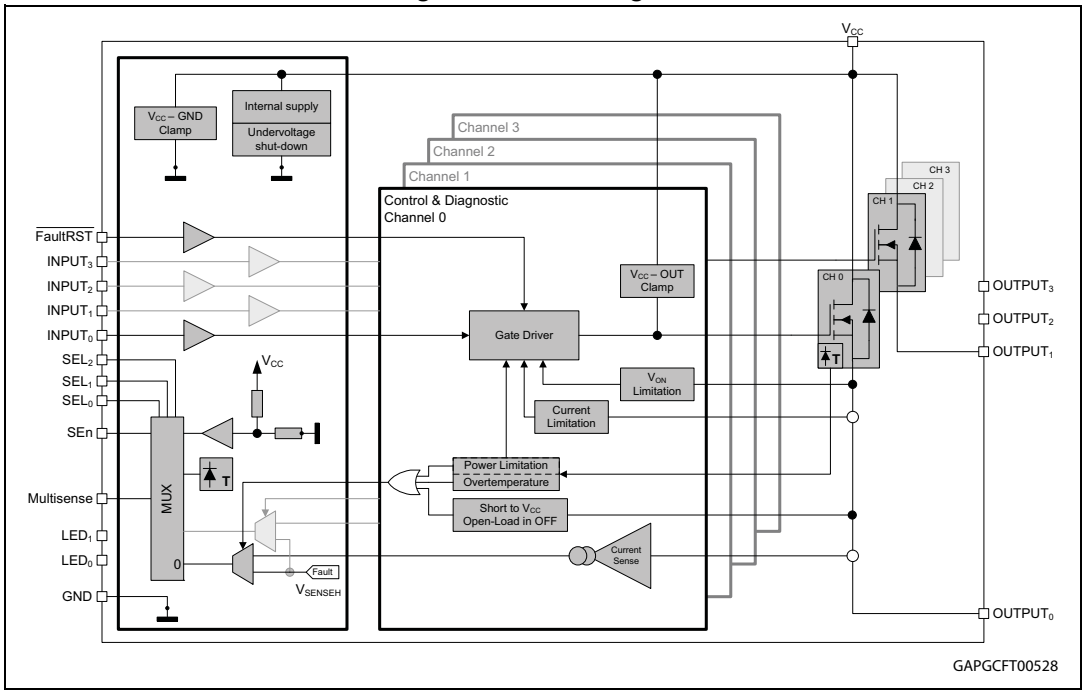


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1,2,3}$	Power output.
GND	Ground connection.
$INPUT_{0,1,2,3}$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin
$LED_{0,1}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they enable the LED mode on logic high level (see *Table 15: Truth table*).
$SEL_{0,1,2}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer (see *Table 15: Truth table*).
$\overline{FaultRST}$	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)

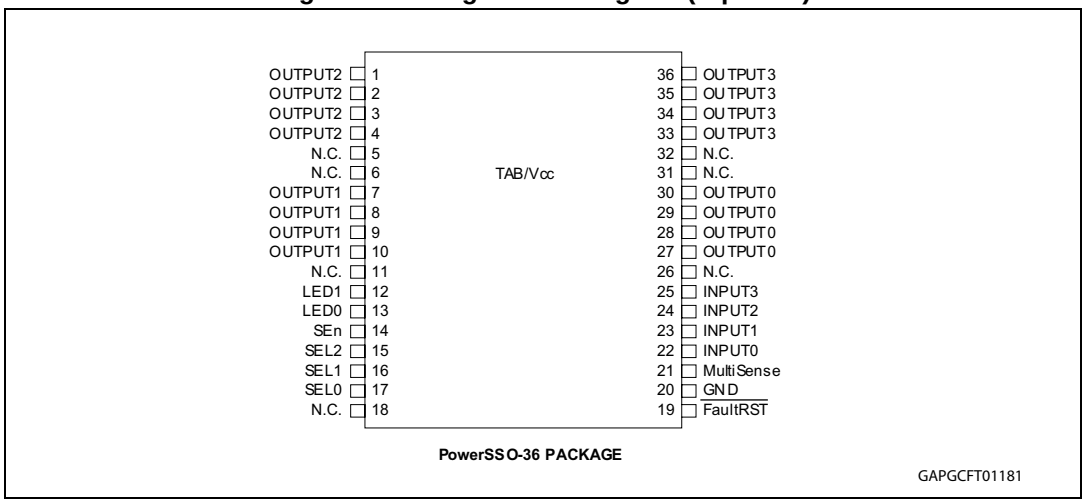


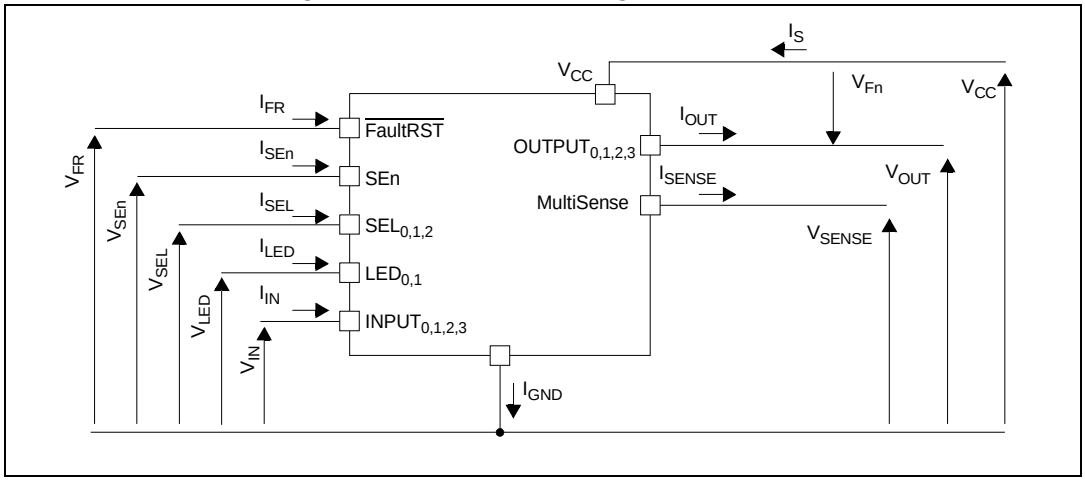
Table 2. Suggested connections for unused and not connected pins

Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, LEDx, $\overline{\text{FaultRST}}$
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



1. $V_{Fn} = V_{OUTn} - V_{CC}$

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; R_L = 4 Ω)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1,2,3}$ DC output current	Internally limited	A
$-I_{OUT\_0,1}$	$OUTPUT_{0,1}$ Reverse DC output current	10	
$-I_{OUT\_2,3}$	$OUTPUT_{2,3}$ Reverse DC output current	10	
I_{IN}	$INPUT_{0,1,2,3}$ DC input current	-1 to 10	mA
I_{LED}	$LED_{0,1}$ DC input current		
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1,2}$ DC input current		
I_{FR}	FaultRST DC input current	-1 to 10	mA

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{FR}	FaultRST DC input voltage	7.5	V
I_{SENSE}	MultiSense pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	-10	mA
	MultiSense pin DC output current in reverse (V_{CC} < 0 V)	20	mA
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150 °C)	36	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) – $INPUT_{0,1,2,3}$ – MultiSense – $LED_{0,1}$, SEn, $SEL_{0,1,2}$, $\overline{FaultRST}$ – $OUTPUT_{0,1,2,3}$ – V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8)(1)(2)	4.9	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(3)	52.5	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)(2)	18	

1. One channel ON.
2. Device mounted on four-layers 2s2p PCB
3. Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace

2.3 Electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

2.3.1 General electrical specification

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
V_{clamp}	Clamp voltage	I_S = 20 mA; 25 °C < T_j < 150 °C	41	46	52	V
		I_S = 20 mA; T_j = -40 °C	38			V
I_{STBY}	Supply current in standby at V_{CC} = 13 V(1)	V_{CC} = 13 V; V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1,2}$ = 0 V; $V_{LED0,1}$ = 0 V; T_j = 25 °C			0.5	µA
		V_{CC} = 13 V; V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1,2}$ = 0 V; $V_{LED0,1}$ = 0 V; T_j = 85 °C(2)			0.5	µA
		V_{CC} = 13 V; V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1,2}$ = 0 V; $V_{LED0,1}$ = 0 V; T_j = 125 °C;			3	µA
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{INx} = V_{OUTx} = V_{FR} = 0 V; $V_{SEL0,1,2}$ = 0 V; $V_{LED0,1}$ = 0 V; V_{SEn} = 5 V to 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{INx} = 5 V; $I_{OUT0,1,2,3}$ = 0 A;		10	16	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; V_{INx} = 5 V; $I_{OUT0,1,2,3}$ = 2.5 A			18.5	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V(1)	V_{INx} = V_{OUTx} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	0.5	µA
		V_{INx} = V_{OUTx} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		3	
V_F	Output - V_{CC} diode voltage(3)	I_{OUT} = -2.5 A; T_j = 150 °C			0.7	V

1. PowerMOS leakage included.

2. Parameter specified by design; not subject to production test.
3. For each channel.

Table 6. Logic Inputs (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$INPUT_{0,1,2,3}$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$\overline{FaultRST}$ characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1,2}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$LED_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{LEDL}	Input low level voltage				0.9	V
I_{LEDL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{LEDH}	Input high level voltage		2.1			V
I_{LEDH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{LED(hyst)}$	Input hysteresis voltage		0.2			V

Table 6. Logic Inputs (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{LEDCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 7. Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(1)		T_{RS} + 1	T_{RS} + 5		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} =5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)(1)			5		
ΔT_{J_SD}	Dynamic temperature			60		K
t_{LATCH_RST}	Fault reset time for output unlatch(1)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; V_{INx} = 5 V; $V_{SEL0,1,2}$ = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}= 2 A; L = 6 mH; T_j = -40 °C	V_{CC} - 38			V
		I_{OUT}= 2 A; L = 6 mH; T_j = 25 °C to 150 °C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT}= 0.25 A		20		mV

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 8. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		-0.7		V
Current Sense characteristics						
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V;	0		0.5	µA
		MultiSense disabled: -1 V < V_{SENSE} < 5 V(1)	-0.5		0.5	
		MultiSense enabled: V_{SEn} = 5 V All channels ON; I_{OUTX} = 0 A; Ch_X diagnostic selected; – E.G. Ch_0: V_{IN0} = 5 V; $V_{IN1,2,3}$ = 5 V; $V_{SEL0,1,2}$ = 0 V; I_{OUT0} = 0 A; $I_{OUT1,2,3}$ = 2.5 A	0		2	
		MultiSense enabled: V_{SEn} = 5 V Ch_X OFF; Ch_X diagnostic selected: – E.G. Ch_0: V_{IN0} = 0 V; $V_{IN1,2,3}$ = 5 V; $V_{SEL0,1,2}$ = 0 V; I_{OUT0} = 0 A; $I_{OUT1,2,3}$ = 2.5 A	0		2	
V_{OUT_MSD}(1)	Output Voltage for MultiSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ – E.g. Ch_0: V_{IN0} = 5 V; $V_{SEL0,1,2}$ = 0 V; I_{OUT0} = 2.5 A		5		V
V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 K; V_{SEn} = 5 V; V_{IN0} = 5 V; $V_{SEL0,1,2}$ = 0 V; I_{OUT0} = 4.5 A; T_j = 150°C	5			V
I_{SENSE_SAT}(1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1,2}$ = 0 V; T_j = 150°C	4			mA
$I_{OUT\_SAT\_BULB}$(1)	Output saturation current in BULB mode	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1,2}$ = 0 V; T_j = 150°C	8			A
$I_{OUT\_SAT\_LED}$(1)	Output saturation current in LED mode	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1,2}$ = 0 V; T_j = 150°C	2.3			A
OFF-state diagnostic						
V_{OL}	OFF state open load voltage detection threshold	V_{SEn} = 5V; Ch_X OFF; Ch_X diagnostic selected – E.G: Ch_0 V_{IN0} = 0 V; $V_{SEL0,1,2}$ = 0 V	2	3	4	V
$I_{L(off2)}$	OFF state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-100		-15	µA

Table 8. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{DSTKON}	OFF state diagnostic delay time from falling edge of INPUT (see *Figure 35*)	V_{SEn} = 5 V; Ch_X ON to OFF transition; Ch_X diagnostic selected – E.G: Ch_0 V_{IN0} = 5 V to 0 V; $V_{SEL0,1,2}$ = 0 V; V_{OUT0} > 4 V	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{INx} = 0 V; V_{FR} = 0 V; $V_{SEL0,1,2}$ = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5V; Ch_X OFF; Ch_X diagnostic selected – E.G: Ch_0 V_{IN0} = 0 V; $V_{SEL0,1,2}$ = 0 V; V_{OUT0} = 0 V to 4 V		5	30	µs
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 KΩ; V_{INx} = 0 V; T_j = -40°C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 KΩ; V_{INx} = 0 V; T_j = 25°C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 KΩ; V_{INx} = 0 V; T_j = 125°C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT(2)	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC}/dT * (T-T_0)$				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; $V_{SEL0,1,2}$ = 5 V; V_{INx} = 0 V; R_{SENSE} = 1 KΩ	3.16	3.23	3.3	V
Transfer function(2)		$V_{SENSE\_VCC} = V_{CC}$ / 4				
Fault diagnostic feedback (see *Table 15*)						
V_{SENSEH}	MultiSense output voltage in fault condition(	V_{CC} = 13 V; R_{SENSE} = 1 kΩ	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (Chip Temperature Sense mode - see *Figure 37*)						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ			60	µs

Table 8. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = V_{SEL1} = 0 V; V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} Voltage Sense mode - see *Figure 37*)						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = V_{SEL1} = V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = V_{SEL1} = V_{SEL2} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense Timings (Multiplexer transition times)(3)						
t_{D_XtoY}	MultiSense transition delay from Ch_X to Ch_Y	V_{IN2} = 5 V; V_{IN3} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; V_{SEL2} = 0 V; I_{OUT2} = 0 A; I_{OUT3} = 2.5 A; R_{SENSE} = 1 kΩ			20	µs
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = V_{SEL2} = 0 V to 5 V; I_{OUT0} = 1.25 A; R_{SENSE} = 1 kΩ			60	µs
t_{D_TCtoCS}	MultiSense transition delay fromT_C sense to current sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = V_{SEL2} = 5 V to 0 V; I_{OUT0} = 1.25 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN2} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; V_{SEL2} = 0 V to 5 V; I_{OUT2} = 1.25 A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN2} = 5 V; V_{SEn} = 5 V; V_{SEL1} = 5 V; V_{SEL0} = V_{SEL2} = 5 V to 0 V; I_{OUT2} = 1.25 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{SEn} = 5 V; $V_{SEL1,2}$ = 5 V; V_{SEL0} = 0 V to 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{SEn} = 5 V; $V_{SEL1,2}$ = 5 V; V_{SEL0} = 5 V to 0 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVSENSEH}$	MultiSense transition delay from stable current sense on Ch_X to V_{SENSEH} on Ch_Y	V_{IN0} = 5 V; V_{IN1} = 0 V; V_{OUT1} > 4 V; V_{SEn} = 5 V; V_{SEL2} = 0 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 2.5 A; R_{SENSE} = 1 kΩ			60	µs

1. Parameter guaranteed by design and characterization; not subject to production test.
2. V_{CC} sensing and T_C sensing are referred to GND potential.
3. Transition delay are measured up to +/- 10% of final conditions.

2.3.2 Bulb mode (default)

Table 9. Power section in Bulb Mode (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON\_0,1,2,3\_BULB}$	On-state resistance in Bulb Mode Ch0, Ch1, Ch2 and Ch3	I_{OUT} = 2.5 A; T_j = 25°C		40		mΩ
		I_{OUT} = 2.5 A; T_j = 150°C			80	
		I_{OUT} = 2.5 A; V_{CC} = 4 V; T_j = 25°C			60	
$R_{ON\_REV\_0,1,2,3}$	On-state resistance in Reverse Battery Ch0, Ch1, Ch2 and Ch3	V_{CC} = -13V; I_{OUT} = -2.5A; T_j = 25°C		40		mΩ
$I_{LIMH\_0,1,2,3\_BULB}$(1)	DC short circuit current in Bulb Mode Ch0, Ch1, Ch2 and Ch3	V_{CC} = 13 V	24	34	48	A
		4 V < V_{CC} < 18 V(2)			48	
$I_{LIML\_0,1,2,3\_BULB}$	Short circuit current during thermal cycling in Bulb Mode Ch0, Ch1, Ch2 and Ch3	V_{CC} = 13 V; T_R < T_j < T_{TSD}		9		
$V_{ON\_0,1,2,3\_BULB}$	Output voltage drop limitation in Bulb Mode Ch0, Ch1, Ch2 and Ch3	I_{OUT} = 0.25 A		20		mV

1. Parameter guaranteed by an indirect test sequence.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 10. Switching in Bulb Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Channel 0, 1, 2 and 3						
$t_{d(on)\_0,1,2,3}$(1)	Turn-on delay time at T_j = 25 °C	R_L = 5.2 Ω	10	60	120	µs
$t_{d(off)\_0,1,2,3}$(1)	Turn-off delay time at T_j = 25 °C	R_L = 5.2 Ω	10	50	100	
$(dV_{OUT}/dt)_{on\_0,1,2,3}$(1)	Turn-on voltage slope at T_j = 25 °C	R_L = 5.2 Ω	0.1	0.5	0.7	V/µs
$(dV_{OUT}/dt)_{off\_0,1,2,3}$(1)	Turn-off voltage slope at T_j = 25 °C	R_L = 5.2 Ω	0.1	0.5	0.7	
$W_{ON\_0,1,2,3}$	Switching energy losses at turn-on (t_{won})	R_L = 5.2 Ω	—	0.2	0.52(2)	mJ

Table 10. Switching in Bulb Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$W_{OFF\_0,1,2,3}$	Switching energy losses at turn-off (t_{woff})	R_L = 5.2 Ω	—	0.2	0.5(2)	mJ
$t_{SKEW\_0,1,2,3}$(1)	Differential pulse skew (t_{PHL} - t_{PLH})	R_L = 5.2 Ω	-65	-15	35	µs

1. See *Figure 35: Switching times and Pulse skew*.
2. Parameter guaranteed by design and characterization, not subject to production test.

Table 11. MultiSense in Bulb Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Current sense characteristics						
Channel 0, 1, 2 and 3						
$K_{OL\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 10 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	430			
$K_{OL\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 10 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	430			
dK_{cal}/K_{cal}(1)(2)	Current sense ratio drift at calibration point	I_{CAL} = 30 mA; I_{OUT} = 10 mA to 50 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-35		35	%
$K_{LED\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	720	1440	2160	
$K_{LED\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	720	1440	2160	
$K_{0\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	930	1550	2170	
$K_{0\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	930	1550	2170	
dK_0/K_0(1)(2)	Current sense ratio drift	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-20		20	%
$K_{1\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1110	1590	2070	
$K_{1\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1085	1550	2015	
dK_1/K_1(1)(2)	Current sense ratio drift	I_{OUT} = 0.5 A; V_{SENSE} = 4V; V_{SEn} = 5 V	-15		15	%
$K_{2\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1160	1450	1740	
$K_{2\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1130	1410	1690	

Table 11. MultiSense in Bulb Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%
$K_{3\_CH0,1\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1295	1440	1585	
$K_{3\_CH2,3\_B}$	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1260	1400	1540	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%
MultiSense timings (Current Sense mode see *Figure 36*)						
Channel 0, 1, 2 and 3						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω		100	250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 5.2 Ω		50	250	µs

1. Parameter specified by design; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Figure 4. Bulb Mode - I_{OUT}/I_{SENSE} versus I_{OUT}

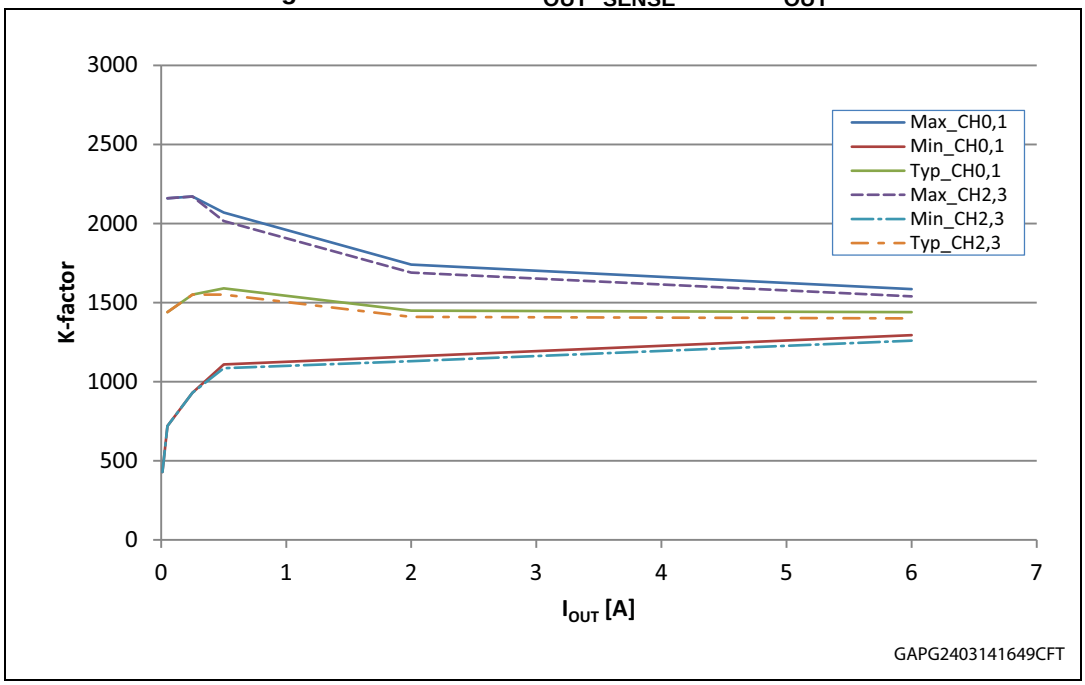
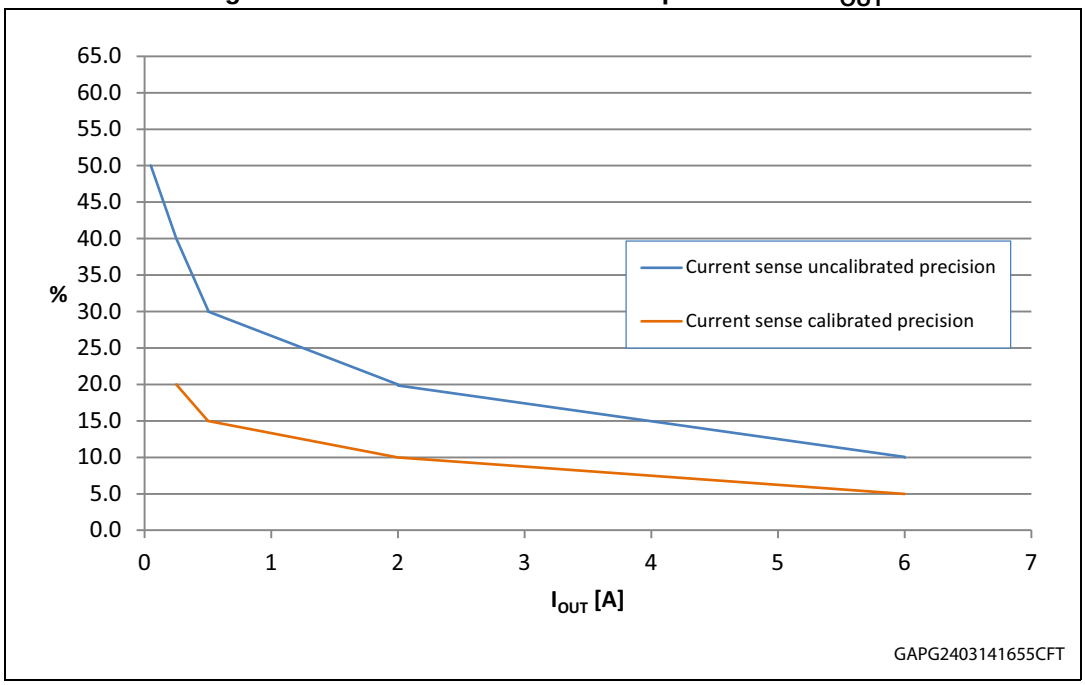
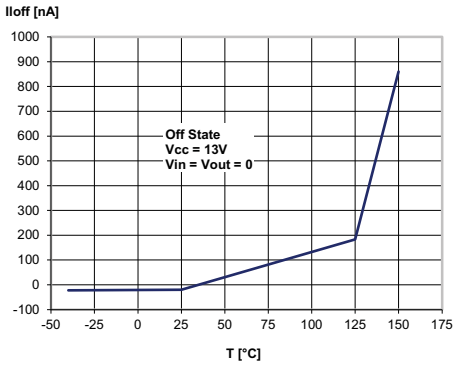


Figure 5. Bulb Mode - current sense precision vs. I_{OUT}



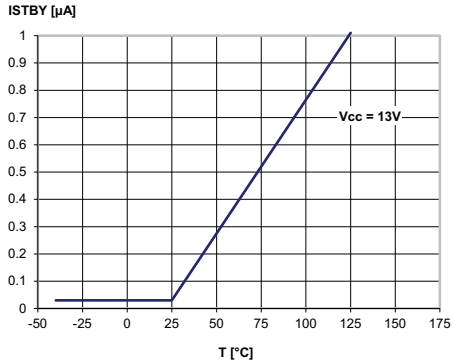
2.4 Electrical characteristics curves - Bulb Mode

Figure 6. OFF-state output current



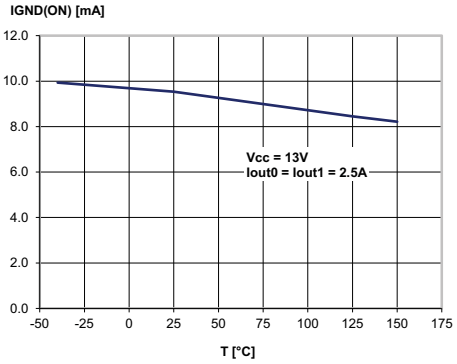
GAPG2503140942CFT

Figure 7. Standby current



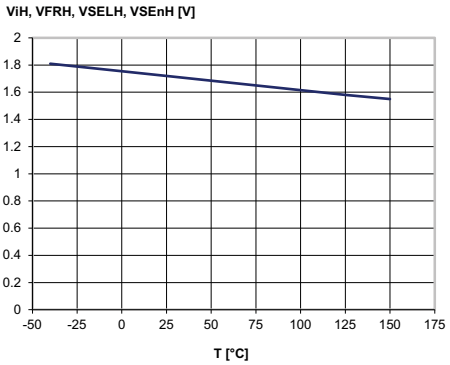
GAPG2503140943CFT

Figure 8. $I_{GND(ON)}$ vs. I_{out}



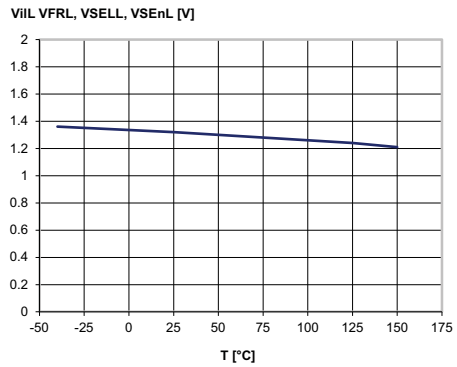
GAPG2503140944CFT

Figure 9. Logic Input high level voltage



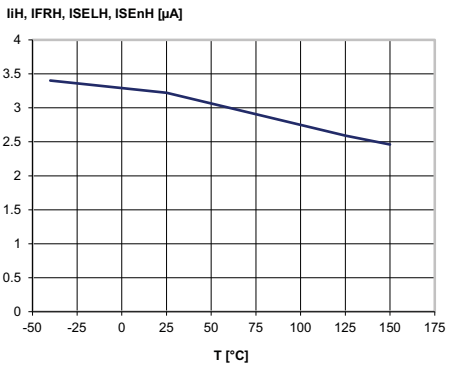
GAPG2503140945CFT

Figure 10. Logic Input low level voltage



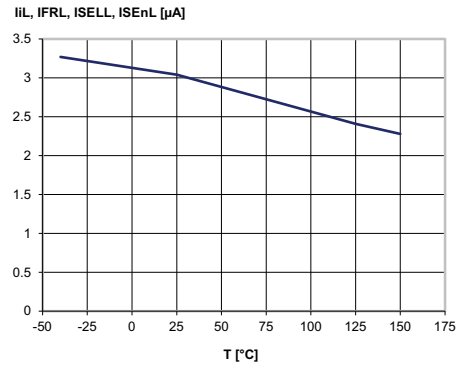
GAPG2503140946CFT

Figure 11. High level logic input current



GAPG2503140947CFT

Figure 12. Low level logic input current



GAPG2503140948CFT

Figure 13. Logic Input hysteresis voltage

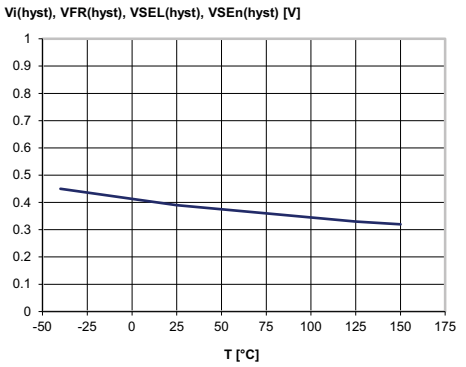


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Figure 14. FaultRST Input clamp voltage

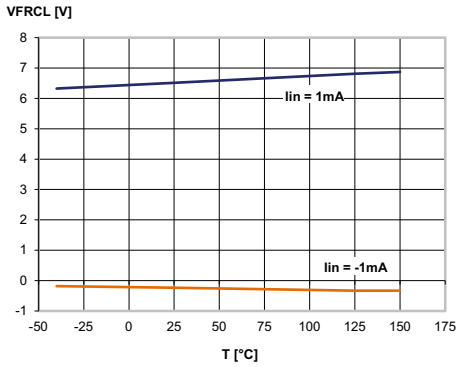

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Figure 15. Undervoltage shutdown

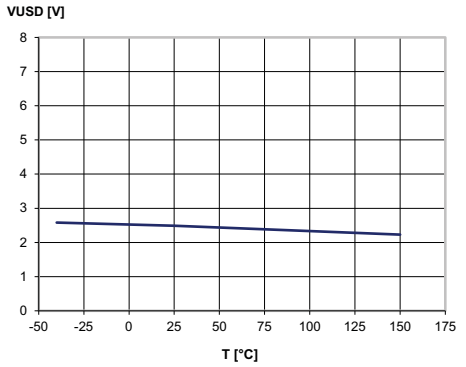

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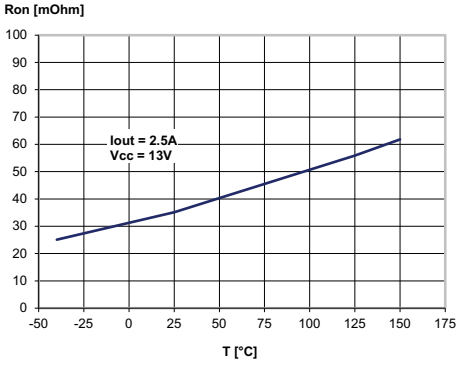
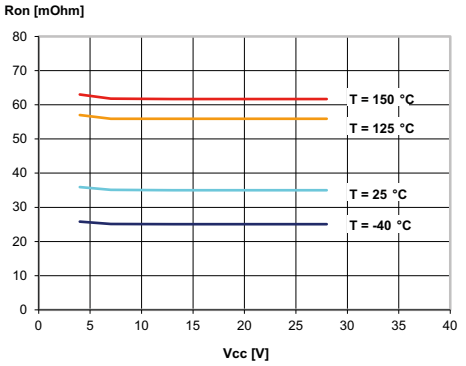
Figure 16. On-state resistance vs. T_{case}



GAPG2503140952CFT

Figure 17. On-state resistance vs. V_{CC}



GAPG2503140953CFT

Figure 18. Turn-on voltage slope

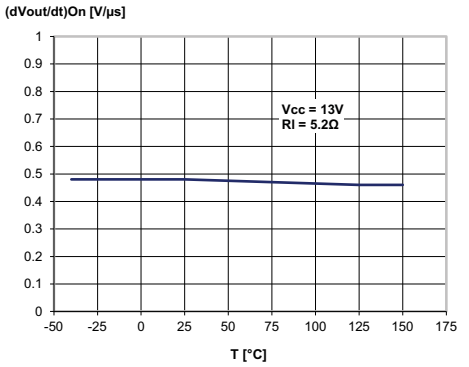


Figure 19. Turn-off voltage slope

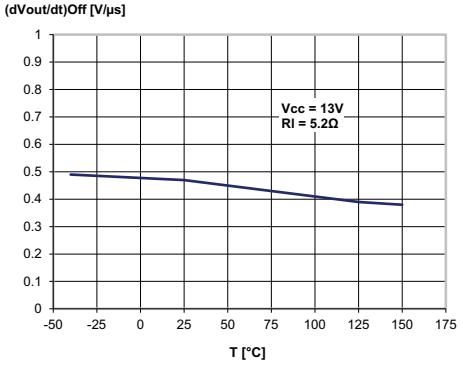


Figure 20. Won vs. T_{case}

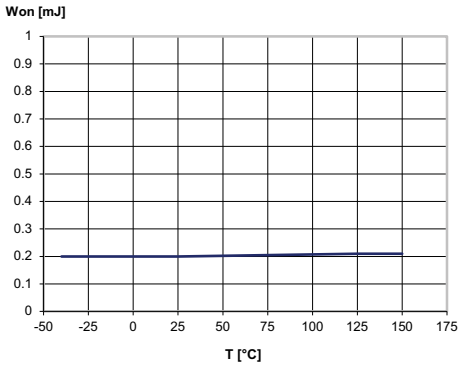


Figure 21. Woff vs. T_{case}

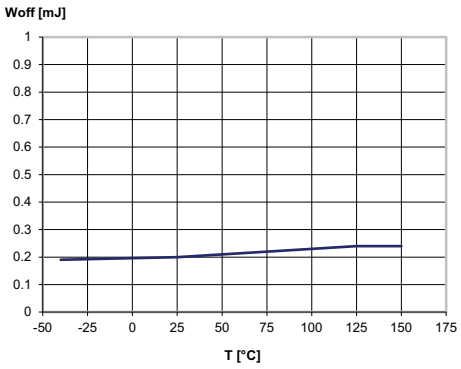


Figure 22. I_{LIMH} vs. T_{case}

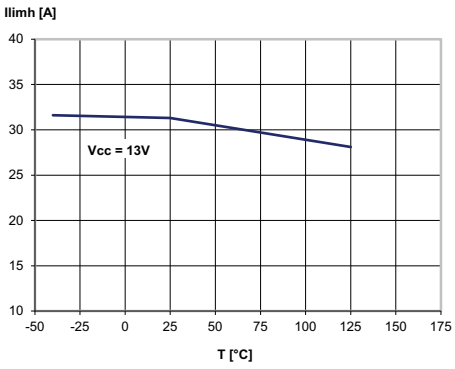


Figure 23. OFF-state open-load voltage detection threshold

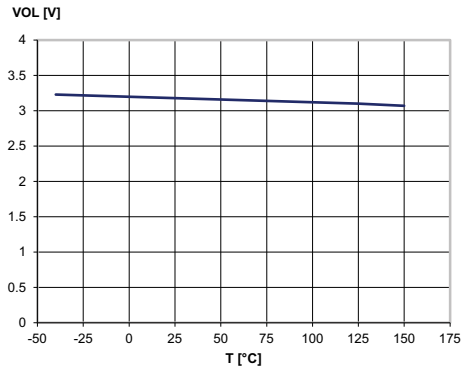


Figure 24. V_{sense} clamp vs. T_{case}

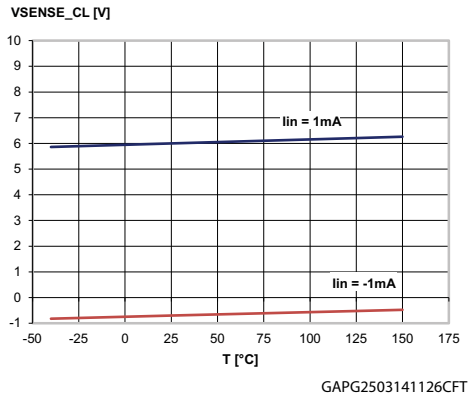
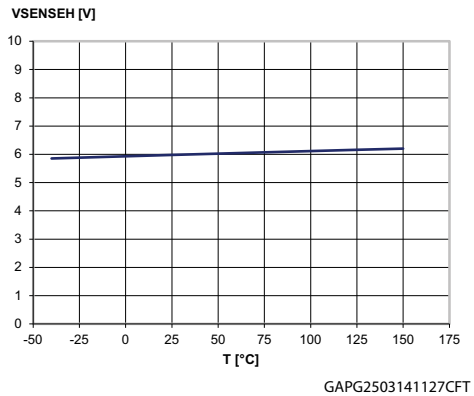


Figure 25. V_{senseh} vs. T_{case}



2.4.1 LED Mode (Channel 0 and 1)

Table 12. Switching in LED Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)\_0,1\_LED}$(1)	Turn-on delay time at T_j = 25 °C	R_L = 22.8 Ω	10	65	120	µs
$t_{d(off)\_0,1\_LED}$(1)	Turn-off delay time at T_j = 25 °C	R_L = 22.8 Ω	10	40	100	
$(dV_{OUT}/dt)_{on\_0,1\_LED}$(1)	Turn-on voltage slope at T_j = 25 °C	R_L = 22.8 Ω	0.2	0.5	0.8	V/µs
$(dV_{OUT}/dt)_{off\_0,1\_LED}$(1)	Turn-off voltage slope at T_j = 25 °C	R_L = 22.8 Ω	0.1	0.5	0.7	
$W_{ON\_0,1\_LED}$	Switching energy losses at turn-on (t_{won})	R_L = 22.8 Ω	—	0.04	0.1(2)	mJ
$W_{OFF\_0,1\_LED}$	Switching energy losses at turn-off (t_{woff})	R_L = 22.8 Ω	—	0.045	0.11(2)	mJ
$t_{SKEW\_0,1\_LED}$(1)	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 22.8 Ω	-75	-25	25	µs

1. See *Figure 35: Switching times and Pulse skew*.
2. Parameter guaranteed by design and characterization, not subject to production test.

Table 13. Power section in LED Mode (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON\_0,1\_LED}$	On-state resistance in LED Mode Ch0 and Ch1	I_{OUT} = 0.57 A; T_j = 25°C		140		mΩ
		I_{OUT} = 0.57 A; T_j = 150°C			280	
		I_{OUT} = 0.57 A; V_{CC} = 5 V; T_j = 25°C			210	
$I_{LIMH\_0,1\_LED}$(1)	DC short circuit current in Bulb Mode Ch0 and Ch1	V_{CC} = 13 V	5.5	8	11	A
		4 V < V_{CC} < 18 V(2)				
$I_{LIML\_0,1\_LED}$	Short circuit current during thermal cycling in Bulb Mode Ch0 and Ch1	V_{CC} = 13 V; T_R < T_j < T_{TSD}		2		
$V_{ON\_0,1\_LED}$	Output voltage drop limitation in LED Mode Ch0 and Ch1	I_{OUT} = 0.07 A		20		mV

1. Parameter guaranteed by an indirect test sequence.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 14. MultiSense in LED Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.01 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	120			
dK_{cal}/K_{cal}(1)(2)	Current sense ratio drift at calibration point	I_{cal} = 17.5 mA; I_{OUT} = 10 mA to 25 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-30		30	%
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	150	380	610	
dK_{LED}/K_{LED}(1)(2)	Current sense ratio drift	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
$K_{0\_CH0,1\_L}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	240	405	570	
dK_0/K_0(1)(2)	Current sense ratio drift	I_{OUT} = 0.15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-15		15	%
$K_{1\_CH0,1\_L}$	I_{OUT}/I_{SENSE}	I_{OUT} = 0.7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	300	380	460	
dK_1/K_1(1)(2)	Current sense ratio drift	I_{OUT} = 0.7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-8		8	%
MultiSense timings (Current Sense mode - see *Figure 36*)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω			60	µs

Table 14. MultiSense in LED Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω			250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 22.8 Ω		50	250	µs

1. Parameter specified by design; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Figure 26. LED Mode - I_{OUT}/I_{SENSE} versus I_{OUT}

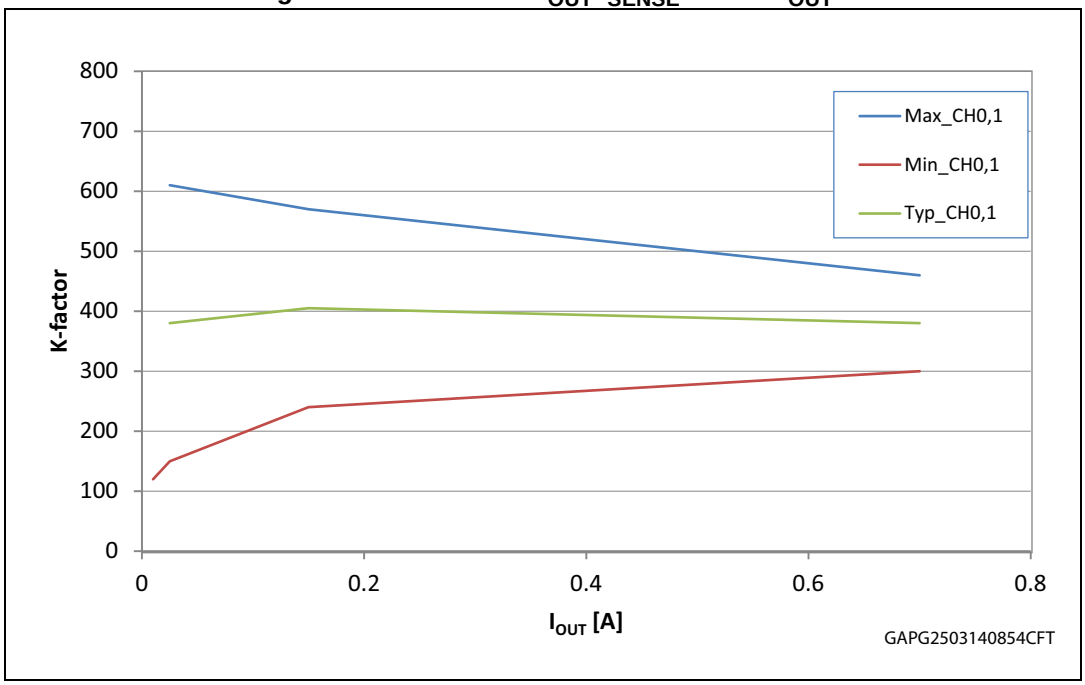
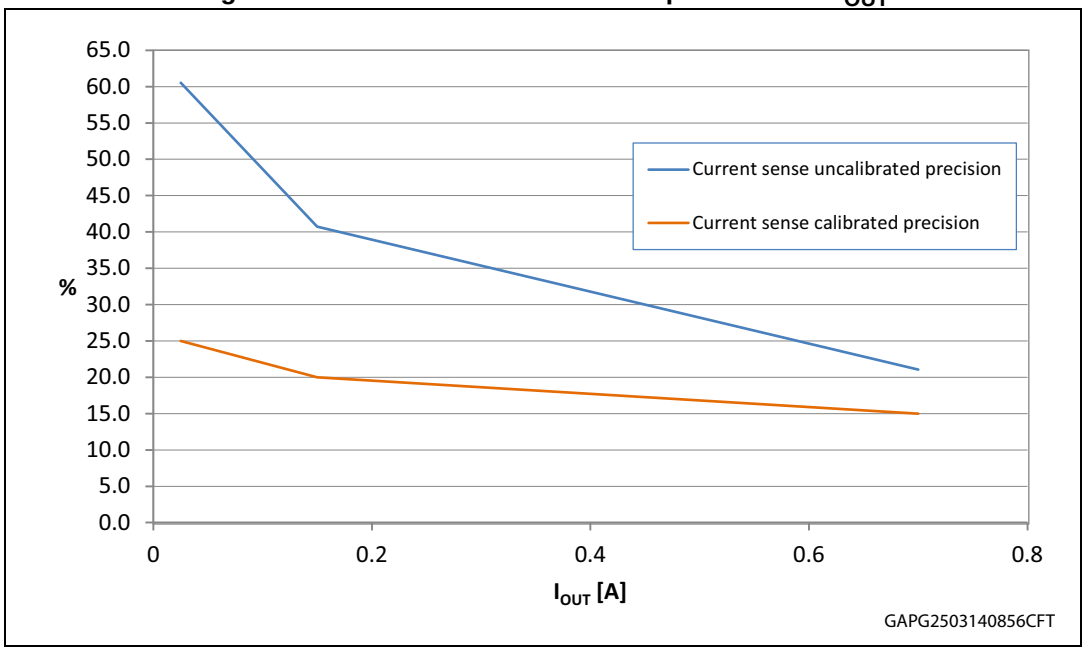


Figure 27. LED Mode - current sense precision vs. I_{OUT}



2.5 Electrical characteristics curves - LED mode

Figure 28. On-state resistance vs. T_{case}

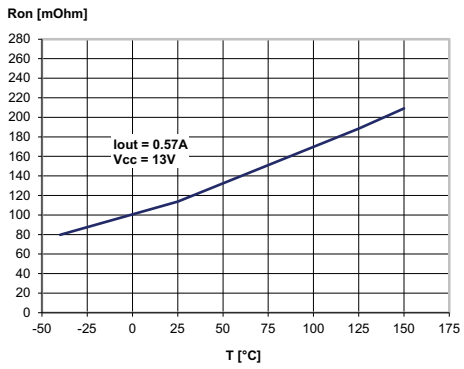


Figure 29. On-state resistance vs. V_{CC}

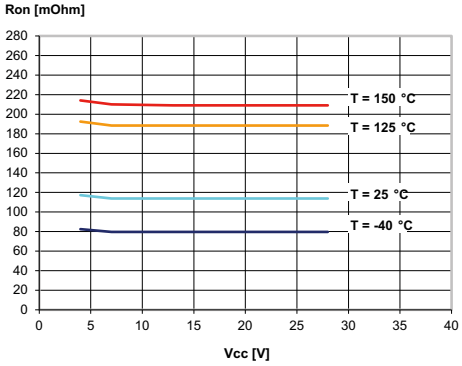


Figure 30. Turn-on voltage slope

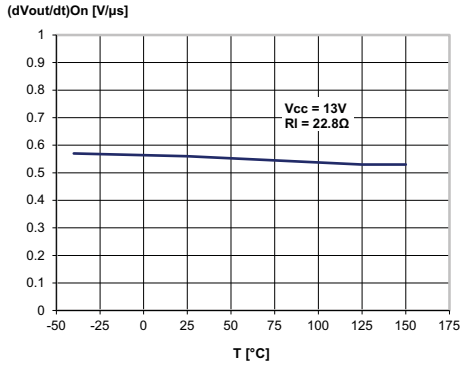


Figure 31. Turn-off voltage slope

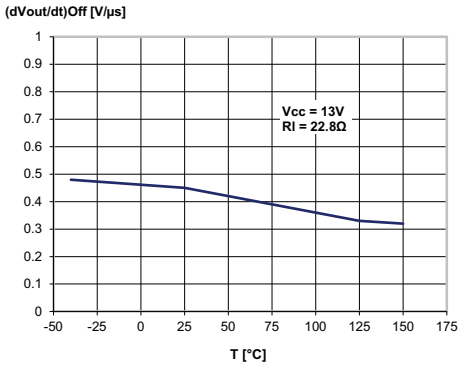


Figure 32. Won vs. T_{case}

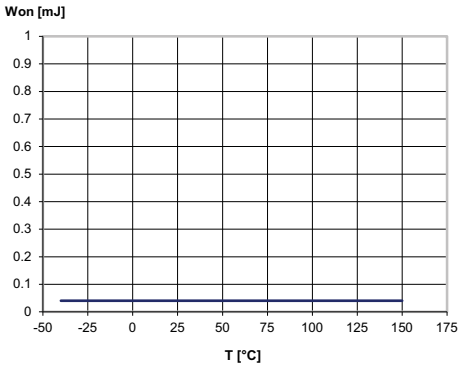


Figure 33. Woff vs. T_{case}

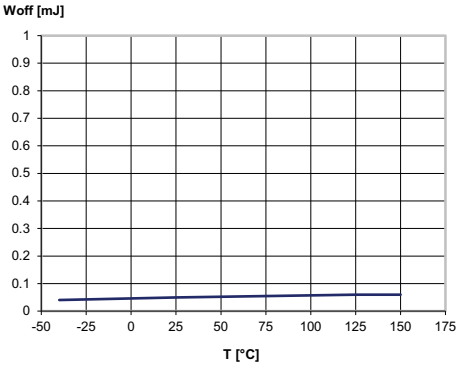


Figure 34. I_{LIMH} vs. T_{case}

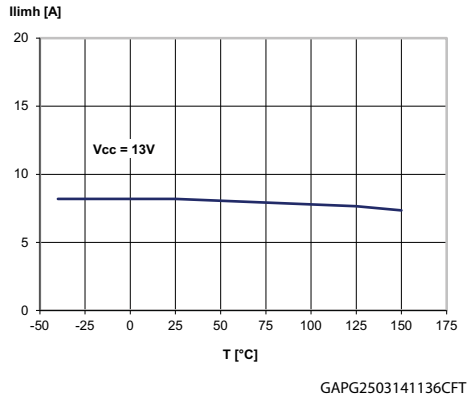


Figure 35. Switching times and Pulse skew

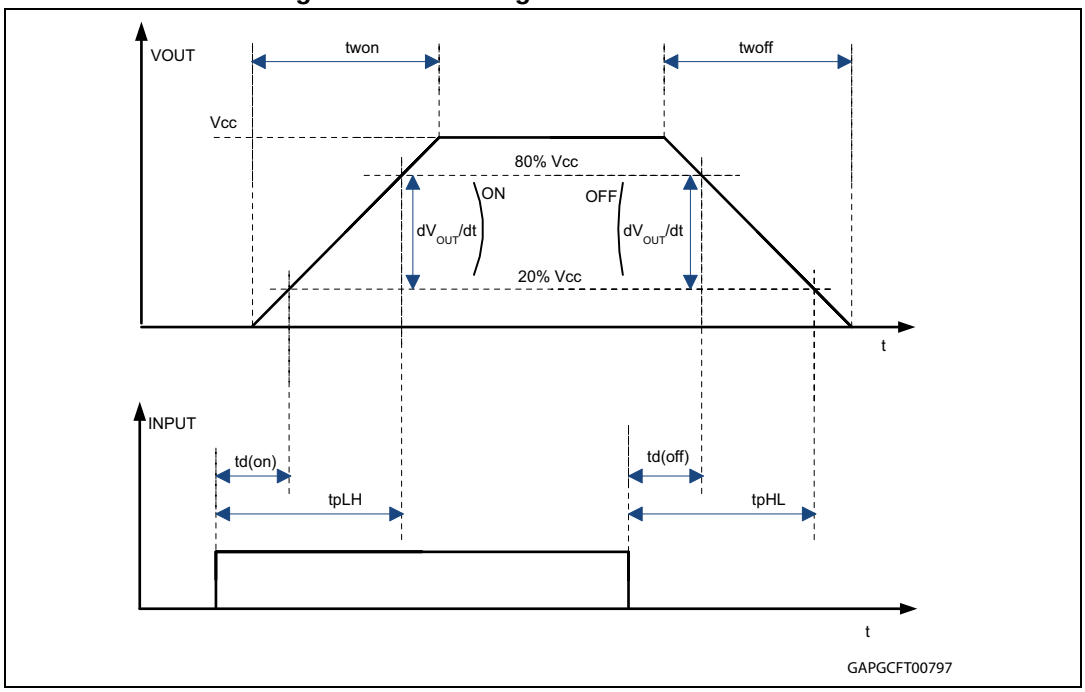


Figure 36. MultiSense timings (current sense mode)

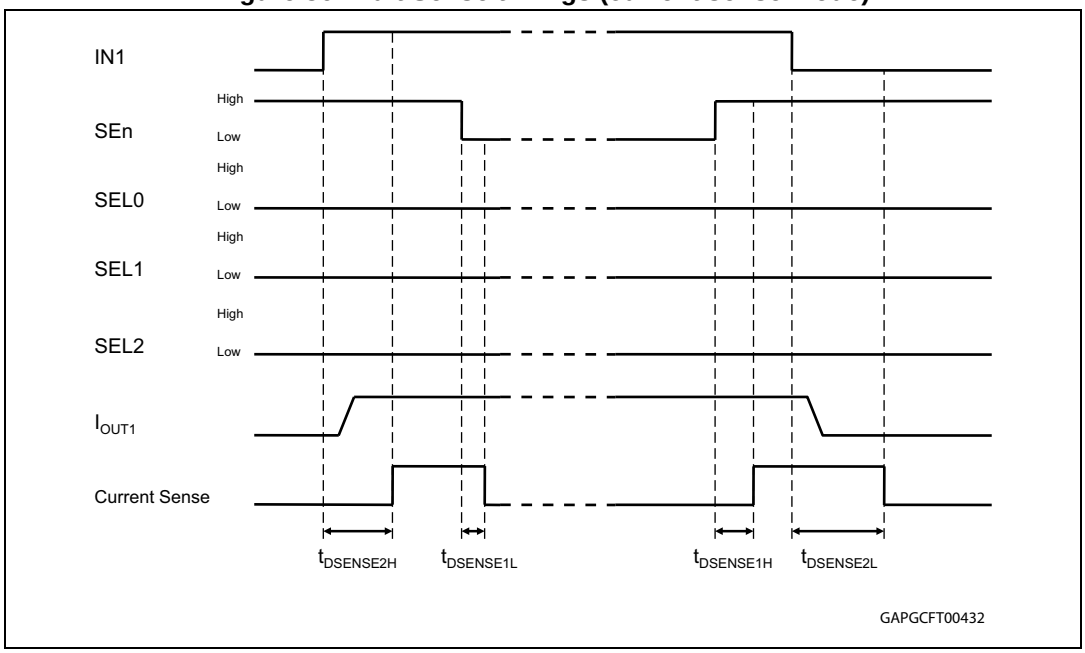


Figure 37. Multisense timings (chip temperature and V_{CC} sense mode)

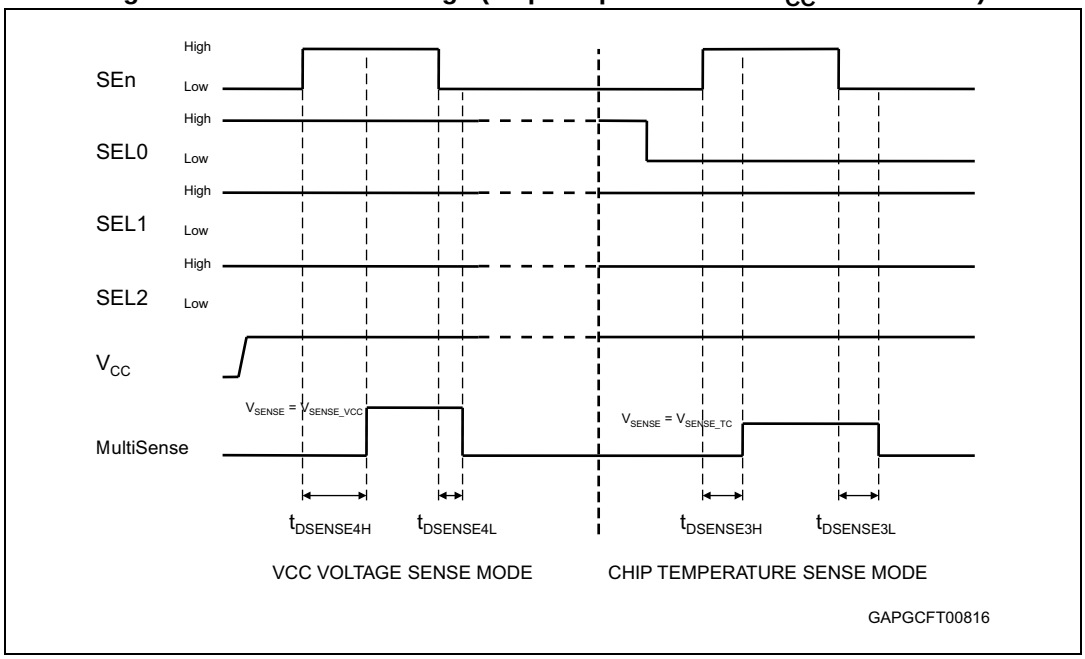
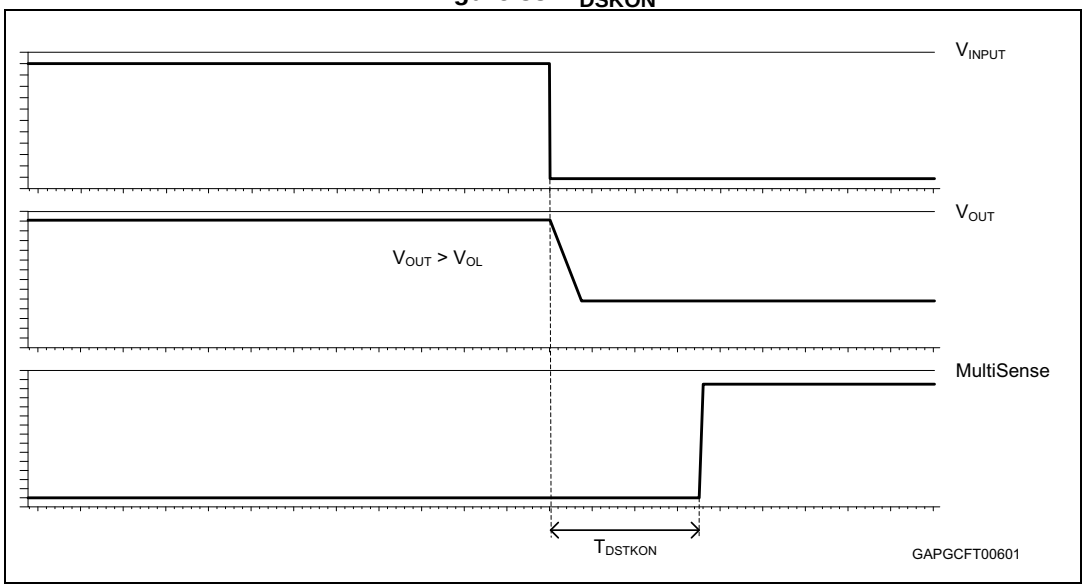


Figure 38. T_{DSKON}



2.5.1 Truth tables

Table 15. Truth table

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150°C	L	X	Refer to *Table 16*		L	Refer to *Table 16*	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	Refer to *Table 16*		L	Refer to *Table 16*	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Output latches-off
Under-voltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	Refer to *Table 16*		H	Refer to *Table 16*	
	Open load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn off	L	X	Refer to *Table 16*		< 0V	Refer to *Table 16*	

Table 16. MultiSense multiplexer addressing

SEn	SEL_2	SEL_1	SEL_0	MUX channel	MultiSense output			
					Normal mode	Overload	OFF-state diag.(1)	Negative output
L	X	X	X		Hi-Z			
H	L	L	L	Channel 0 diagnostic	I_{SENSE} = 1/K * I_{OUT0}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	L	H	Channel 1 diagnostic	I_{SENSE} = 1/K * I_{OUT1}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	L	Channel 2 diagnostic	I_{SENSE} = 1/K * I_{OUT2}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	H	Channel 3 diagnostic	I_{SENSE} = 1/K * I_{OUT3}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	H	L	L	T_{CHIP} Sense	$V_{SENSE} = V_{SENSE\_TC}$			
H	H	L	H	V_{CC} Sense	$V_{SENSE} = V_{SENSE\_VCC}$			

Table 16. MultiSense multiplexer addressing (continued)

SEn	SEL_2	SEL_1	SEL_0	MUX channel	MultiSense output			
					Normal mode	Overload	OFF-state diag.(1)	Negative output
H	H	H	L	T_{CHIP} Sense	$V_{SENSE} = V_{SENSE\_TC}$			
H	H	H	H	V_{CC} Sense	$V_{SENSE} = V_{SENSE\_VCC}$			

1. In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic.
Example 1: FR = 1; IN_0 = 0; OUT_0 = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0
Example 2: FR = 1; IN_0 = 0; OUT_0 = latched, $V_{OUT0} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

Table 17. Bulb/LED Mode Configuration

LED_1	LED_0	Configuration	
		Channel 1	Channel 0
L	L	Bulb	Bulb
L	H	Bulb	LED
H	L	LED	Bulb
H	H	LED	LED

2.5.2 Immunity to electrical transient disturbances on V_{CC} (ISO 7637-2)

Table 18. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) test pulse	Test levels (1)		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50µs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1µs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1µs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b(2)	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 19. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004E test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(1)	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 20. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (see *Table 7*, FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

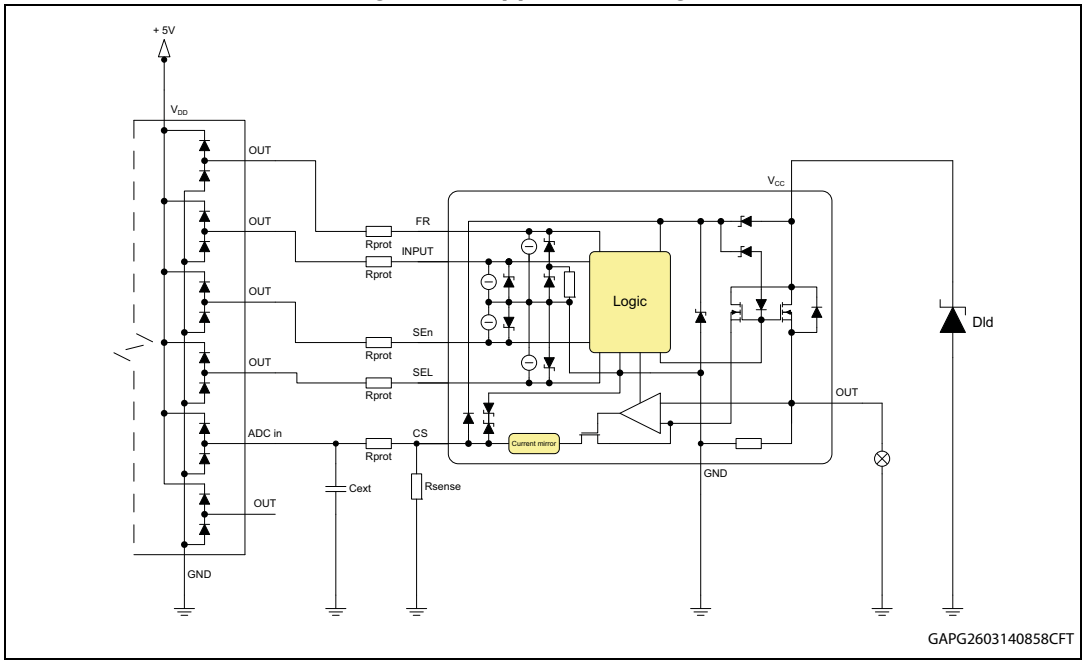
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} (see *Table 7*), allowing the inductor energy to be dissipated without damaging the device.

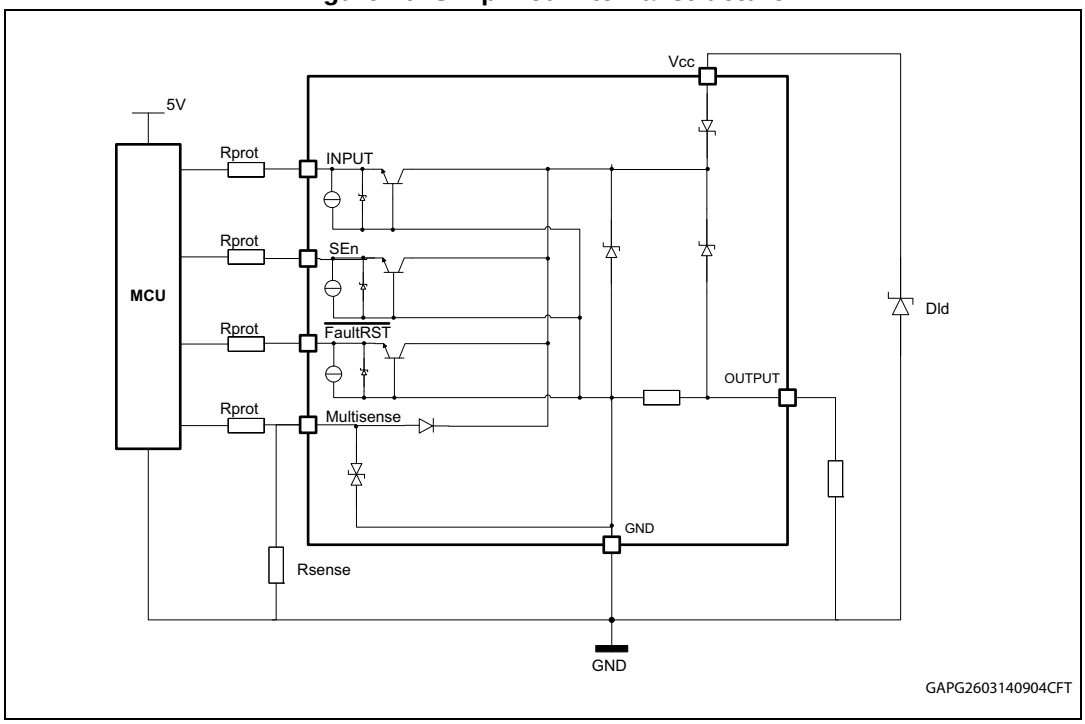
4 Application information

Figure 39. Application diagram



4.1 Protection against reverse battery

Figure 40. Simplified internal structure



The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 21*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 21. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S(1)		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50µs, 2Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1µs, 50Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1µs, 50Ω
4(2)	IV	-7V	1 pulse			100ms, 0.01Ω
Load dump according to ISO 16750-2:2010						
Test B(3)		40V	5 pulse	1 min		400ms, 2Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.
2. Test pulse from ISO 7637-2:2004(E).
3. With 40 V external suppressor referred to ground (-40°C < T_j < 150°C).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

$$7.5\ k\Omega \leq R_{prot} \leq 140\ k\Omega.$$

Recommended values: R_{prot} = 15 kΩ

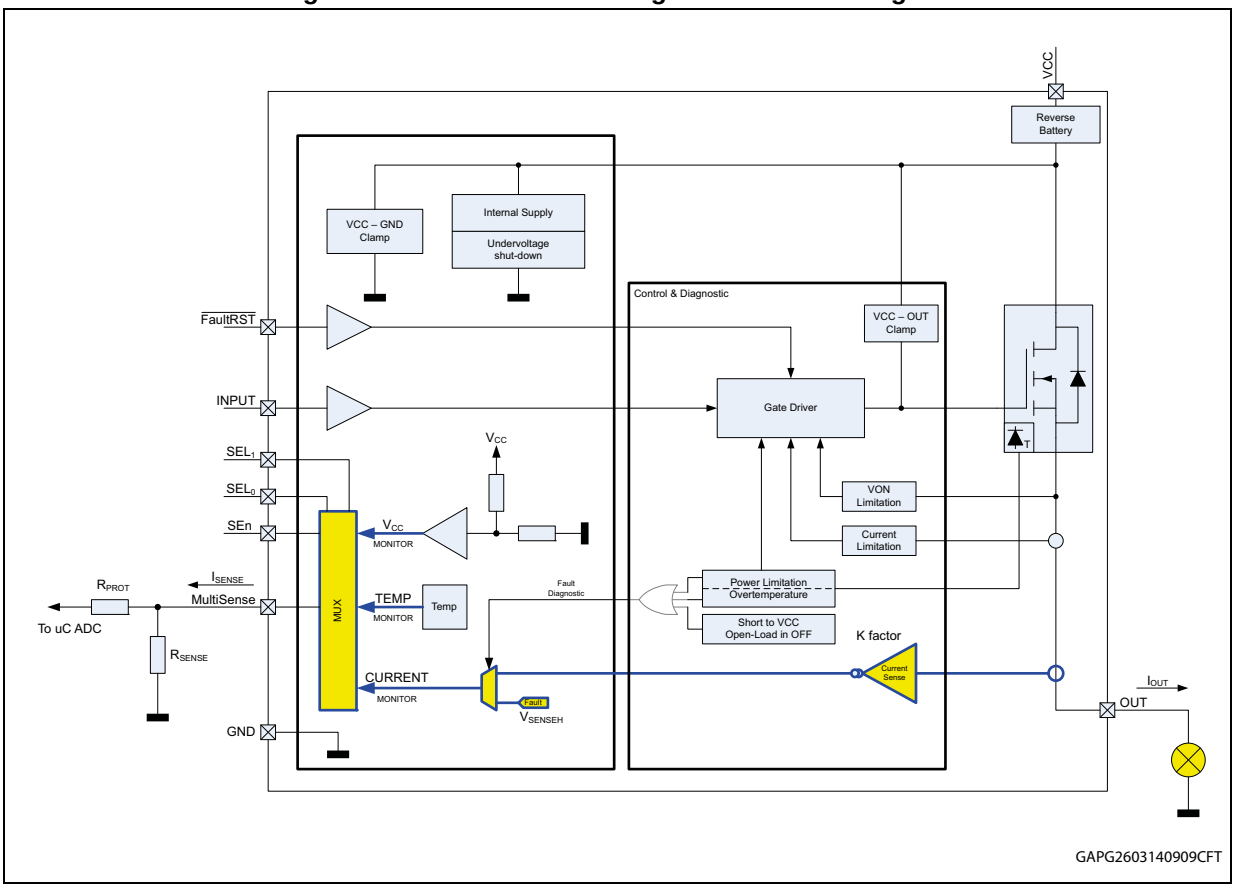
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (Multisense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage propotional to V_{CC}
- T_{CASE}: voltage propotional to chip temperature

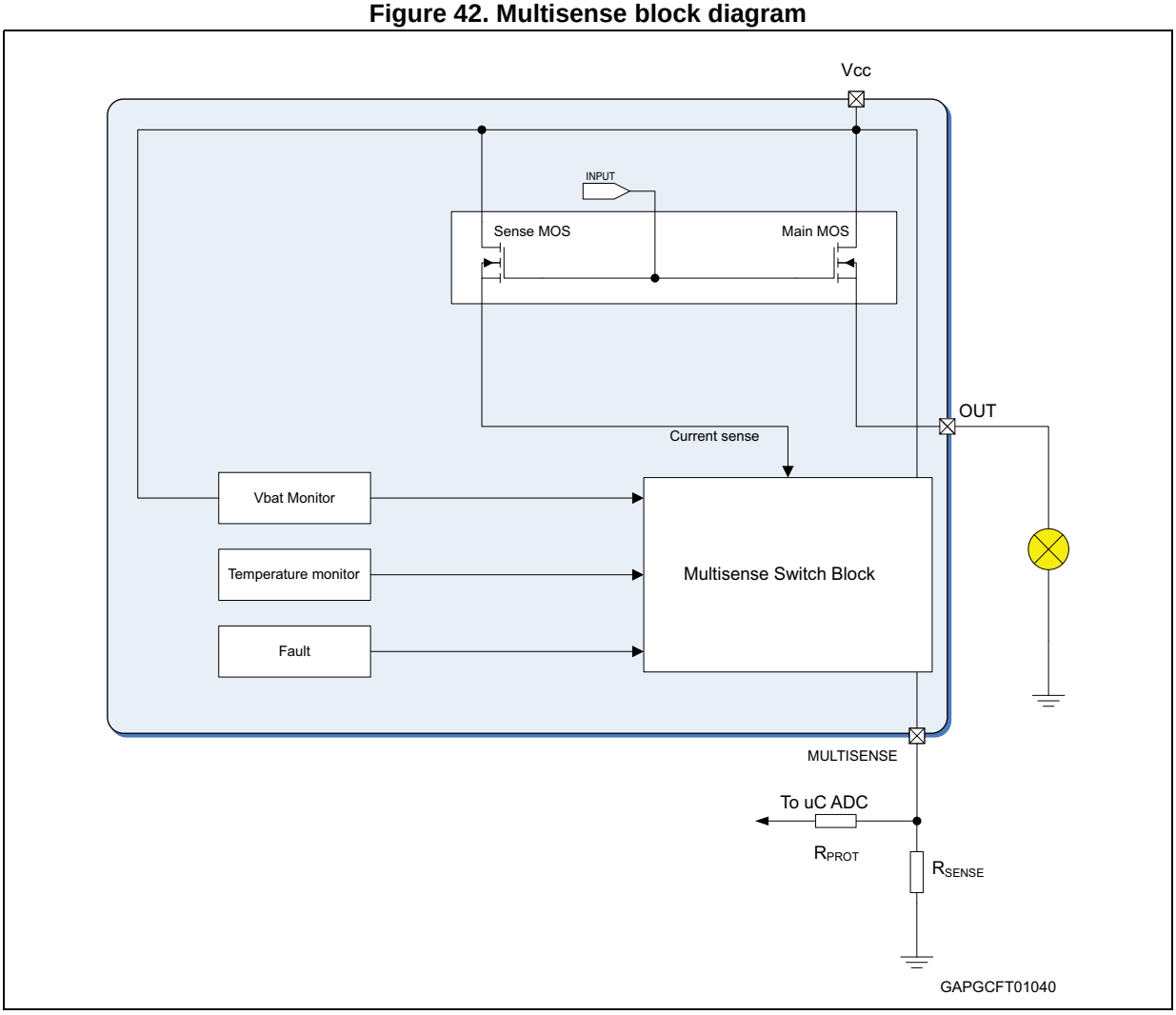
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *Table 16*.

Figure 41. Multisense and diagnostic – block diagram



4.4.1 Principle of Multisense signal generation

Figure 42. Multisense block diagram



Current monitor

When current mode is selected in the Multisense, this output is capable to provide:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by Multisense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where :

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from Multisense pin in current output mode
- I_{OUT} is current flowing through output
- K factor represent the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the Multisense pin which is switched to a “current limited” voltage source, V_{SENSEH} (see *Table 8*).

In any case, the current sourced by the Multisense in this condition is limited to I_{SENSEH} (see *Table 8*).

Figure 43. Analogue HSD – open-load detection in off-state

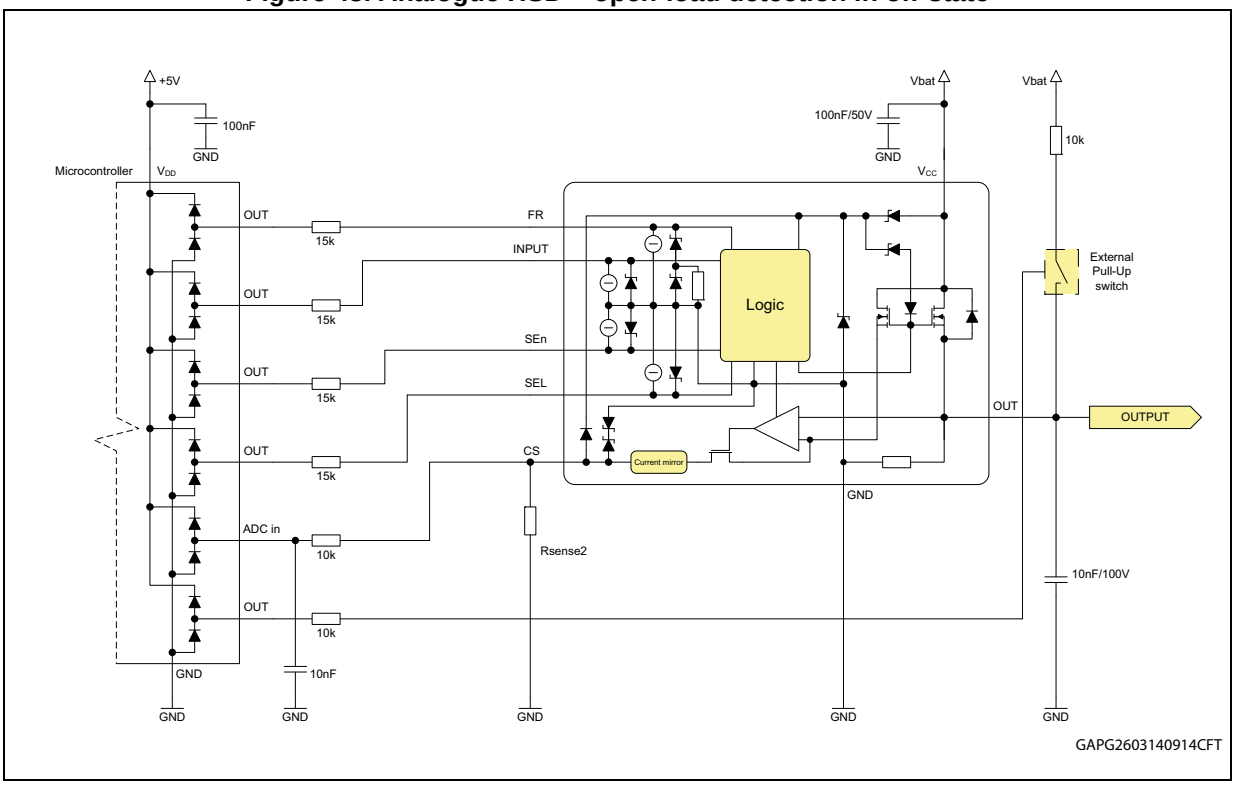


Figure 44. Open-load / short to V_{CC} condition

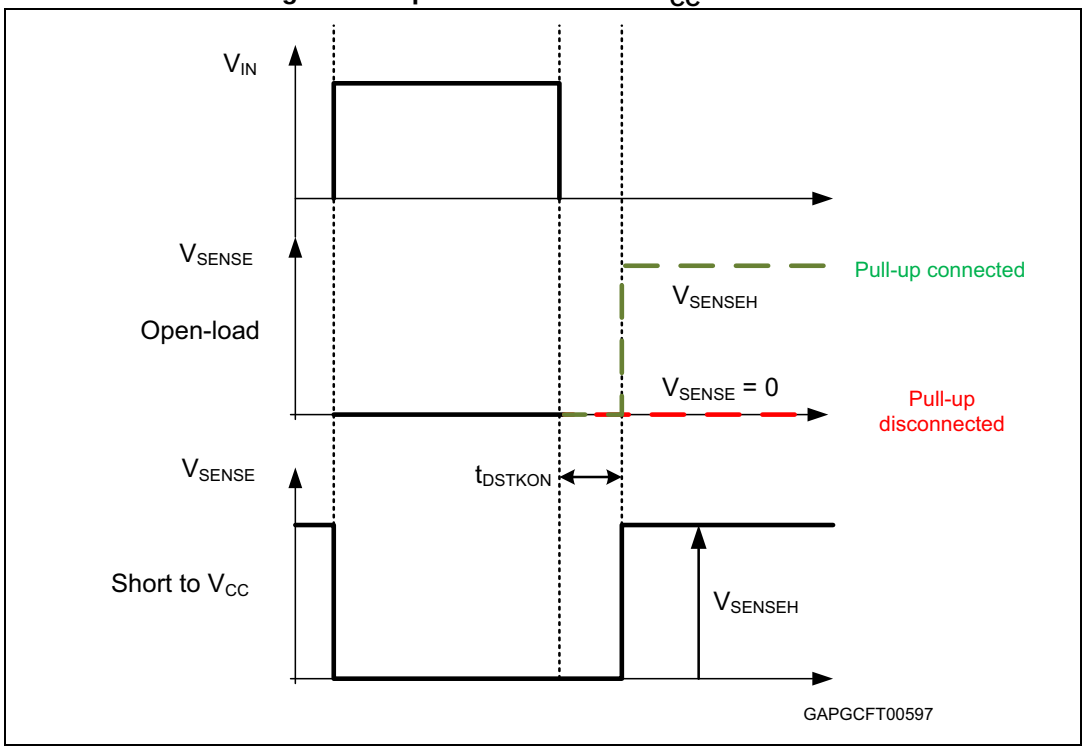


Table 22. MultiSense pin levels in off-state

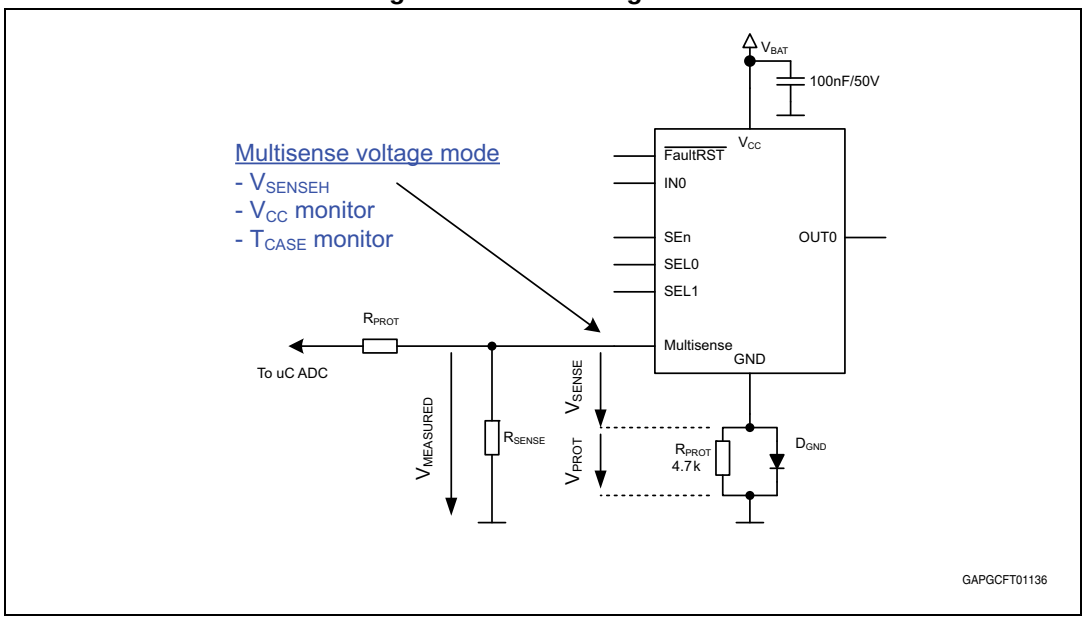
Condition	Output	MultiSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 T_{CASE} and V_{CC} monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because of a voltage shift is generated between device GND and the microcontroller input GND reference.

Figure 45 shows link between $V_{MEASURED}$ and real V_{SENSE} signal.

Figure 45. GND voltage shift



V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 4$.

Case temperature monitor

Case temperature monitor is capable to provide information about actual device temperature. Since diode is used for temperature sensing, following equation describe link between temperature and output V_{SENSE} level:

$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC} / dT * (T - T_0)$

where dV_{SENSE_TC} / dT ~ typically -5.5 mV/K (for temperature range (-40°C to +150°C).

4.4.3 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

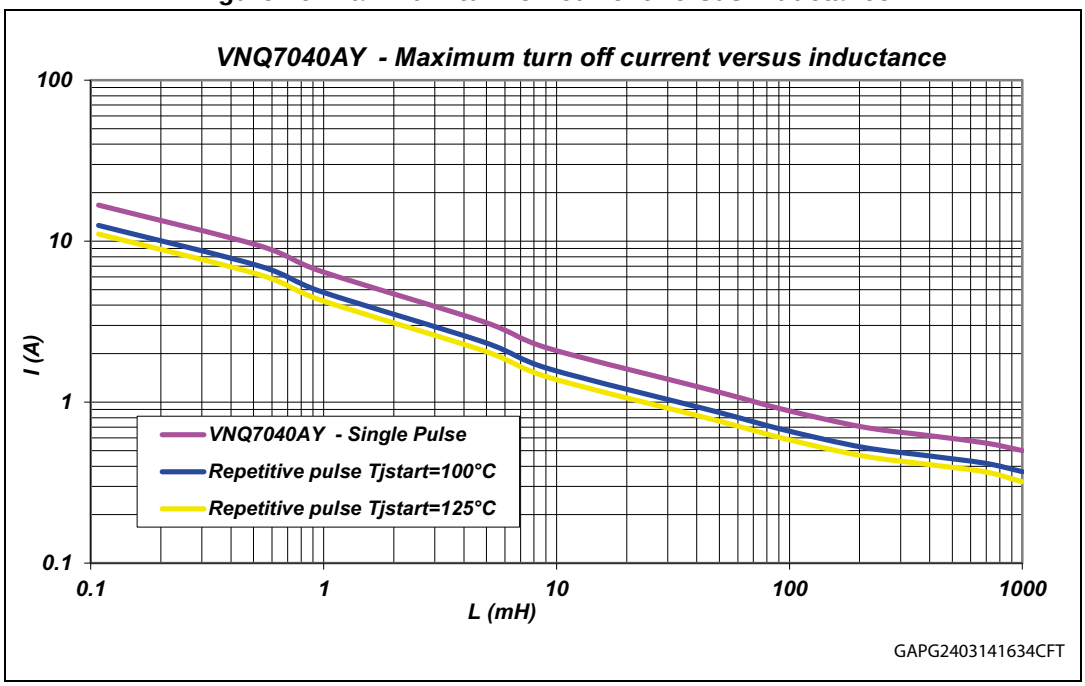
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with to following equation:

Equation 2

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

4.5 Maximum demagnetization energy (V_{CC} = 16 V)

Figure 46. Maximum turn off current versus inductance



5 Package and PCB thermal data

5.1 PowerSSO-36 thermal data

Figure 47. PowerSSO-36 PC board

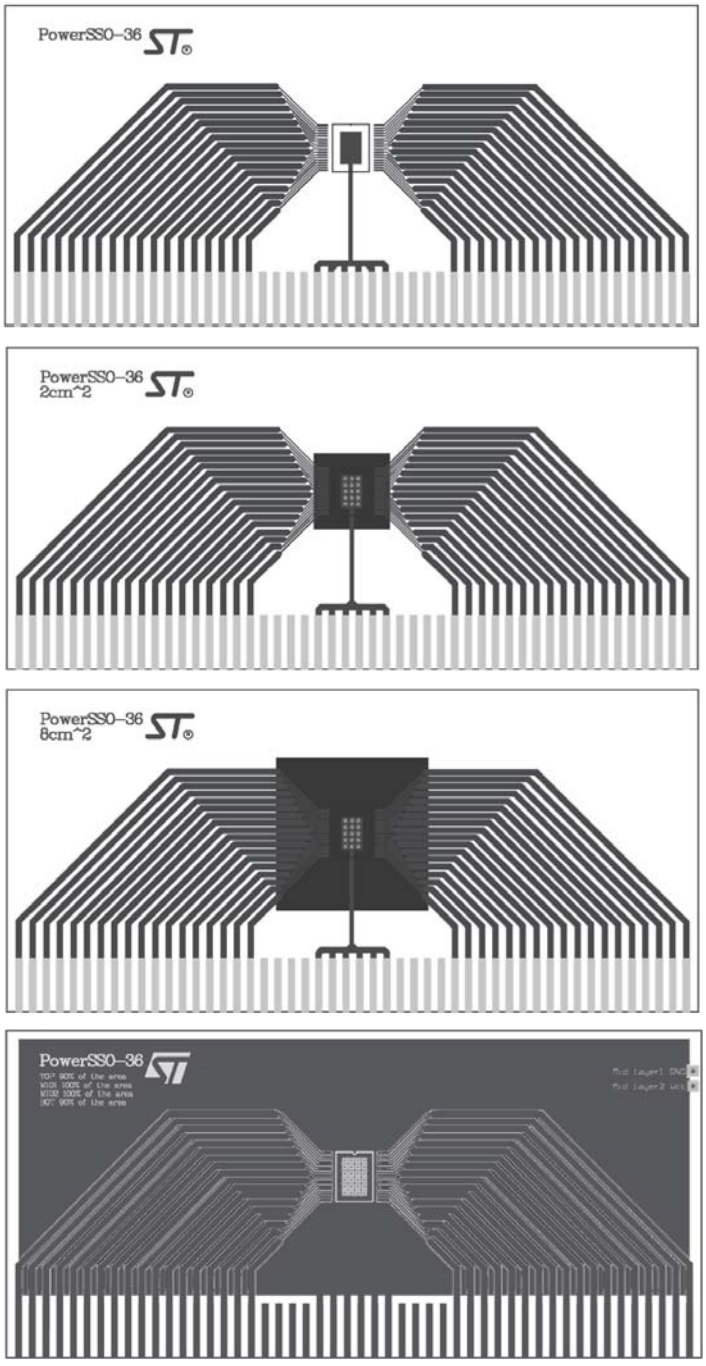


Table 23. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	129 mm x 60 mm
Board Material	FR4
Cu thickness (outer layers)	0.070 mm
Cu thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Cu thickness on vias	0.025 mm
Footprint dimension	4.1 mm x 6.5 mm

Figure 48. Rthj-amb vs PCB copper area in open box free air condition

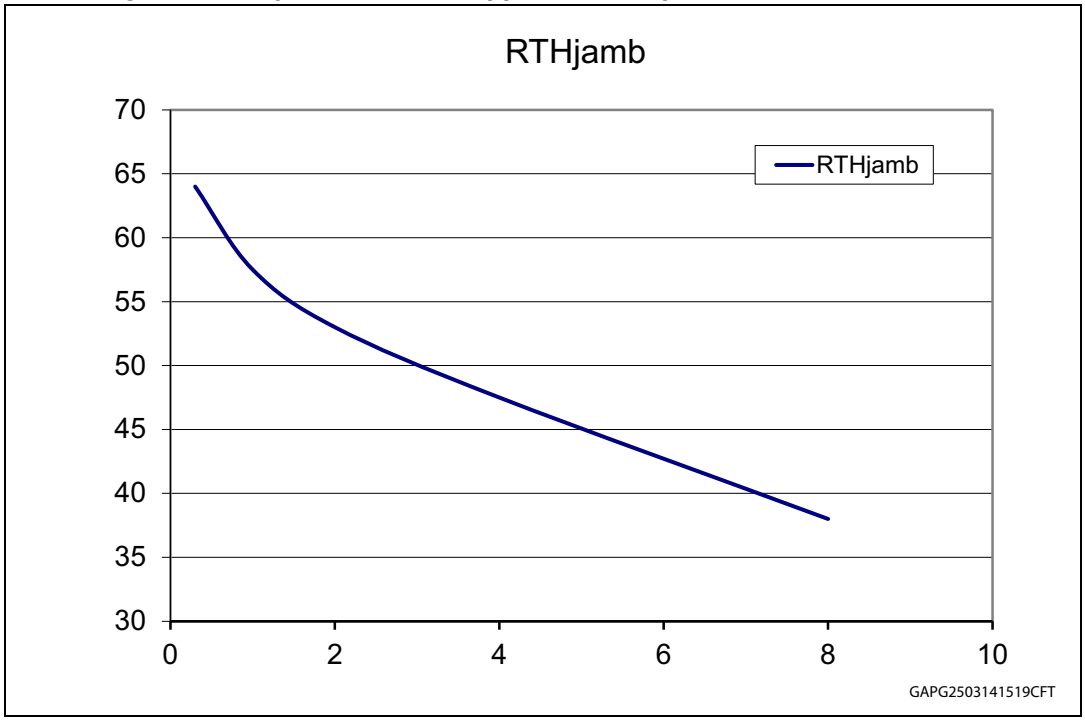


Figure 49. PowerSSO-36 thermal impedance junction ambient

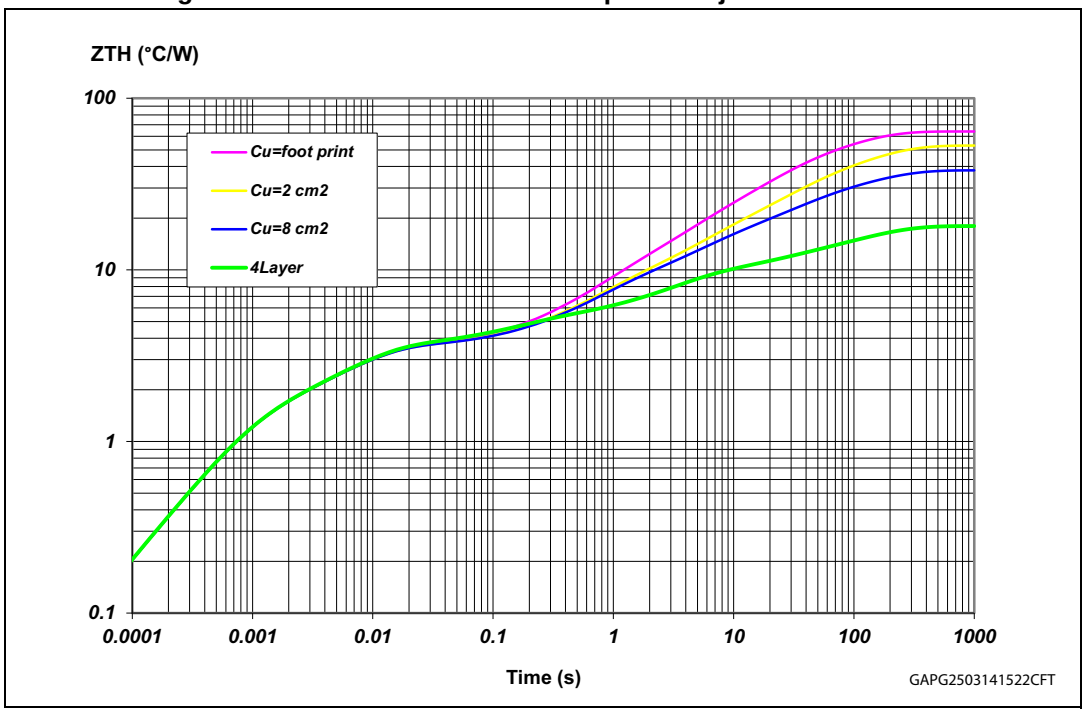


Figure 50. Thermal fitting model of a HSD in PowerSSO-36

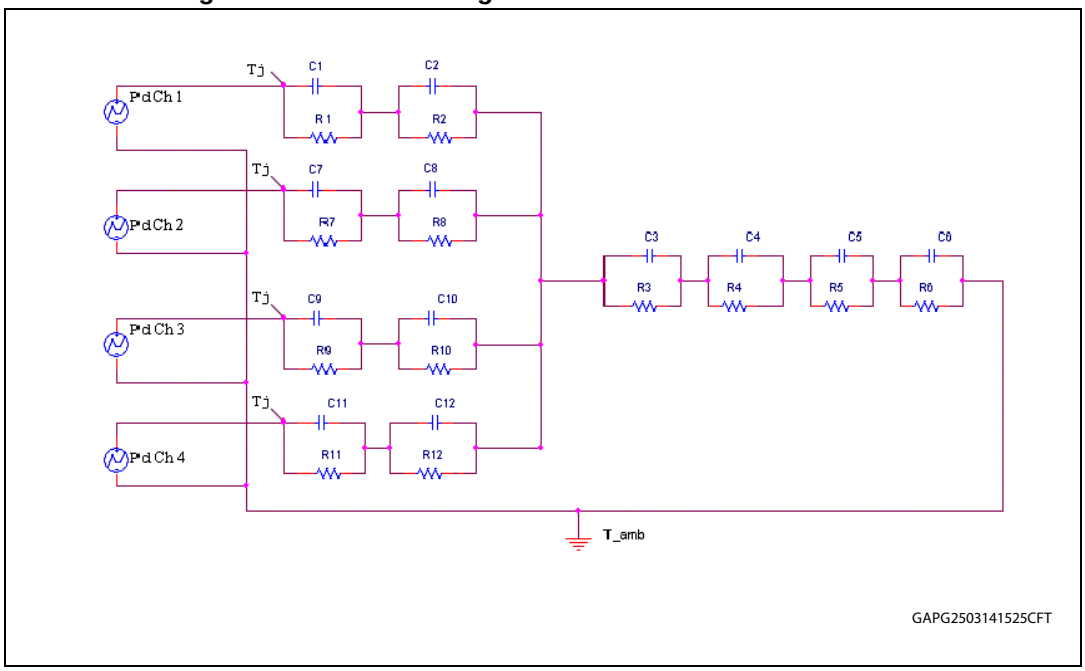


Table 24. Thermal parameters

Area/island (cm^2)	FP	2	8	4L
R1 = R7 = R9 = R11 (°C/W)	1.2			
R2 = R8 = R10 = R12 (°C/W)	2.3			
R3 (°C/W)	3.5	3.5	3.5	3.5
R4 (°C/W)	7	6	6	4
R5 (°C/W)	20	14	10	2
R6 (°C/W)	30	26	15	7
C1 = C7 = C9 = C11 (W·s/°C)	0.0006			
C2 = C8 = C10 = C12 (W·s/°C)	0.003			
C3 (W·s/°C)	0.02	0.02	0.02	0.01
C4 (W·s/°C)	0.5	0.8	0.8	0.8
C5 (W·s/°C)	1	2	3	10
C6 (W·s/°C)	3	5	9	18

6 Package information

6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 PowerSSO-36 mechanical data

Figure 51. PowerSSO-36 package dimensions

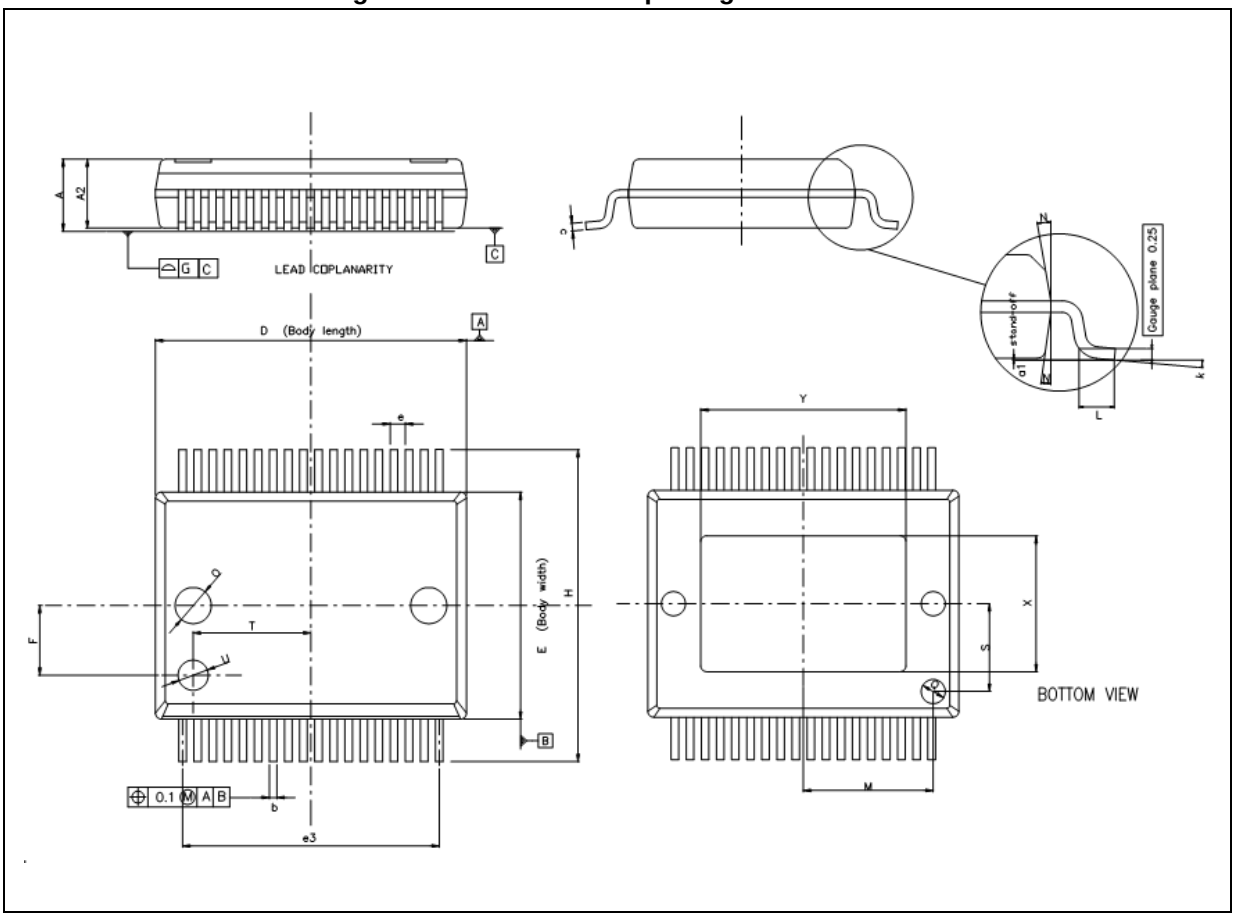


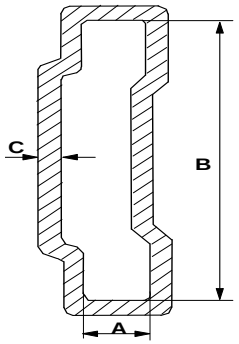
Table 25. PowerSSO-36 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.15	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1.0	-
X(1)	4.3	-	5.2
Y(1)	6.9	-	7.5

1. Corresponding to internal variation C.

6.3 Packing information

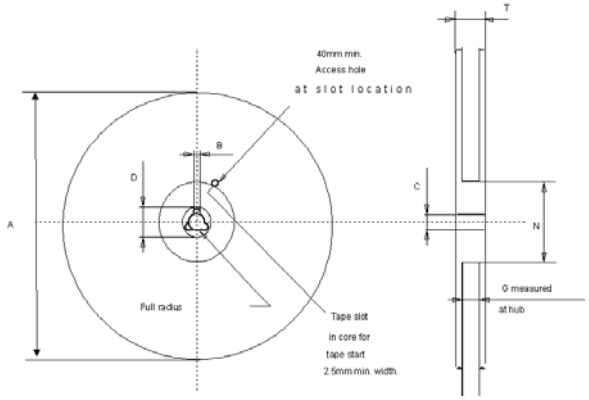
Figure 52. PowerSSO-36 tube shipment (no suffix)



Base q.ty	49
Bulk q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 53. PowerSSO-36 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

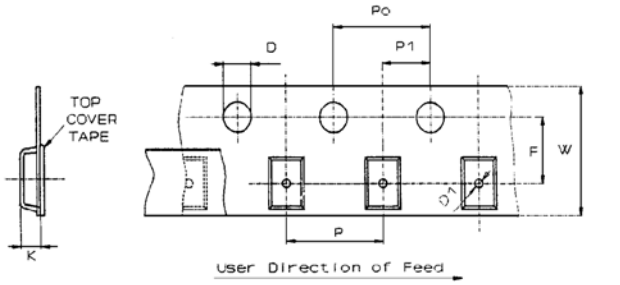
Base q.ty	1000
Bulk q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

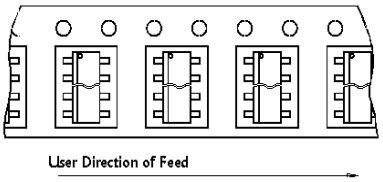
TAPE DIMENSIONS

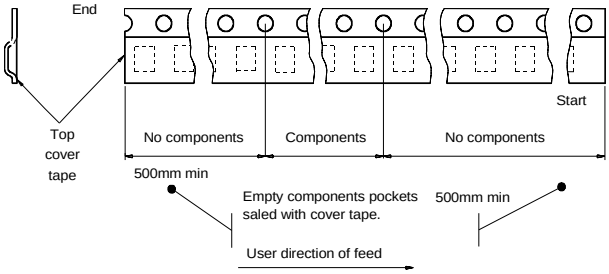
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	12
Hole diameter	**D (± 0.05)**	1.55
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.1)**	11.5
Compartment depth	**K (max)**	2.85
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







7 Order codes

Table 26. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	VNQ7040AY-E	VNQ7040AYTR-E

8 Revision history

Table 27. Document revision history

Date	Revision	Changes
14-Nov-2011	1	Initial release.
14-Feb-2013	2	Updated *Figure 2: Configuration diagram (top view)* *Table 1: Pin functions*: – GND: updated function description
20-Mar-2013	3	Updated *Features* list Updated *Table 1: Pin functions* and *Table :* *Table 3: Absolute maximum ratings*: – V_{CC}, $-V_{CC}$, V_{FR}, $-I_{OUT\_0,1}$, $-I_{OUT\_2,3}$: updated value – V_{CCPK}, I_{SENSE}, V_{ESD}: updated parameter and value – V_{CCJS}: added row – $-V_{SENSE}$: removed row Updated *Table 4: Thermal data* *Table 5: Power section*: – $V_{USDReset}$, $I_{GND(ON)}$: added row – t_{D_STBY}: updated test conditions and value – V_{clamp}, I_{STBY}, $I_{S(ON)}$, $I_{L(off)}$: updated test conditions row *Table 7: Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*: – V_{DEMAG}, T_{HYST}: updated value – t_{LATCH_RST}: updated test conditions and values *Table 8: MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*: – V_{SENSE_CL}, V_{OL}, t_{STKON}, t_{D_VOL}, $t_{DSENSE3H}$, $t_{DSENSE3L}$, $t_{DSENSE4H}$, $t_{DSENSE4L}$, t_{D_XtoY}, t_{D_CStoTC}, t_{D_TCtoCS}, $t_{D\_CStoVCC}$, $t_{D\_VCCtoCS}$, $t_{D\_TCtoVCC}$, $t_{D\_VCCtoTC}$, $t_{D\_CStoVSENSEH}$: updated test conditions – I_{SENSE0}, $I_{L(off2)}$, V_{SENSE_TC}, V_{SENSE_VCC}, V_{SENSEH}: updated test conditions and values – V_{OUT_MSD}, V_{SENSE_SAT}, I_{SENSE_SAT}, $I_{OUT\_SAT\_BULB}$, $I_{OUT\_SAT\_LED}$, $t_{D\_OL\_V}$: added rows – I_{SENSEH}: updated value *Table 9: Power section in Bulb Mode (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified)*: – $R_{ON\_0,1,2,3\_BULB}$: updated test conditions and values – $R_{ON\_REV\_0,1,2,3}$: updated value Updated *Table 10: Switching in Bulb Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)*, *Table 11: MultiSense in Bulb Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*, *Table 12: Switching in LED Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)* and *Table 14: MultiSense in LED Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)* Removed *Figure: Switching times* and *Figure: Pulse skew* Added *Figure 35: Switching times and Pulse skew* Updated *Figure 36: MultiSense timings (current sense mode)* and *Figure 37: Multisense timings (chip temperature and VCC sense mode)*

Table 27. Document revision history (continued)

Date	Revision	Changes
20-Mar-2013	3 (cont'd)	Added *Figure 38: T_{DSKON}* *Table 15: Truth table*: – Overload: updated conditions Updated *Table 16: MultiSense multiplexer addressing* Removed *Section: Waveforms*
22-Jul-2013	4	*Table 10: Switching in Bulb Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)*: – $t_{SKEW\_0,1,2,3}$: updated values Updated *Table 11: MultiSense in Bulb Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)* *Table 12: Switching in LED Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)*: – $t_{SKEW\_0,1\_LED}$: updated values Updated *Table 14: MultiSense in LED Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*
18-Sep-2013	5	Updated disclaimer.
11-Feb-2014	6	Updated *Table 10: Switching in Bulb Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)* and *Table 12: Switching in LED Mode (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)*
19-Jun-2014	7	*Table 3: Absolute maximum ratings*: – E_{MAX}: updated value *Table 4: Thermal data* Added *Figure 4: Bulb Mode - I_{OUT}/I_{SENSE} versus I_{OUT}* and *Figure 5: Bulb Mode - current sense precision vs. I_{OUT}* Added *Section 2.4: Electrical characteristics curves - Bulb Mode* Added *Figure 26: LED Mode - I_{OUT}/I_{SENSE} versus I_{OUT}* and *Figure 27: LED Mode - current sense precision vs. I_{OUT}* Added *Section 2.5: Electrical characteristics curves - LED mode* Removed *Section: Immunity to electrical transient disturbances on VCC (ISO 7637-2)* Added *Chapter 3: Protections*, *Chapter 4: Application information* and *Chapter 5: Package and PCB thermal data*
30-Sep-2014	8	Updated *Chapter 5: Package and PCB thermal data*

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