CBTL12131

DisplayPort multiplexer for bidirectional video in all-in-one computer systems

Rev. 1 — 25 February 2011 Product data sheet

1. General description

CBTL12131 is an integrated DisplayPort high-speed path switch/multiplexer that allows all-in-one computer systems to efficiently manage path switching between different display modes of operation. With the CBTL12131, video can be routed either from one DisplayPort source (GPU1) to an integrated DisplayPort panel and simultaneously from a second DisplayPort source (GPU2) to an external DisplayPort sink; or from an external DisplayPort source to the integrated DisplayPort panel.

The device is configured as four main Ports A through D, each providing four high-speed differential lanes for DisplayPort Main Link (ML) channels, one high-speed differential lane for the DisplayPort AUX channel, and one single-ended lane for the HPD (Hot Plug Detect) signal. One port (Port A) provides an additional alternate lane for the AUX channel, in order to allow bypassing of external AC-coupling capacitors for support of the DDC channel in case an external connected sink is a '++DP' type cable adapter.

For the path supporting the 'external source to integrated DisplayPort panel' mode, a programmable equalizer is provided which allows compensation for channel loss that the external source or internal sink are unable to adequately compensate for. The equalizer is self-biasing and is programmable to five gain-frequency curves, of which one is a flat response and four are active equalization. The equalizer output can also be set to one of two levels of pre-emphasis (including flat), and also differential swing level can be set to one of two levels. All options (EQ, pre-emphasis, level) are easily programmed using board-strapping (resistor, short or open) of three unique Quinary Input programming pins.

The CBTL12131 includes additional features that support use of the external DisplayPort connector in both directions: either an external sink (monitor or cable adapter) or external source (notebook computer) can be connected, while CBTL12131 configures the direction and termination of the related signals accordingly. The port facing the external DisplayPort connector (Port B) is equipped with dedicated sensing circuitry which detects and reports the status of the HPD and AUX lines, to support the system controller in determining and setting the proper connection status. The AUX channel of Port B also has switchable integrated termination, to allow the system controller to apply the correct DC termination in case an external DisplayPort source is connected. Moreover, it affords the system controller the means to detect the type of system (sink, source or all-in-one computer) connected at Port B, and apply the proper termination required in each scenario.

The CBTL12131 is powered from a single 3.3 V power supply, consumes very little current while providing low insertion loss and low return loss high-speed differential switch channels suitable for use in DisplayPort v1.1a interconnect. All switch and configuration settings can be performed by board-strapping or driving simple CMOS inputs—no software or bus configuration is required. CBTL12131 is available in a 6 mm × 6 mm

TFBGA64 package with 0.5 mm ball pitch; owing to its high level of integration and versatility, it is eminently suitable for use in computers employing bidirectional DisplayPort video.

2. Features and benefits

2.1 High-speed DisplayPort Main Link multiplexing

- Switch path topologies supporting:
  - ‘dual through’ mode (two GPUs to two displays simultaneously)
  - ‘external source’ mode (external source to internal display)
- Supports DisplayPort v1.1a at 2.7 Gbit/s
- High-bandwidth analog pass-gate technology
- Configurable equalization in ‘external source’ mode path
- Pre-emphasis level control for equalizer in ‘external source’ mode path
- Very low intra-pair differential skew of < 5 ps
- Very low inter-pair skew of < 180 ps

2.2 DDC and AUX multiplexing

- Switch path topologies supporting:
  - ‘dual through’ mode (two GPUs to two displays)
  - ‘external source’ mode (external source to internal display)
- ‘AC coupling bypass’ mode on Port A (for external ++DP sink)
- Supports DisplayPort v1.1a AUX channel
- Supports DDC/I^2C-bus multiplexing
- High-bandwidth analog pass-gate technology

2.3 HPD channel management

- Active logic management of HPD signals
- Bidirectional HPD I/O for external connector (Port B)
- HPD input for integrated DisplayPort display (Port D)
- Two HPD outputs to both GPUs, one for internal (Port C) and one for external video (Port A)
- 5 V tolerance on all HPD inputs
- 3.3 V LVTTL logic output levels for all HPD outputs
- Internal 200 kΩ pull-down resistor on Port B and Port D HPD input ensures default LOW when no sink is connected

2.4 Link state detection, configuration and reporting

- Detection of DC state of AUX_P and AUX_N lines of external display (Port B)
- Filtering of HPD interrupt pulse from external display (Port B)
- Reporting of detected/filtered Port B AUX and HPD states via CMOS outputs (to external system controller)
- AUX channel bias control inputs for Port B to allow configuration as source or sink

- Integrated high-ohmic pull-down (4.7 MΩ) and switchable 100 kΩ and 500 kΩ resistors for Port B AUX bias control

2.5 Equalizer

- Programmable equalizer for channel loss compensation from Port B to Port D (external source mode)
- Five levels of input equalization (including flat)
- Two levels of output pre-emphasis (including flat)
- Two output voltage swing levels
- Three quinary input control pins allow equalization, pre-emphasis and output voltage swing selection by simple board strapping

2.6 General

- Power supply 3.3 V ± 10 %
- Low active mode supply current of 30 mA typical (Dual-through mode)
- Active mode supply current of 120 mA typical (External source mode, EQ = on)
- ESD resilience to 4 kV HBM, 1 kV CDM
- Available in TFBGA64 6 mm × 6 mm package

3. Typical system configuration

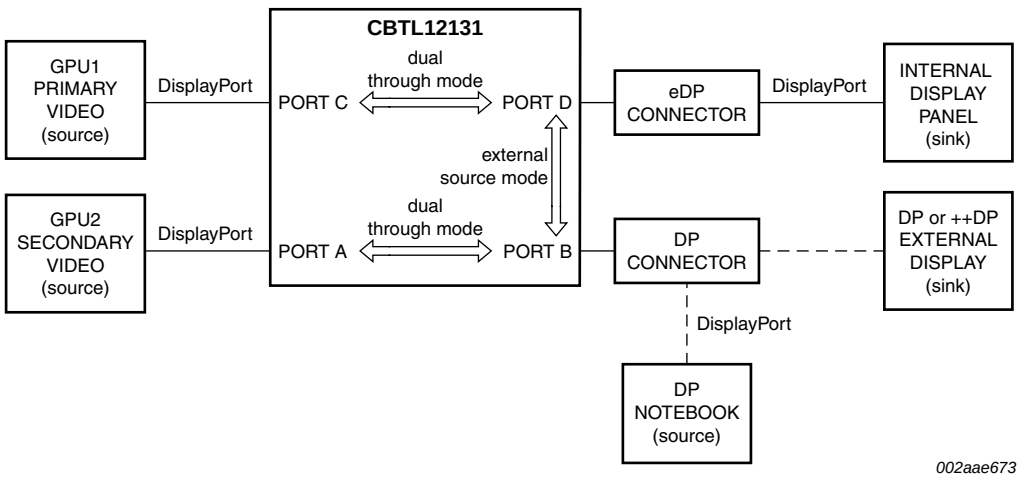


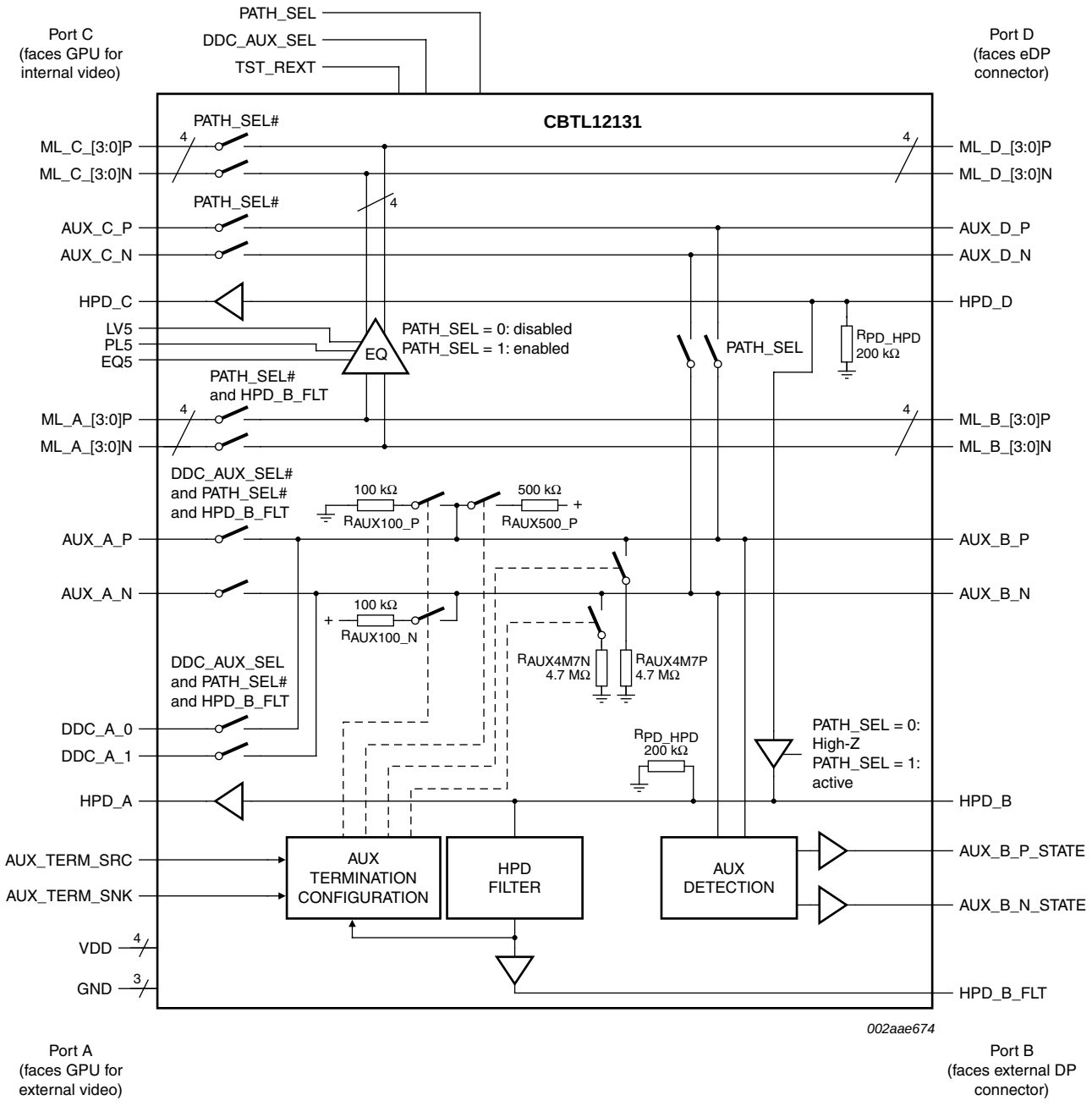
Fig 1. CBTL12131 in typical system configuration

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
CBTL12131ET	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls; body 6 × 6 × 0.8 mm	SOT543-1

5. Functional diagram



(1) Switch is in ON (conducting) position when qualifier = TRUE.

Fig 2. Functional diagram

6. Pinning information

6.1 Pinning

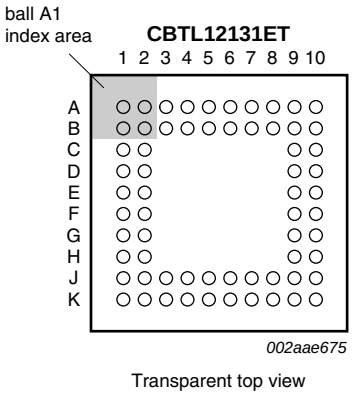


Fig 3. Pin configuration for TFBGA64

	Port D (faces eDP connector)					Port B (faces external DP connector)				
	1	2	3	4	5	6	7	8	9	10
A	ML_D_0P	ML_D_1P	ML_D_2P	ML_D_3P	HPD_D	HPD_B	ML_B_0P	ML_B_1P	ML_B_2P	ML_B_3P
B	ML_D_0N	ML_D_1N	ML_D_2N	ML_D_3N	VDD	GND	ML_B_0N	ML_B_1N	ML_B_2N	ML_B_3N
C	AUX_D_P	AUX_D_N							AUX_B_N	AUX_B_P
D	AUX_B_P_STATE	AUX_B_N_STATE							PL5	DDC_AUX_SEL
E	PATH_SEL	VDD							VDD	EQ5
F	TST_REXT	GND				Transparent top view			LV5	HPD_B_FLT
G	AUX_TERM_SRC	AUX_TERM_SNK							DDC_A_1	DDC_A_0
H	AUX_C_P	AUX_C_N							AUX_A_N	AUX_A_P
J	ML_C_0N	ML_C_1N	ML_C_2N	ML_C_3N	VDD	GND	ML_A_0N	ML_A_1N	ML_A_2N	ML_A_3N
K	ML_C_0P	ML_C_1P	ML_C_2P	ML_C_3P	HPD_C	HPD_A	ML_A_0P	ML_A_1P	ML_A_2P	ML_A_3P

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Port C (faces GPU for internal video)

Port A (faces GPU for external video)

Fig 4. Ball mapping for TFBGA64

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
Control inputs			
PATH_SEL	E1	3.3 V low-voltage CMOS single-ended input	Input to set the path configuration of the CBTL12131. When LOW, Ports A and B are mutually connected, as well as Ports C and D. When HIGH, Port B is connected to Port D.
DDC_AUX_SEL	D10	3.3 V low-voltage CMOS single-ended input	Input to select between DDC and AUX terminals for Port A. When HIGH, the DDC_A_P and DDC_A_N terminals are connected to their respective AUX_B_P and AUX_B_N terminals on Port B. When LOW, the AUX_A_P and AUX_A_N terminals are connected to their respective AUX_B_P and AUX_B_N terminals on Port B.
EQ5	E10	3.3 V low-voltage CMOS quinary input	Equalizer setting input pin. This pin can be board-strapped to one of five decode values: short to GND, resistor to GND, open-circuit, resistor to VDD, short to VDD. See Table 7 for truth table.
PL5	D9	3.3 V low-voltage CMOS quinary input	Pre-emphasis level setting input pin. This pin can be board-strapped to one of five decode values: short to GND, resistor to GND, open-circuit, resistor to VDD, short to VDD. See Table 8 for truth table.
LV5	F9	3.3 V low-voltage CMOS quinary input	Output differential swing setting input pin. This pin can be board-strapped to one of five decode values: short to GND, resistor to GND, open-circuit, resistor to VDD, short to VDD. See Table 9 for truth table.
TST_REXT	F1	3.3 V low-voltage CMOS single-ended input with current sensing analog input	Test pin for NXP use, combined with external current sensing function. Should be tied to ground via an external resistor of value 10 kΩ ± 1 %. This pin must not be left open-circuit to avoid possible erroneous engagement of test mode in normal operation.
AUX_TERM_SRC	G1	3.3 V low-voltage CMOS single-ended input	Input to enable source-type termination on the Port B AUX pair. When HIGH, 100 kΩ termination resistors are applied to the Port B AUX pair. When LOW, the termination resistors will be disabled (high-impedance).
AUX_TERM_SNK	G2	3.3 V low-voltage CMOS single-ended input	Input to enable sink-style termination on the Port B AUX pair. When HIGH, a 500 kΩ termination resistor to VDD is applied to AUX_B_P. When LOW, the termination resistor will be disabled (high-impedance).
Status outputs			
HPD_B_FLT	F10	3.3 V low-voltage CMOS single-ended output	This outputs a filtered version of HPD_B.
AUX_B_P_STATE	D1	3.3 V low-voltage CMOS single-ended output	DC state (HIGH or LOW) of AUX_B_P signal.
AUX_B_N_STATE	D2	3.3 V low-voltage CMOS single-ended output	DC state (HIGH or LOW) of AUX_B_N signal.

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
Port A terminals			
ML_A_0P	K7	differential port terminal	Four high-speed differential pairs for DisplayPort Main Link signals, Port A. Designated as port facing the GPU for external video. Port A will be exclusively connected to Port B when PATH_SEL = LOW, and will be high-impedance when PATH_SEL = HIGH.
ML_A_0N	J7	differential port terminal	
ML_A_1P	K8	differential port terminal	
ML_A_1N	J8	differential port terminal	
ML_A_2P	K9	differential port terminal	
ML_A_2N	J9	differential port terminal	
ML_A_3P	K10	differential port terminal	
ML_A_3N	J10	differential port terminal	
AUX_A_P	H10	differential port terminal	High-speed differential pair for DisplayPort AUX signals, Port A. These terminals are active when DDC_AUX_SEL = LOW only; when DDC_AUX_SEL = HIGH, these are high-impedance.
AUX_A_N	H9	differential port terminal	
DDC_A_0	G10	differential port terminal	Port A terminal intended for AUX AC coupling capacitor bypass. These terminals are active when DDC_AUX_SEL = HIGH only; when DDC_AUX_SEL = LOW, these are high-impedance.
DDC_A_1	G9	differential port terminal	
HPD_A	K6	3.3 V LVTTL single-ended output	3.3 V LVTTL HPD output for Port A. When PATH_SEL = LOW, this output follows the state of HPD_B (from external DP or ++DP sink). When PATH_SEL = HIGH, this output is always LOW.
Port B terminals			
ML_B_0P	A7	differential port terminal	Four high-speed differential pairs for DisplayPort Main Link signals, Port B. Designated as port facing the external DP connector. Port B will be exclusively connected to Port A when PATH_SEL = LOW **and** HPD_B_FLT = HIGH, and will be exclusively connected to Port D when PATH_SEL = HIGH. When PATH_SEL = HIGH, the signal ordering and association to Port D ML signals is automatically corrected by internal routing, to map to the DP connector's inverted signal ordering for a DP sink-side connector.
ML_B_0N	B7	differential port terminal	
ML_B_1P	A8	differential port terminal	
ML_B_1N	B8	differential port terminal	
ML_B_2P	A9	differential port terminal	
ML_B_2N	B9	differential port terminal	
ML_B_3P	A10	differential port terminal	
ML_B_3N	B10	differential port terminal	
AUX_B_P	C10	differential port terminal	High-speed differential pair for DisplayPort AUX signals, Port B.
AUX_B_N	C9	differential port terminal	
HPD_B	A6	3.3 V bidirectional LVTTL I/O with high-Z state	HPD input with 5 V tolerance or output for Port B, to be connected to the external DP connector. When PATH_SEL = LOW, HPD_B is configured as input (from external DP or ++DP sink). When PATH_SEL = HIGH, HPD_B is configured as output and follows the state of HPD_D (from internal sink), to be connected via DP connector to an external DP source.

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
Port C terminals			
ML_C_0P	K1	differential port terminal	Four high-speed differential pairs for DisplayPort Main Link signals, Port C. Designated as port facing the GPU for internal video. Port C will be exclusively connected to Port D when PATH_SEL = LOW, and will be high-impedance when PATH_SEL = HIGH.
ML_C_0N	J1	differential port terminal	
ML_C_1P	K2	differential port terminal	
ML_C_1N	J2	differential port terminal	
ML_C_2P	K3	differential port terminal	
ML_C_2N	J3	differential port terminal	
ML_C_3P	K4	differential port terminal	
ML_C_3N	J4	differential port terminal	
AUX_C_P	H1	differential port terminal	High-speed differential pair for DisplayPort AUX signals, Port C.
AUX_C_N	H2	differential port terminal	
HPD_C	K5	3.3 V LVTTL single-ended output	3.3 V LVTTL HPD output for Port C. When PATH_SEL = LOW, this output follows the state of HPD_D (from internal sink). When PATH_SEL = HIGH, this output is always LOW.
Port D terminals			
ML_D_0P	A1	differential port terminal	Four high-speed differential pairs for DisplayPort Main Link signals, Port D. Designated as port facing the internal eDP display module connector. Port D will be exclusively connected to Port C when PATH_SEL = LOW, and will be exclusively connected to Port B when PATH_SEL = HIGH.
ML_D_0N	B1	differential port terminal	
ML_D_1P	A2	differential port terminal	
ML_D_1N	B2	differential port terminal	
ML_D_2P	A3	differential port terminal	
ML_D_2N	B3	differential port terminal	
ML_D_3P	A4	differential port terminal	
ML_D_3N	B4	differential port terminal	
AUX_D_P	C1	differential port terminal	High-speed differential pair for DisplayPort AUX signals, Port D.
AUX_D_N	C2	differential port terminal	
HPD_D	A5	3.3 V LVTTL single-ended input	5 V tolerant HPD input for Port D, to be connected to the internal sink.
Supply and ground			
VDD	B5, E2, E9, J5	power supply	3.3 V power supply pins.
GND	B6, F2, J6	ground	Ground pins.

7. Functional description

7.1 General

The CBTL12131 is a high-bandwidth DisplayPort channel switching device designed for use in all-in-one computers. It contains high-bandwidth switches arranged between four Ports (A through D) to allow two different channel topologies, where each channel comprises a Main Link (ML), AUX and HPD path for comprehensive DisplayPort channel switching. One can select between two basic configurations: either Ports A and C are connected to Ports B and D respectively, or Port B is connected to Port D while Ports A and C are high-impedance. In addition, the CBTL12131 includes circuitry to assist in detection and configuration of Port B designated as the port facing the external DisplayPort connector. This section describes these functional blocks in detail.

7.2 Main Link DisplayPort switches/multiplexers

The Main Link path topology provides for four differential pairs in each Port, and an equalizer for each differential pair in the path from Port B to Port D, as shown in Figure 5. The Main Link switches are operated by CMOS input PATH_SEL and further qualified by the state of internally derived signal HPD_B_FLT (see Section 7.6 for details). When PATH_SEL is LOW, Ports C and D are mutually connected, Ports A and B are mutually connected only when HPD_B_FLT is HIGH, and the equalizer is turned off (isolating). When PATH_SEL is HIGH, Ports A and C are disconnected (high-impedance) and Port D is connected to Port B via the equalizer. The equalizer can by bypassed or configured by quinary input EQ5 to any of five equalizer settings (including a flat response) depending on specific application conditions. For details on the Equalizer function, please refer to Section 7.7.

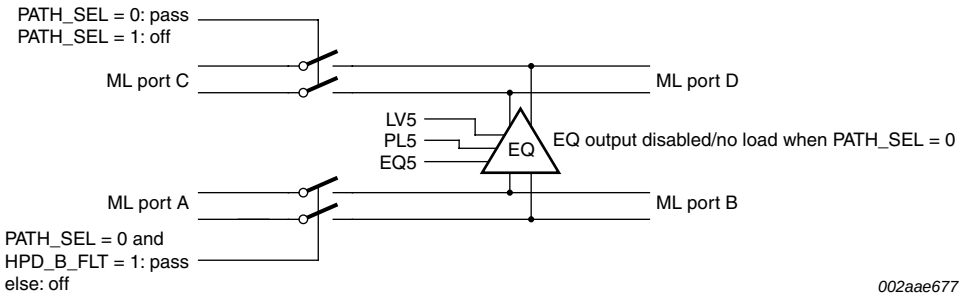


Fig 5. Main Link channel topology

Table 3. Main Link channel configuration

Legend: high-Z = isolating, high-impedance; ACT = active, low-impedance.

Inputs		Channels			Comment
PATH_SEL	HPD_B_FLT	Port C - Port D	Port A - Port B	Port B - Port D	
0	0	ACT	high-Z	high-Z	Normal mode; internal display only
0	1	ACT	ACT	high-Z	Normal mode with dual display
1	0	high-Z	high-Z	ACT	External source mode with internal display not yet asserting HPD
1	1	high-Z	high-Z	ACT	External source mode with internal display asserting HPD

Table 4. Main Link signal mappings

Legend: high-Z = isolating, high-impedance; ACT = active, low-impedance; EQ = active, equalized/re-driven.

Inputs		Channels									Comment (all other ports shall be mutually isolated)
PATH_SEL	HPD_B_FLT	Port C - Port D			Port A - Port B			Port B - Port D[1]			
0	0	ML_C_0P	ACT	ML_D_0P	ML_A_0P	high-Z	ML_B_0P	ML_B_0P	high-Z	ML_D_3N	Normal mode; internal display only
		ML_C_0N	ACT	ML_D_0N	ML_A_0N	high-Z	ML_B_0N	ML_B_0N	high-Z	ML_D_3P	
		ML_C_1P	ACT	ML_D_1P	ML_A_1P	high-Z	ML_B_1P	ML_B_1P	high-Z	ML_D_2N	
		ML_C_1N	ACT	ML_D_1N	ML_A_1N	high-Z	ML_B_1N	ML_B_1N	high-Z	ML_D_2P	
		ML_C_2P	ACT	ML_D_2P	ML_A_2P	high-Z	ML_B_2P	ML_B_2P	high-Z	ML_D_1N	
		ML_C_2N	ACT	ML_D_2N	ML_A_2N	high-Z	ML_B_2N	ML_B_2N	high-Z	ML_D_1P	
		ML_C_3P	ACT	ML_D_3P	ML_A_3P	high-Z	ML_B_3P	ML_B_3P	high-Z	ML_D_0N	
		ML_C_3N	ACT	ML_D_3N	ML_A_3N	high-Z	ML_B_3N	ML_B_3N	high-Z	ML_D_0P	
0	1	ML_C_0P	ACT	ML_D_0P	ML_A_0P	ACT	ML_B_0P	ML_B_0P	high-Z	ML_D_3N	Normal mode with dual display
		ML_C_0N	ACT	ML_D_0N	ML_A_0N	ACT	ML_B_0N	ML_B_0N	high-Z	ML_D_3P	
		ML_C_1P	ACT	ML_D_1P	ML_A_1P	ACT	ML_B_1P	ML_B_1P	high-Z	ML_D_2N	
		ML_C_1N	ACT	ML_D_1N	ML_A_1N	ACT	ML_B_1N	ML_B_1N	high-Z	ML_D_2P	
		ML_C_2P	ACT	ML_D_2P	ML_A_2P	ACT	ML_B_2P	ML_B_2P	high-Z	ML_D_1N	
		ML_C_2N	ACT	ML_D_2N	ML_A_2N	ACT	ML_B_2N	ML_B_2N	high-Z	ML_D_1P	
		ML_C_3P	ACT	ML_D_3P	ML_A_3P	ACT	ML_B_3P	ML_B_3P	high-Z	ML_D_0N	
		ML_C_3N	ACT	ML_D_3N	ML_A_3N	ACT	ML_B_3N	ML_B_3N	high-Z	ML_D_0P	
1	X	ML_C_0P	high-Z	ML_D_0P	ML_A_0P	high-Z	ML_B_0P	ML_B_0P	EQ	ML_D_3N	External source mode
		ML_C_0N	high-Z	ML_D_0N	ML_A_0N	high-Z	ML_B_0N	ML_B_0N	EQ	ML_D_3P	
		ML_C_1P	high-Z	ML_D_1P	ML_A_1P	high-Z	ML_B_1P	ML_B_1P	EQ	ML_D_2N	
		ML_C_1N	high-Z	ML_D_1N	ML_A_1N	high-Z	ML_B_1N	ML_B_1N	EQ	ML_D_2P	
		ML_C_2P	high-Z	ML_D_2P	ML_A_2P	high-Z	ML_B_2P	ML_B_2P	EQ	ML_D_1N	
		ML_C_2N	high-Z	ML_D_2N	ML_A_2N	high-Z	ML_B_2N	ML_B_2N	EQ	ML_D_1P	
		ML_C_3P	high-Z	ML_D_3P	ML_A_3P	high-Z	ML_B_3P	ML_B_3P	EQ	ML_D_0N	
		ML_C_3N	high-Z	ML_D_3N	ML_A_3N	high-Z	ML_B_3N	ML_B_3N	EQ	ML_D_0P	

[1] **Remark:** Signal ordering between Port B and Port D is inverted in order to achieve proper signal-to-pin mapping in accordance with sink side status of connector at Port B.

7.3 AUX and DDC switches/multiplexers

For all ports except Port A, only a single pair of signal lines is provided. The path configuration for the AUX/DDC channels follows that of the Main Link: when PATH_SEL = LOW, Ports C and D are connected; when PATH_SEL = LOW **and** HPD_B_FLT = HIGH, also Ports A and B are connected; when PATH_SEL = HIGH, Port D is connected to Port B, and Ports A and C are isolated (see Figure 6).

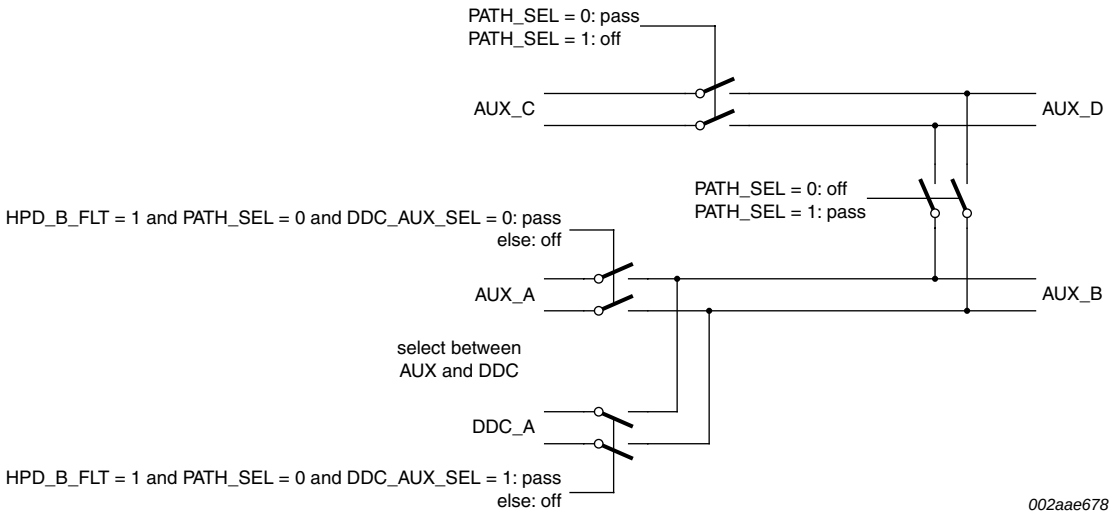


Fig 6. AUX and DDC channel topology

Port A additionally provides a second pair of signal lines, to allow bypassing of external AC-coupling capacitors (normally placed in series with the AUX channel) in the case when an external ++DP cable adapter is detected, and therefore a DC path needs to be provided from the external DP connector's AUX_P and AUX_N lines, in order to support DDC communication across those lines between the External Graphics GPU (facing Port A) and the external ++DP cable adapter. Selection between the DDC and AUX channels of Port A is determined by the input DDC_AUX_SEL: when DDC_AUX_SEL = LOW, the active channel is AUX_A; when DDC_AUX_SEL = HIGH, the active channel is DDC_A. Typically, DDC_AUX_SEL is driven by a qualified version of the DP 'Cable Detect' signal (pin 4 of a miniDP connector or pin 13 of a normal DP connector) and will be HIGH when such a cable adaptor is connected and powered.

Table 5. AUX/DDC channel configuration

Legend: high-Z = isolating, high-impedance; ACT = active, low-impedance.

Inputs			Channel				Comment (all other ports shall be mutually isolated)
PATH_SEL	HPD_B_FLT	DDC_AUX_SEL	Port C - Port D	Port A - Port B		Port B - Port D	
				AUX_A	DDC_A		
0	0	X	ACT	high-Z	high-Z	high-Z	Normal mode; internal display only
0	1	0	ACT	ACT	high-Z	high-Z	Normal mode with dual display
0	1	1	ACT	high-Z	ACT	high-Z	Normal mode with dual display using ++DP display adaptor
1	0	X	high-Z	high-Z	high-Z	ACT	External source mode with internal display not yet asserting HPD
1	1	X	high-Z	high-Z	high-Z	ACT	External source mode with internal display asserting HPD

7.4 HPD signal path

The HPD signal path, unlike the Main Link and AUX/DDC paths, uses active LVTTL logic rather than passive switching. As shown in Figure 7, the topology follows that of the Main Link and AUX channels but with the signal direction in reverse direction (since the HPD signal direction is always from sink to source). When PATH_SEL is LOW, output HPD_C follows and re-drives input HPD_D and similarly HPD_A follows the logic state of input HPD_B. An integrated 200 kΩ resistor (RPD_HPD) between HPD_B and GND ensures a logic LOW when no device is connected to Port B. When PATH_SEL is HIGH, HPD_B becomes an output and follows the logic state of HPD_D. Please also refer to Section 7.6 for specific details on the HPD filtering function.

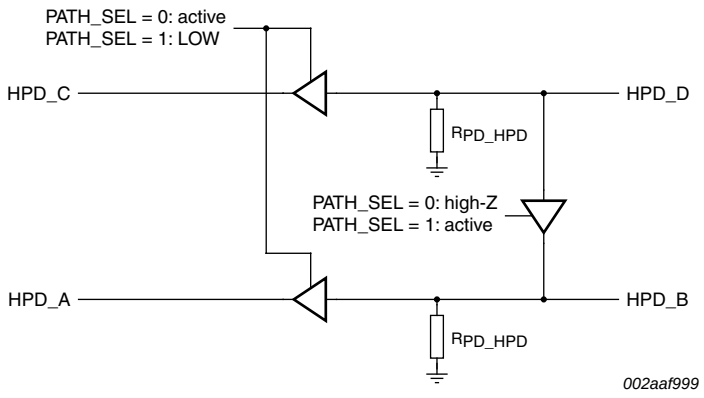


Fig 7. HPD channel topology

Table 6. HPD channel configuration

Inputs			Outputs				Comment
PATH_SEL	HPD_B	HPD_D	HPD_A	HPD_B	HPD_B_FLT[1]	HPD_C	
0	0	0	0	high-Z	0	0	Normal mode; internal display not (yet) asserting HPD
0	0	1	0	high-Z	0	1	Normal mode; internal display asserting HPD
0	1	0	1	high-Z	1	0	Normal mode but unexpected condition; internal display not asserting HPD during normal operation
0	1	1	1	high-Z	1	1	Normal mode; with external sink asserting HPD
1	n/a	0	0	0	0	0	External source mode with internal display not (yet) asserting HPD
1	n/a	1	0	1	1	0	External source mode with internal display asserting HPD

[1] Steady-state is shown only. A HIGH-to-LOW transition will be filtered (~4 ms delay).

7.5 AUX logic state detection

CBTL12131 includes a helpful function to determine the DC state of the AUX_B_P and AUX_B_N pins thereby aiding in the detection of devices connected to the external DP connector. The DC state of these pins is output on pins AUX_B_P_STATE and AUX_B_N_STATE respectively, after the 1 Mbit/s (typ) Manchester-encoded bitstream is removed by filtering.

7.6 HPD logic state detection

To further aid in detection of externally connected devices on Port B, the HPD_B_FLT pin outputs a filtered version of pin HPD_B. The filtering function suppresses the 1 ms (typ) LOW interrupt pulse from a DisplayPort sink, thereby avoiding a false disconnect detection. Only a LOW pulse greater than 4 ms will result in a LOW output on HPD_B_FLT.

7.7 Equalizer

The Equalizer function equalizes the signal on the Main Link channel of Port B and re-drives them to Port D and ultimately to the internal display panel.

The Equalizer is only active when PATH_SEL is HIGH. When PATH_SEL is LOW, the equalizer is effectively disabled and presents minimum parasitic load to the Main Link channels.

The Equalizer has configurable Equalization (EQ) settings for its input (Port B side), which can be set to one of five options by quinary input pin EQ5. See Table 7 for programming options.

Table 7. Equalizer settings

Inputs	Quinary notation	Equalizer mode (see Figure 8)
EQ5		
short to GND	0_5	0 dB
10 kΩ resistor to GND	1_5	2 dB
open-circuit	2_5	3.5 dB
10 kΩ resistor to VDD	3_5	6.5 dB
short to VDD	4_5	9 dB

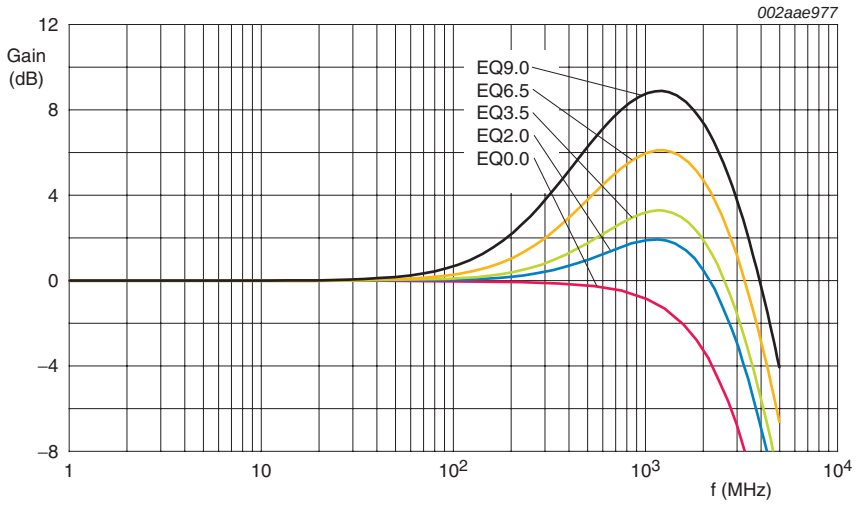


Fig 8. Equalizer gain versus frequency

The Equalizer also has two different levels of Pre-emphasis for its output (Port D side), which can be set by quinary input pin PL5; as well as two different output differential swing levels, which can be set by quinary input pin LV5. See Table 8 and Table 9 for programming options.

Table 8. Pre-emphasis settings

Inputs	Quinary notation	Output mode
PL5		
short to GND	0_5	0 dB
10 kΩ resistor to GND	1_5	3.5 dB[1]
open-circuit	2_5	reserved
10 kΩ resistor to VDD	3_5	reserved
short to VDD	4_5	reserved

[1] Only available with 400 mV output voltage swing setting (see Table 9).

Table 9. Output voltage swing settings

Inputs	Quinary notation	Output mode
LV5		
short to GND	0_5	400 mV
10 kΩ resistor to GND	1_5	600 mV[1]
open-circuit	2_5	reserved
10 kΩ resistor to VDD	3_5	reserved
short to VDD	4_5	reserved

[1] 600 mV level setting overrides pre-emphasis settings.

7.8 AUX channel bias and termination

The AUX lines of Port B can be biased and terminated in accordance with the DisplayPort Interoperability Guidelines in accordance with the configuration for either a sink or source, depending on which is required. The control input for the termination and bias are CMOS inputs AUX_TERM_SRC and AUX_TERM_SNK.

Together with the state of PATH_SEL and HPD_B_FLT (the filtered, steady state of HPD_B), these signals allow a detection scheme by which the system controller can resolve different connection scenarios of the external DisplayPort connector at Port B:

- Nothing is connected
- An external source is connected
- An external sink is connected (either with or without source detection being performed by the sink)
- An external, second all-in-one system (using a topology similar or equivalent to CBTL12131)

At first connection time, the latter scenario may appear identical to the first. In this case, AUX_TERM_SNK (which applies a 500 kΩ pull-up on AUX_B_P line provided) can be toggled HIGH in order to allow the other system to detect a connected sink, and configure itself accordingly as a source.

Using AUX_TERM_SRC, the system controller is able to check whether the attached device is a sink which is not asserting HPD (as some sinks will employ source detection for power saving reasons). By applying the integrated 100 kΩ pull-up and pull-down resistors, the attached sink will detect a source and assert its HDP when it is ready.

When HPD_B_FLT is HIGH, this means the attached device is asserting HPD and CBTL12131 will activate its source type 100 kΩ termination resistors.

When PATH_SEL is HIGH, this means the internal DisplayPort sink (embedded panel) is active, and its 1 MΩ termination resistors will apply the correct AUX bias to represent a sink device.

In the default condition (PATH_SEL, HPD_B_FLT and AUX_TERM_SNK/SRC are all LOW), 4.7 MΩ pull-down resistors are applied to the AUX_B pair, in order to avoid floating conditions in case two similar systems are connected together.

When both AUX_TERM_SRC and AUX_TERM_SNK are HIGH, all integrated termination resistors will be de-activated. For correct system operation, the system controller needs to guarantee that AUX_TERM_SRC and AUX_TERM_SNK are never HIGH at the same time, unless the external termination resistors are implemented.

Table 10. AUX channel bias and termination

Legend: high-Z = isolating, high-impedance; ACT = active, nominal-impedance.

Inputs				AUX terminations					Comments
PATH_SEL	HPD_B_FLT [1]	AUX_TERM_SRC	AUX_TERM_SNK	RAUX100P	RAUX100N	RAUX500P	RAUX4M7P	RAUX4M7N	
0	0	0	0	high-Z	high-Z	high-Z	ACT	ACT	Nothing connected.
0	0	0	1	high-Z	high-Z	ACT	high-Z	ACT	Override in scenario of two systems both using CBTL12131 connected together.[2]
0	0	1	0	ACT	ACT	high-Z	high-Z	high-Z	Allow sink to perform source detection.[3]
0	0	1	1	high-Z	high-Z	high-Z	high-Z	high-Z	[4][5]
0	1	0	0	ACT	ACT	high-Z	high-Z	high-Z	Dual display mode - normal condition.
0	1	0	1	ACT	ACT	high-Z	high-Z	high-Z	Not an expected condition. Already in dual display mode with source termination active.
0	1	1	0	ACT	ACT	high-Z	high-Z	high-Z	Not an expected condition. Already in dual display mode with source termination active.
0	1	1	1	high-Z	high-Z	high-Z	high-Z	high-Z	[4][5]
1	X	X	X	high-Z	high-Z	high-Z	high-Z	high-Z	Internal display expected to exhibit 1 MΩ pull-up and pull-down, hence no termination needed.

[1] HPD_B_FLT is an internally derived signal, not an input to CBTL12131. HPD_B_FLT will follow input HPD_B.

[2] System controller will assert AUX_TERM_SNK HIGH when user action prompts a ‘toggle’, hence system should configure itself as a sink.

[3] System controller will assert AUX_TERM_SRC HIGH when it has determined that a Sink is connected, hence system should configure itself as a source.

[4] System controller should guarantee that (AUX_TERM_SNK & AUX_TERM_SRC) is never TRUE for normal operation unless the external termination resistors are used.

[5] AUX_TERM_SRC **and** AUX_TERM_SNK = TRUE are used as a disable mechanism for the integrated AUX bias network when external termination resistors are used.

7.9 TST_REXT function

Pin TST_REXT has a dual function. In normal operation, this pin should be tied to analog GND externally via a 10 kΩ, 1 % accuracy resistor. The external resistor functions as a reference to establish accurate internal current sources for the EQ output stage. The second function of this pin is to put CBTL12131 in test mode by driving it HIGH. This test mode is for internal use only and has no use in normal operation.

8. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.3	+4.6	V
T_{case}	case temperature	for operation within specification		–40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	4000	V
		CDM	[2]	-	1000	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing. Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged-Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged-Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 12. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_I	input voltage		-	-	3.6	V
		HPD inputs	-	-	5.5	V
T_{amb}	ambient temperature	operating in free air	–40	-	+85	°C

10. Characteristics

10.1 General characteristics

Table 13. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	PATH_SEL = 0	-	30	40	mA
		PATH_SEL = 1	-	120	150	mA
$t_{startup}$	start-up time	supply voltage valid to channel specified operating characteristics	-	-	10	µs
t_{rcfg}	reconfiguration time	PATH_SEL state change to channel specified operating characteristics	-	-	10	µs

10.2 DisplayPort channel characteristics

Table 14. DisplayPort channel characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		–0.3	-	+2.6	V
V_{IC}	common-mode input voltage		0	-	2.0	V
V_{ID}	differential input voltage		-	-	+1.2	V
DDIL	differential insertion loss	channel is on; 0 Hz ≤ f ≤ 1.0 GHz	–2.0	–1.5	-	dB
		channel is on; f = 2.5 GHz	–3.5	-	-	dB
		channel is off; 0 Hz ≤ f ≤ 3.0 GHz	-	-	–30	dB
DDRL	differential return loss	channel is on; 0 Hz ≤ f ≤ 1.0 GHz	-	-	–10	dB
DDNEXT	differential near-end crosstalk	adjacent channels are on; 0 Hz ≤ f ≤ 1.0 GHz	-	-	–30	dB
B	bandwidth	–3.0 dB intercept	-	2.6	-	GHz
t_{PD}	propagation delay	from left-side port to right-side port or vice versa; PATH_SEL = 0	-	-	180	ps
		from Port B to Port D; PATH_SEL = 1	-	-	2	ms
$t_{sk(dif)}$	differential skew time	intra-pair	-	-	5	ps
t_{sk}	skew time	inter-pair	-	-	180	ps
$V_{TX\_DIFFp-p}$	differential peak-to-peak output voltage	Port D output; PATH_SEL = 1				
		LV5 short to GND	-	400	-	mV
		LV5 10 kΩ resistor to GND	-	600	-	mV
$V_{TX\_PREEMP\_RATIO}$	pre-emphasis ratio	Port D output; PATH_SEL = 1				
		PL5 short to GND	-	0	-	dB
		PL5 10 kΩ resistor to GND	-	3.5	-	dB

10.3 AUX and DDC ports

Table 15. AUX and DDC port characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_I	input voltage	DDC		–0.3	-	+3.6	V
		AUX; single-ended; Figure 9		0.16	-	0.7	V
α_{AUX}	AUX attenuation	with 100 Ω termination		-	2	3.5	dB
$V_{bias(DC)}$	bias voltage (DC)	AUX_P; Figure 9		0	-	2.0	V
		AUX_N; Figure 9		1.5	-	3.6	V
t_{PD}	propagation delay	between connected ports	[1]	-	180	-	ps

[1] Time from DDC/AUX input changing state to AUX output changing state. Includes DDC/AUX rise/fall time.

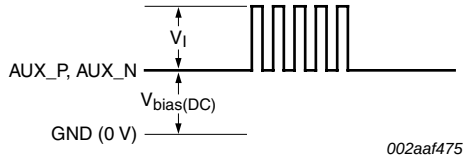


Fig 9. AUX_P and AUX_N input voltage waveform

10.4 HPD input, HPD output

Table 16. HPD input and output characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_I	input voltage		[1]	–0.3	-	3.6	V
t_{PD}	propagation delay	between connected ports	[2]	-	40	60	ns

[1] Low-speed input changes state on cable plug/unplug.

[2] Time from HPD_SINK changing state to HPD changing state. Includes HPD rise/fall time.

10.5 Control inputs

Table 17. Control input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	CMOS inputs	2.0	-	3.6	V
V_{IL}	LOW-level input voltage	CMOS inputs	0	-	0.8	V
I_{LI}	input leakage current	measured with input at $V_{IH(max)}$ and $V_{IL(min)}$	-	-	10	μA

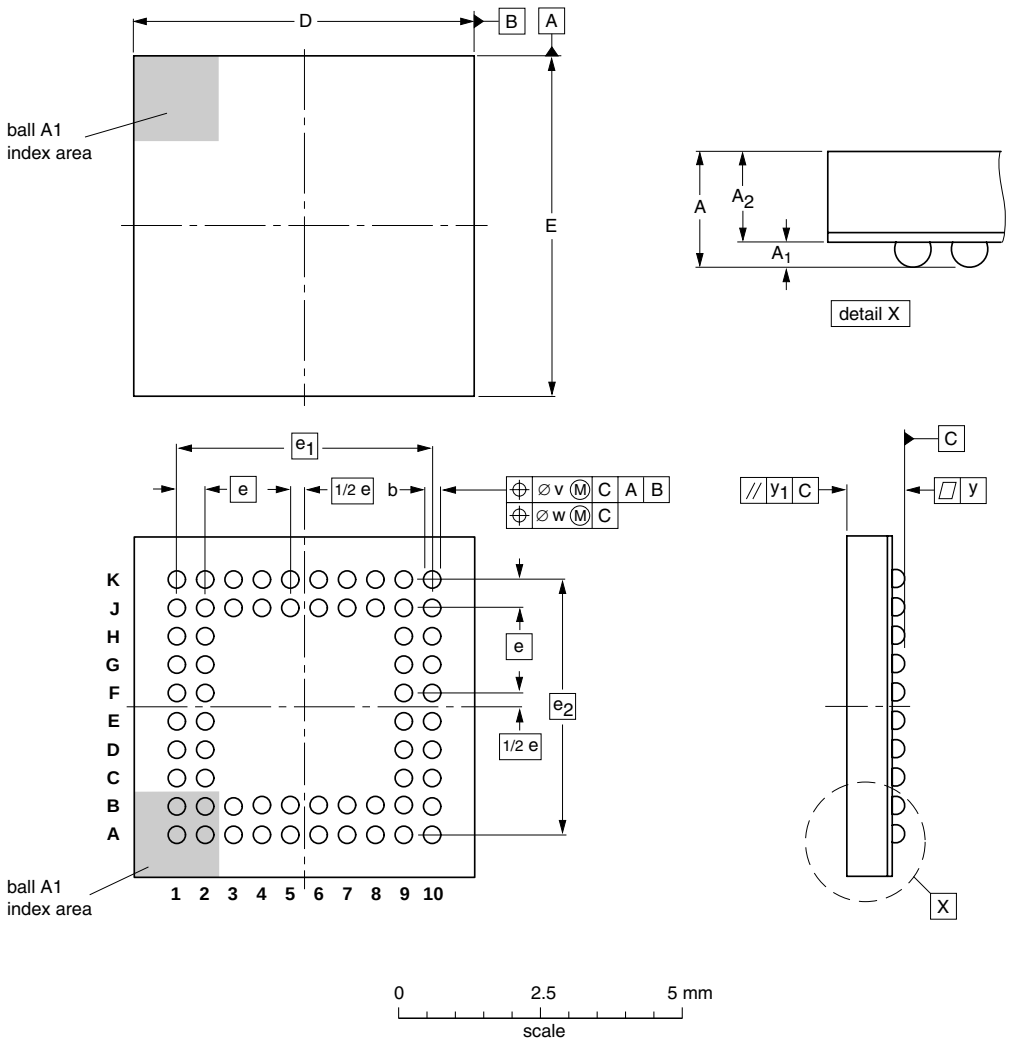
10.6 Status outputs

Table 18. Status output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	CMOS outputs	2.5	-	-	V
V_{OL}	LOW-level output voltage	CMOS outputs	0	-	0.2	V
t_t	transition time	10 % to 90 %	1	-	60	ns

11. Package outline

TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls; body 6 x 6 x 0.8 mm **SOT543-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.1	0.25 0.15	0.85 0.75	0.35 0.25	6.1 5.9	6.1 5.9	0.5	4.5	4.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT543-1	- - -	MO-195	- - -			~~00-11-22~~ 02-04-09

Fig 10. Package outline SOT543-1 (TFBGA64)

12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 19 and 20

Table 19. SnPb eutectic process (from J-STD-020C)

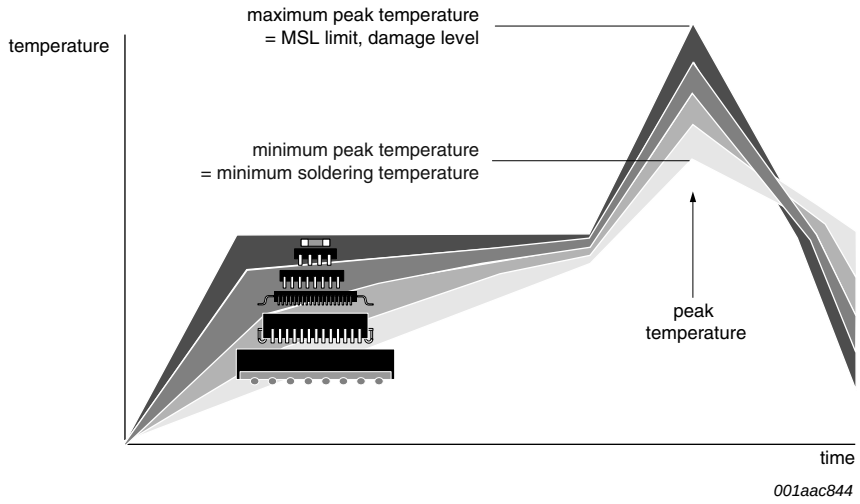
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 20. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 21. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DDC	Data Display Channel
DP	DisplayPort
eDP	embedded DisplayPort
ESD	ElectroStatic Discharge
GPU	Graphics Processor Unit
HBM	Human Body Model
HPD	Hot Plug Detect
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LVTTL	Low Voltage Transistor-Transistor Logic
ML	Main Link

14. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL12131 v.1	20110225	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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