

ADG701/ADG702

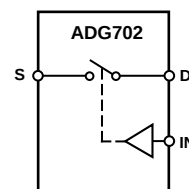
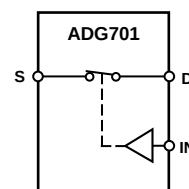
FEATURES

+1.8 V to +5.5 V Single Supply
2 Ω (Typ) On Resistance
Low On-Resistance Flatness
-3 dB Bandwidth >200 MHz
Rail-to-Rail Operation
6-Lead SOT-23
8-Lead μ SOIC Package
Fast Switching Times
 t_{ON} 18 ns
 t_{OFF} 12 ns
Typical Power Consumption (<0.01 μ W)
TTL/CMOS Compatible

APPLICATIONS

Battery Powered Systems
Communication Systems
Sample Hold Systems
Audio Signal Routing
Video Switching
Mechanical Reed Relay Replacement

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR
A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG701/ADG702 are monolithic CMOS SPST switches. These switches are designed on an advanced submicron process that provides low power dissipation yet high switching speed, low on resistance, low leakage currents and -3 dB bandwidths of greater than 200 MHz can be achieved.

The ADG701/ADG702 can operate from a single +1.8 V to +5.5 V supply making it ideal for use in battery powered instruments and with the new generation of DACs and ADCs from Analog Devices.

As can be seen from the Functional Block Diagrams, with a logic input of "1" the switch of the ADG701 is closed, while that of the ADG702 is open. Each switch conducts equally well in both directions when ON.

The ADG701/ADG702 are available in 6-lead SOT-23 and 8-lead μ SOIC packages.

PRODUCT HIGHLIGHTS

1. +1.8 V to +5.5 V Single Supply Operation. The ADG701/ADG702 offer high performance, including low on resistance and fast switching times and is fully specified and guaranteed with +3 V and +5 V supply rails.
2. Very Low R_{ON} (3 Ω max at 5 V, 5 Ω max at 3 V). At 1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.
3. On-Resistance Flatness $R_{FLAT(ON)}$ (1 Ω max).
4. -3 dB Bandwidth >200 MHz.
5. Low Power Dissipation. CMOS construction ensures low power dissipation.
6. Fast t_{ON}/t_{OFF} .
7. Tiny 6-Lead SOT-23 and 8-Lead μ SOIC.

REV. A

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ADG701/ADG702—SPECIFICATIONS¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^{\circ}\text{C}$ unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	V _S = 0 V to V _{DD} , I _S = −10 mA; Test Circuit 1 V _S = 0 V to V _{DD} , I _S = −10 mA
On Resistance (R _{ON})	2		Ω typ	
	3	4	Ω max	
On-Resistance Flatness (R _{FLAT(ON)})	0.5		Ω typ	
		1.0	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = +5.5 V V _S = 4.5 V/1 V, V _D = 1 V/4.5 V; Test Circuit 2 V _S = 4.5 V/1 V, V _D = 1 V/4.5 V; Test Circuit 2 V _S = V _D = 1 V, or 4.5 V; Test Circuit 3
	±0.25	±0.35	nA max	
Drain OFF Leakage I _D (OFF)	±0.01		nA typ	
	±0.25	±0.35	nA max	
Channel ON Leakage I _D , I _S (ON)	±0.01		nA typ	
	±0.25	±0.35	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}		0.8	V max	
Input Current				
I _{INL} or I _{INH}	0.005		μA typ	
		±0.1	μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	12		ns typ	R _L = 300 Ω, C _L = 35 pF V _S = 3 V; Test Circuit 4 R _L = 300 Ω, C _L = 35 pF V _S = 3 V; Test Circuit 4 V _S = 2 V, R _S = 0 Ω, C _L = 1 nF; Test Circuit 5 R _L = 50 Ω, C _L = 5 pF, f = 10 MHz; R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 6 R _L = 50 Ω, C _L = 5 pF; Test Circuit 7
		18	ns max	
t _{OFF}	8		ns typ	
		12	ns max	
Charge Injection	5		pC typ	
Off Isolation	−55		dB typ	
	−75		dB typ	
Bandwidth −3 dB	200		MHz typ	
C _S (OFF)	17		pF typ	
C _D (OFF)	17		pF typ	
C _D , C _S (ON)	38		pF typ	
POWER REQUIREMENTS				
I _{DD}	0.001		μA typ	V _{DD} = +5.5 V Digital Inputs = 0 V or 5 V
		1.0	μA max	

NOTES

¹Temperature ranges are as follows: B Versions: -40°C to $+85^{\circ}\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹ ($V_{DD} = 3\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^{\circ}\text{C}$ unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	V _S = 0 V to V _{DD} , I _S = −10 mA; Test Circuit 1 V _S = 0 V to V _{DD} , I _S = −10 mA
On Resistance (R _{ON})	3.5		Ω typ	
	5	6	Ω max	
On-Resistance Flatness (R _{FLAT(ON)})	1.5		Ω typ	
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = +3.3 V V _S = 3 V/1 V, V _D = 1 V/3 V; Test Circuit 2 V _S = 3 V/1 V, V _D = 1 V/3 V; Test Circuit 2 V _S = V _D = 1 V, or 3 V; Test Circuit 3
	±0.25	±0.35	nA max	
Drain OFF Leakage I _D (OFF)	±0.01		nA typ	
	±0.25	±0.35	nA max	
Channel ON Leakage I _D , I _S (ON)	±0.01		nA typ	
	±0.25	±0.35	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}		0.4	V max	
Input Current				
I _{INL} or I _{INH}	0.005	±0.1	μA typ μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	14	20	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 2 V, Test Circuit 4 R _L = 300 Ω, C _L = 35 pF V _S = 2 V, Test Circuit 4 V _S = 1.5 V, R _S = 0 Ω, C _L = 1 nF; Test Circuit 5 R _L = 50 Ω, C _L = 5 pF, f = 10 MHz R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 6 R _L = 50 Ω, C _L = 5 pF; Test Circuit 7
t _{OFF}	8	13	ns typ ns max	
Charge Injection	4		pC typ	
Off Isolation	−55 −75		dB typ dB typ	
Bandwidth −3 dB	200		MHz typ	
C _S (OFF)	17		pF typ	
C _D (OFF)	17		pF typ	
C _D , C _S (ON)	38		pF typ	
POWER REQUIREMENTS				
I _{DD}	0.001	1.0	μA typ μA max	V _{DD} = +3.3 V Digital Inputs = 0 V or 3 V

NOTES

¹Temperature ranges are as follows: B Versions: -40°C to $+85^{\circ}\text{C}$.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG701/ADG702

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs ²	−0.3 V to V _{DD} +0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
μSOIC Package, Power Dissipation	315 mW
θ _{JA} Thermal Impedance	206°C/W
θ _{JC} Thermal Impedance	44°C/W
SOT-23 Package, Power Dissipation	282 mW
θ _{JA} Thermal Impedance	229.6°C/W
θ _{JC} Thermal Impedance	91.99°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
ESD	2 kV

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table

ADG701 In	ADG702 In	Switch Condition
0	1	OFF
1	0	ON

ORDERING GUIDE

Model	Temperature Range	Brand*	Package Descriptions	Package Options
ADG701BRT	−40°C to +85°C	S3B	SOT-23 (Plastic Surface Mount)	RT-6
ADG702BRT	−40°C to +85°C	S4B	SOT-23 (Plastic Surface Mount)	RT-6
ADG701BRM	−40°C to +85°C	S3B	μSOIC (Small Outline)	RM-8
ADG702BRM	−40°C to +85°C	S4B	μSOIC (Small Outline)	RM-8

*Brand = Due to package size limitations, these three characters represent the part number.

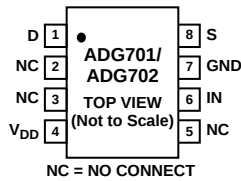
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG701/ADG702 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

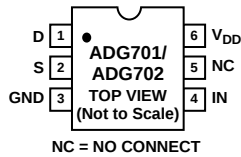


PIN CONFIGURATIONS

8-Lead μ SOIC (RM-8)



6-Lead Plastic Surface Mount (SOT-23) (RT-6)



TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic Resistance Between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF."
I_D (OFF)	Drain Leakage Current with the Switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON."
$V_D (V_S)$	Analog Voltage on Terminals D, S.
C_S (OFF)	"OFF" Switch Source Capacitance.
C_D (OFF)	"OFF" Switch Drain Capacitance.
C_D, C_S (ON)	"ON" Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
Off Isolation	A measure of Unwanted Signal Coupling Through an "OFF" Switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by -3 dBs.
On Response	The frequency response of the "ON" switch.
On Loss	The voltage drop across the "ON" switch seen on the On Response vs. Frequency plot as how many dBs the signal is away from 0 dB at very low frequencies.

ADG701/ADG702—Typical Performance Characteristics

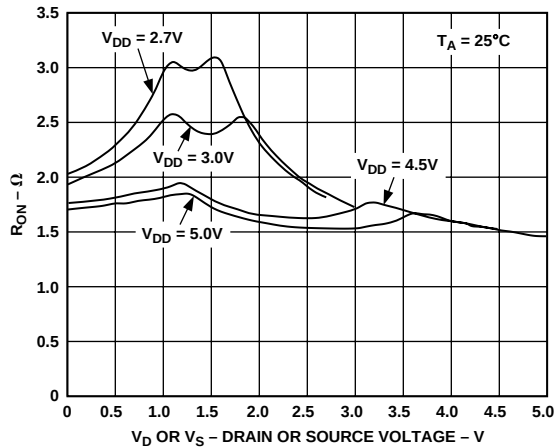


Figure 1. On Resistance as a Function of V_D (V_S) Single Supplies

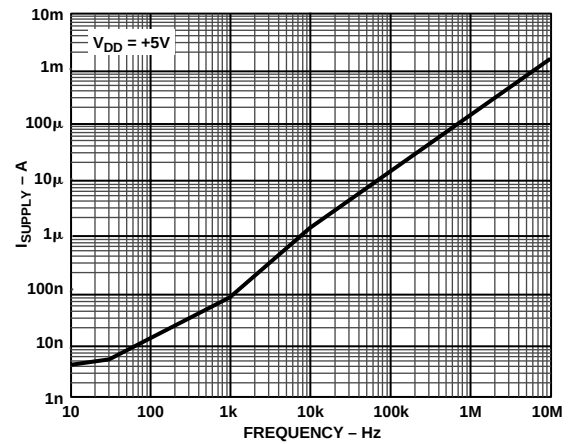


Figure 4. Supply Current vs. Input Switching Frequency

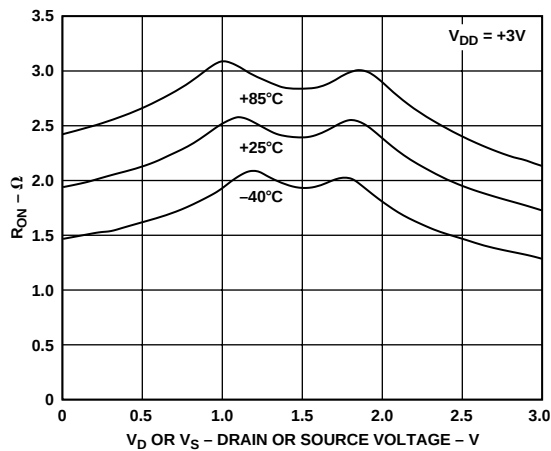


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 3\text{ V}$

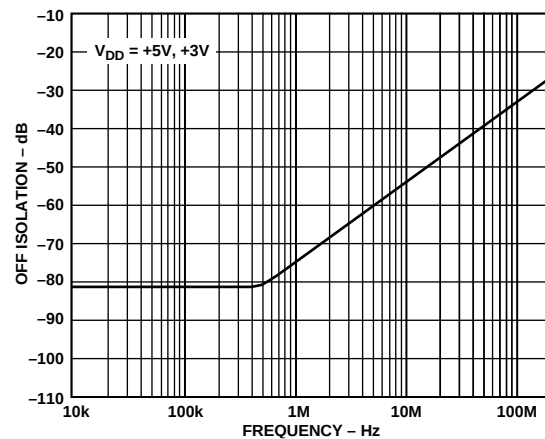


Figure 5. Off Isolation vs. Frequency

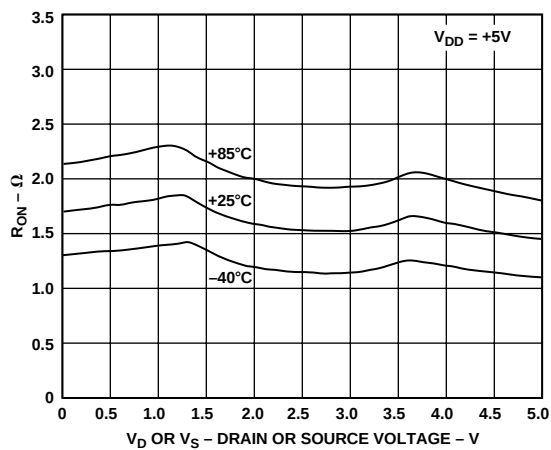


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 5\text{ V}$

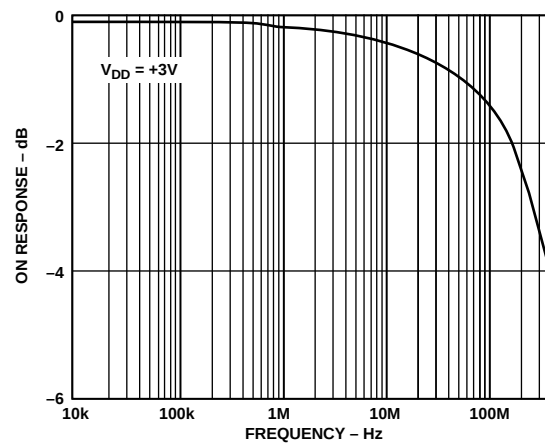
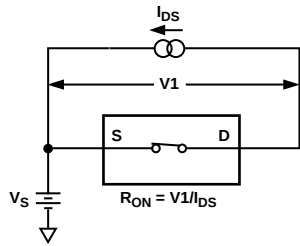
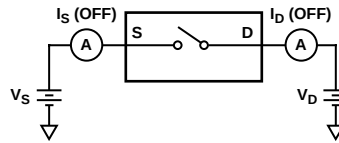


Figure 6. On Response vs. Frequency

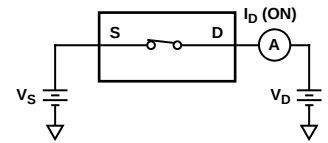
Test Circuits



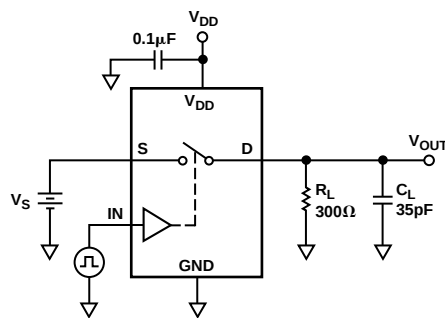
Test Circuit 1. On Resistance



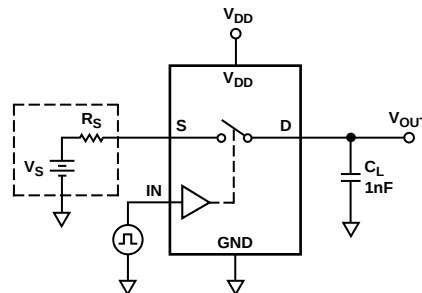
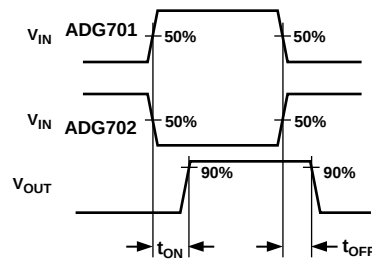
Test Circuit 2. Off Leakage



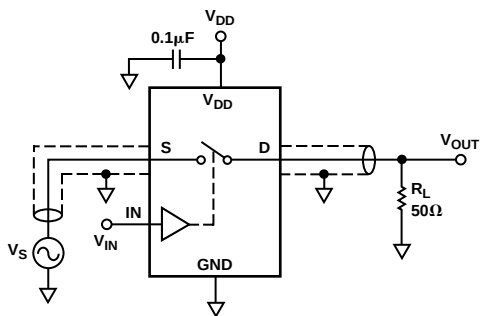
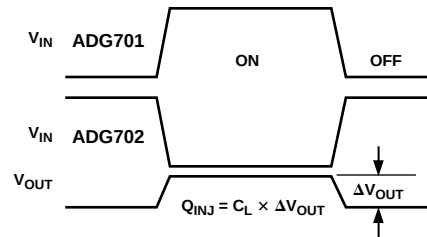
Test Circuit 3. On Leakage



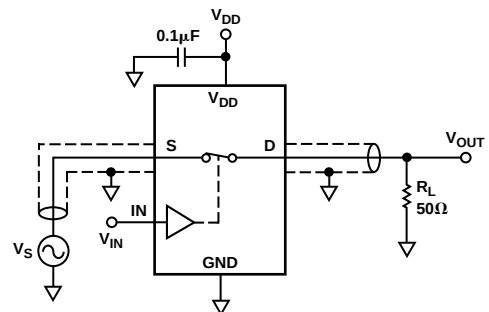
Test Circuit 4. Switching Times



Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation



Test Circuit 7. Bandwidth

