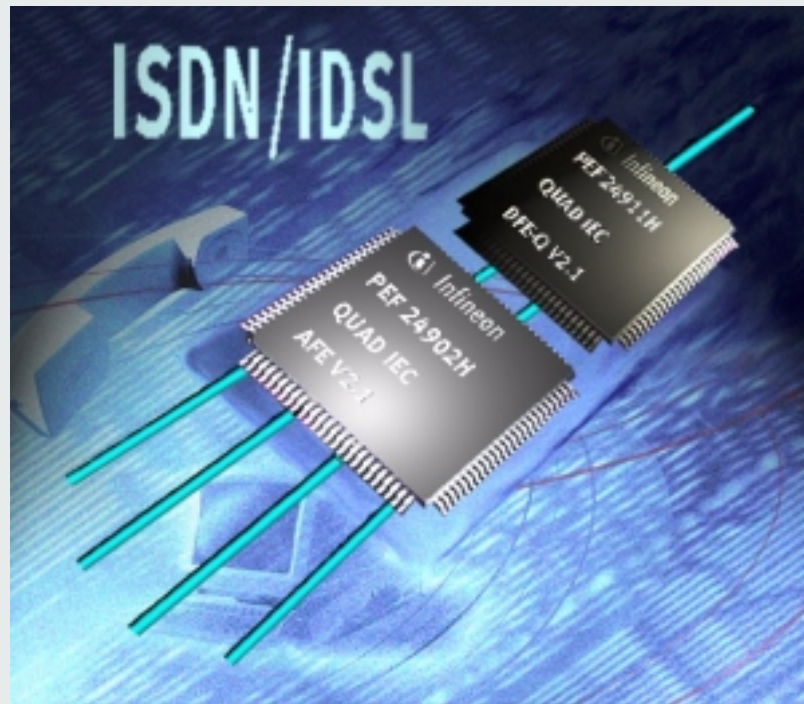


IEC4-Q

PEF 24911 V2.1 (DFE-Q) &
PEF 24902 V2.1 (AFE)

ISDN Echocancellation Circuit
4-Channel for 2B1Q Line Code

The widely used ISDN 4-channel chipset IEC4-Q consisting of the analog frontend PEB/F 24902 (AFE) and the digital frontend PEB/F 24911 (DFE-Q) has been optimized by a redesign of the digital part. The improvements of the DFE-Q are a reduced supply-voltage due to its advanced low power 3.3V-CMOS-technology, the doubling of the IOM[®]-2 data-rate up to 4Mbit/s and new features in terms of testability and analysis. The IEC4-Q chipset fulfills all relevant ANSI, ETSI and ITU standards. Because of its multichannel-architecture it is extremely suitable for highly integrated ISDN- and IDSL-linecards.



ISDN/IDSL

Applications

- Central office digital linecard
- Access network linecards
- PBX Linecards

Features

- Two chip solution featuring full duplex data transmission and reception over two-wire metallic subscriber loops providing 4x ISDN basic rate access or 4x IDSL access at 144kbit/s
- Fully compliant to:
 - ANSI T1.601 (1998)
 - ETSI TS 102 080 (1998)
 - Recommendation ITU-T G.961
- Meets requirements for all ANSI and ETSI loops
- 2B1Q block code at 80 kHz symbol rate
- LT mode
- Low power consumption
- IOM[®]-2 interface for stand alone mode
- Activation and deactivation
- Masterclock generated by PLL
- Automatic polarity adaption
- Automatic gain control
- Adaptive echocancellation
- Adaptive equalization
- 4 relay driver pins per channel to switch relays or power controller
- 2 status pins per channel
- Extended temperature range (-40°C to +85°C)
- JTAG boundary scan
- P-MQFP-64 package
- Part of the Infineon system solution

Add-On Features of the DFE-Q PEF 24911 V2.1 compared to V1.x

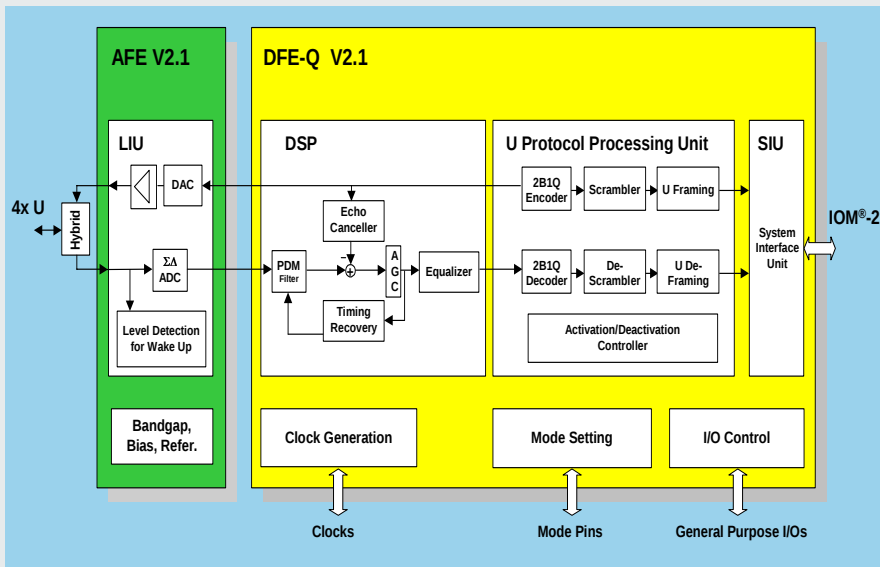
- Max. IOM[®]-2 data rate 4 Mbit/s (DCL=8MHz)
- +3.3 V instead of +5V power supply
- Dedicated pins for SSP and DT test modes
- DOUT configurable either as open drain or push-pull (tristate) output
- Monitor Time-Out (MTO)
- New MON-12 class features internal register access
- Additional digital local loops
- Bit Error Rate Measurement per port
- Optimized LT-state machine
- Backward compatibility to V1.x:
 - no software changes required
 - pinning-compatible

ISDN/IDSL 4-Channel Chipset



Never stop thinking.

Block Diagram



Ordering Code

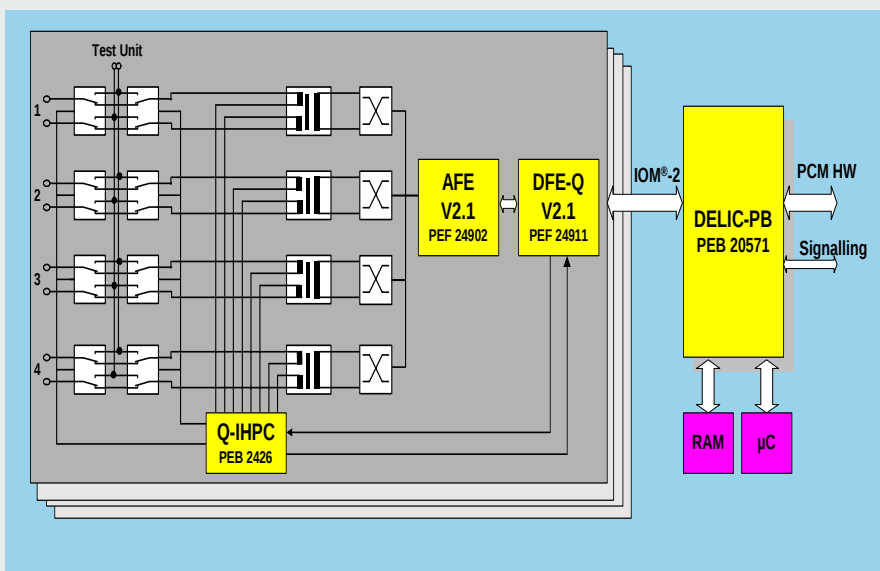
Type	Package	Sales Code	Availability
PEF 24911 H V2.1	P-MQFP-64	Q67233-H1233	Development
PEF 24902 H V2.1	P-MQFP-64	Q67101-H6850	Available

Tools and Documentation

Name	Sales Code	Status
Data Sheet PEB/F 24902 V2.1		03.00
Data Sheet PEF 24911 V2.1		08.00
Smart 24911 V2.0 Demoboard	Q67230-H1234	Development

Application Example

ISDN/IDSL Linecard



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