TEXAS INSTRUMENTS

TVP5010

NTSC/PAL Video Decoder

Data Manual

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Mixed-Signal Products

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1 Introduction

The TVP5010, is a high quality single chip digital video decoder that converts base-band analog NTSC and PAL video signals into digital components video. Both composite and S-video are supported and 8-, 12-, and 16-bit outputs are selectable. Sampling is square-pixel or ITU-R BT.601 (13.5 MHz) and is line locked for correct pixel alignment. The output formats can be 8-bit or 16-bit 4:2:2, 12-bit 4:1:1, or 8-bit ITU-R BT.656. The TVP5010 uses TI patented technology for locking to weak, noisy, or unstable signals, and a genlock control output is generated for synchronizing downstream video encoders.

Two-line (1-H delay) comb filtering is available for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts; a chroma trap filter is also available. Video characteristics including hue, contrast, and saturation are programmable using one of five supported host port interfaces. The TVP5010 generates synchronization, blanking, field, lock, and clock signals in addition to digital video outputs.

The main blocks of TVP5010 include:

- Analog processors and A/D converters
- Y/C separation
- Chrominance processor
- Luminance processor
- Clock/Timing processor and power-down control
- Output formatter
- Host port interface

1.1 Features

- Accepts NTSC (M) and PAL (B, D, G, H, I, M, N) composite video, S-video
- Four analog video inputs for up to 4 composite inputs or 2 S-video inputs
- Two built-in-analog signal processing channels with clamping and AGC
- Dual high speed 8-bit A/D converters for luminance and chrominance processing
- Patented architecture for locking to weak, noisy, or unstable signals
- Comb filters for both cross-color and cross-luminance noise reductions
- Line locked clock and sampling
- I^2C host port
- Programmable data rates:
  - 12.2727 MHz square-pixel (NTSC)
  - 14.7500 MHz square-pixel (PAL)
  - 13.5 MHz ITU-R BT.601 (NTSC and PAL)
- Programmable output formats: 16-bit or 8-bit 4:2:2 YCbCr, 12-Bit 4:1:1 YCbCr and ITU-R BT.656 with embedded syncs
- ITU-R BT.601 or extended coding range
- Brightness, contrast, saturation , and hue control through host port
- 80-terminal TQFP package

1.2 Applications

- Digital image processing
- Video conferencing
- Multimedia
- Digital video
- Desktop video
- Video capture
- Video editing

1.3 Functional Block Diagram

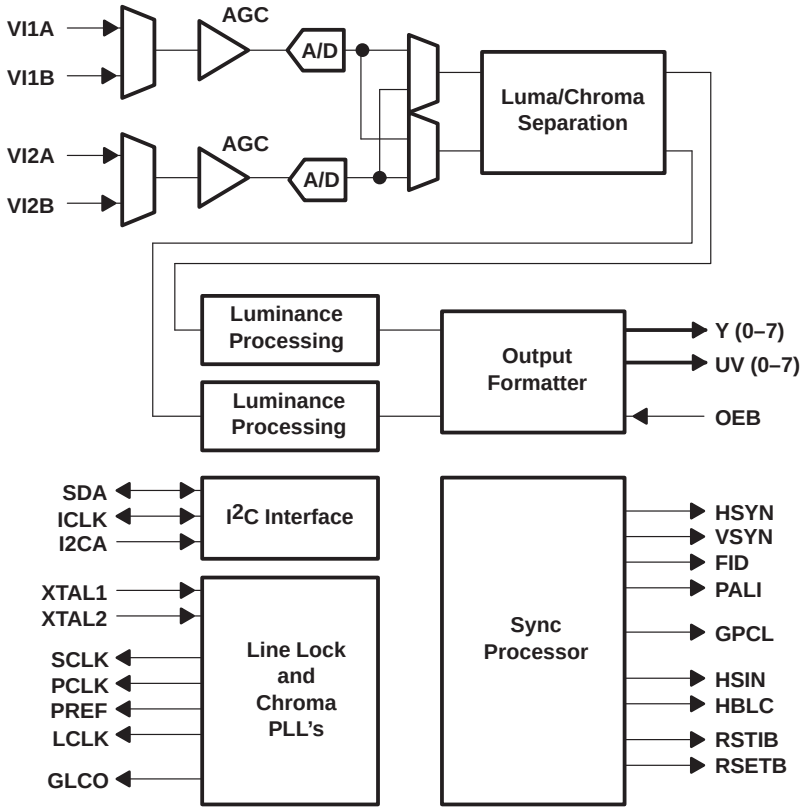


Figure 1–1. Functional Block Diagram

1.4 Terminal Assignments

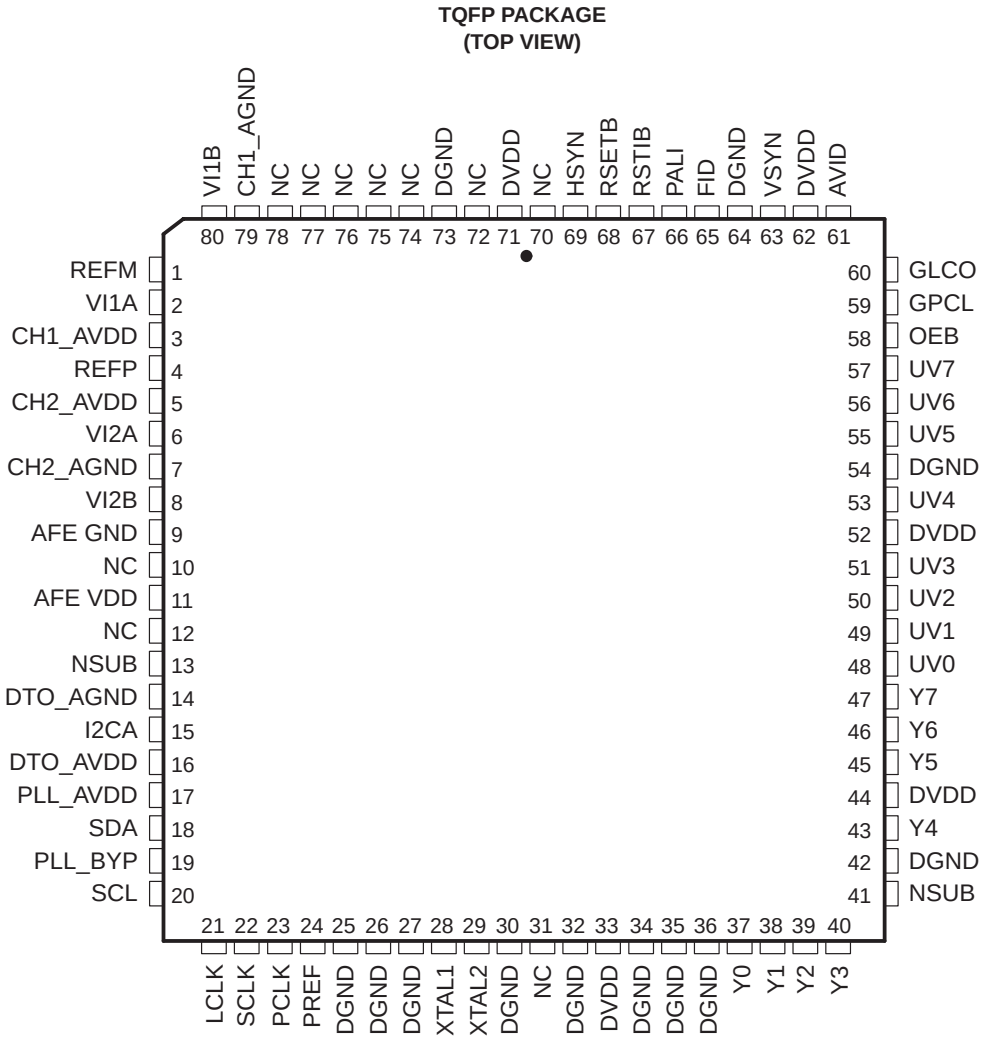


Figure 1–2. TVP5010 Pin Assignments

1.5 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Analog Video			
VI1A VI1B VI2A VI2B	2 80 6 8	I	Analog Video inputs. Up to four composite inputs or two S-video inputs or a combination of the two. The inputs must be ac coupled. The recommended coupling capacitor is 0.1 μF.
Digital Video			
Y[0:7]	37, 38, 39, 40, 43, 45, 46, 47	O	8-bit digital luminance outputs, or 8-bit multiplexed luminance and chrominance outputs. These pins may also be configured to output data from the channel 1 A/D converter.
UV[0:7]	48, 49, 50, 51, 53, 55, 56, 57	I/O	8-bit digital chrominance outputs. These pins may also be configured to output data from the channel 2 A/D converter.
Clock Signals			
LCLK	21	O	Clock output with one-half the frequency of the pixel clock (PCLK)
SCLK	22	O	System clock output with twice the frequency of the pixel clock (PCLK).
PCLK	23	O	Pixel clock output. The frequency is 12.2727 MHz for square-pixel NTSC, 14.75 MHz for square-pixel PAL, and 13.5 MHz for ITU-R BT.601 sampling modes.
XTAL1 XTAL2	28 29	I	External clock reference. XTAL1 may be connected to a TTL-compatible oscillator or to one terminal of a crystal oscillator. XTAL2 may be connected to the second terminal of a crystal oscillator or left unconnected. The oscillator frequencies used are 26.800 MHz for square pixel sampling or 24.576 MHz for ITU-R BT.601 sampling.
PREF	24	O	Clock phase reference signal. This signal may be used to qualify clock edges when SCLK is used to clock data which is changing at the pixel clock rate.
Sync Signals			
HSYN	69	O	Horizontal sync signal. The rising edge time is programmable.
VSYN	63	O	Vertical sync or vertical blanking signal. The function of this pin is selected via I^2C control.
FID	65	O	Odd/even field indicator or vertical lock indicator. For odd/even indicator, a logic 1 indicates the odd field. For vertical lock indicator, a logic 1 indicates the internal vertical processor is in locked state. The function of this pin is selected via I^2C control.
PALI	66	O	PAL line indicator or horizontal lock indicator. For PAL line indicator, a logic 1 indicates a noninverted line, and a logic 0 indicates an inverted line. For horizontal lock indicator, a logic 1 indicates the internal horizontal PLL is in a locked state. The function of this pin is selected via I^2C control.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Sync Signals (continued)			
AVID	61	O	Active video indicator. This signal is high during the horizontal active time of the video output on the Y and UV pins. AVID continues to toggle during vertical blanking intervals.
I^2C-Bus			
SDA	18	I/O	I^2C-bus serial data
SCL	20	I/O	I^2C-bus serial clock
I2CA	15	I/O	I^2C slave address select
Miscellaneous Signals			
RSTIB	67	I	Reset input, active low. A low input initiates the reset sequence described in Section 2.10.
RSETB	68	O	Reset output, active low. This signal is low during the reset sequence described in Section 2.10.
OEB	58	I	Output enable, active low; or data input for 9- or 10-bit external A/D. The function of this pin is selected via I^2C control. When this pin is an output enable a logic 1 input forces Y and UV output pins to high impedance states.
GLCO	60	O	Genlock control output. This pin serially outputs color subcarrier PLL information. The information can be decoded by a slave device to allow genlocking to the TVP5010. Data is transmitted at the SCLK rate.
GPCL	59	I/O	General purpose control logic. This pin has four functions: 1. General purpose output. In this mode the state of GPCL is directly programmed via I^2C. 2. Vertical blank output. In this mode the GPCL pin is used to indicate the vertical blanking interval of the output video. 3. LSB of input data from 10-bit external A/D. 4. Sync lock control input. In this mode when GPCL is high the output clocks and horizontal line count are forced to nominal values. The function of this pin is selected via I^2C control.
No Connect	10, 12, 31, 70, 72, 74, 75, 76, 77, 78	O	Factory test only, do not connect.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Power Supplies			
REFP	4		A/D reference supply. Connect to 5 V analog.
REFM	1		A/D reference ground. Connect to analog ground.
CH1_AVDD CH2_AVDD	3 5		Analog front end supplies. Connect to 5 V analog.
CH1_AGND CH2_AGND	79 7		Analog front end grounds. Connect to analog ground.
DTO_AVDD	16		Supply for DTO portion of clock/sync circuit. Connect to 5 V analog.
DTO_AGND	14		Ground for DTO. Connect to analog ground.
PLL_AVDD	17		Supply for PLL portion of clock/sync circuit. Connect to 5 V analog.
PLL_BYP	19		Bypass to PLL_AVDD (pin 17) with a 0.1 μF capacitor.
AFE_DVDD	11		Digital supply for analog front end. Connect to 5 V digital.
AFE_DGND	9		Digital ground for analog front end.
NSUB	13, 41		Substrate ground. Connect to analog ground.
DGND	25, 26, 27, 30, 32, 34, 35, 36, 42, 54, 64, 73		Digital grounds
DVDD	33, 44, 52, 62, 71		Digital supplies, 5 V

2 Detailed Description

2.1 Analog Video Processors and A/D Converters

Figure 2–1 shows the detailed functional diagram of the analog video processors and A/D converters. This block provides the analog interface to all the video inputs. It accepts up to four inputs, performs analog signal conditioning (i.e., video clamping, video amplifying), and carries out analog-to-digital conversion.

2.1.1 Video Input Selection

Four high impedance video inputs are sources for two internal analog channels in the TVP5010. The internal multiplexers via the host port bus can select the desired input. The user can connect the four analog video inputs in the following combinations:

- Four selectable individual composite video inputs
- 1 S-video input and two composite video inputs
- 2 S-video inputs

2.1.2 Analog Input Clamping and Automatic Gain Control Circuits

The internal clamp circuit restores the ac coupled video signals to a fixed dc level before A/D conversion. The clamping circuits provides line-by-line restoration of the video sync level to a fixed dc reference voltage. The circuit has two modes of clamping, coarse and fine. In coarse, the most negative portion of the signal (typically the sync tip) is clamped to a fixed dc level. The circuit uses fine mode to prevent spurious level shifting caused by noise that is more negative than the sync tip on the input signal. When fine mode is enabled, after sync position is detected, clamping is only enabled during sync period. S-video requires fine clamping mode for proper operation.

Input video signals may vary significantly from the normal level of 1 Vpp. An automatic gain control (AGC) circuit adjusts the signal amplitude to use the maximum range of the A/D converters without clipping.

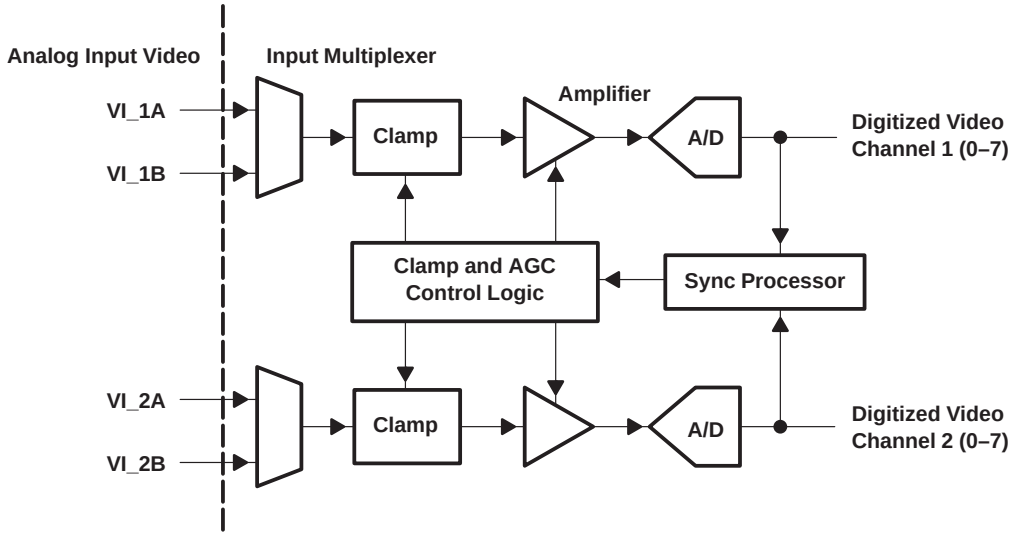


Figure 2–1. Analog Video Processors and A/D Converters

2.1.3 A/D Converters

The TVP5010 contains two 8-bit A/D converters which digitize the analog video signal inputs. To prevent high frequencies which are above half of the sampling rate from entering into the system, video input(s) may require an external antialiasing low pass filter.

2.2 Digital Processing

Figure 2–2 shows the block diagram of the digital video decoder processing. This block receives digitized composite or S-video signals from the A/D converters, and performs Y/C separation, chroma demodulation, and Y-signal enhancements. It also generates the horizontal and vertical syncs. The YUV digital output may be programmed into various formats: 16-bit or 8-bit 4:2:2, 12-bit 4:1:1 and ITU-R BT.656 parallel interface standard. The circuit uses comb filters to reduce the cross-chroma and cross-luma noise.

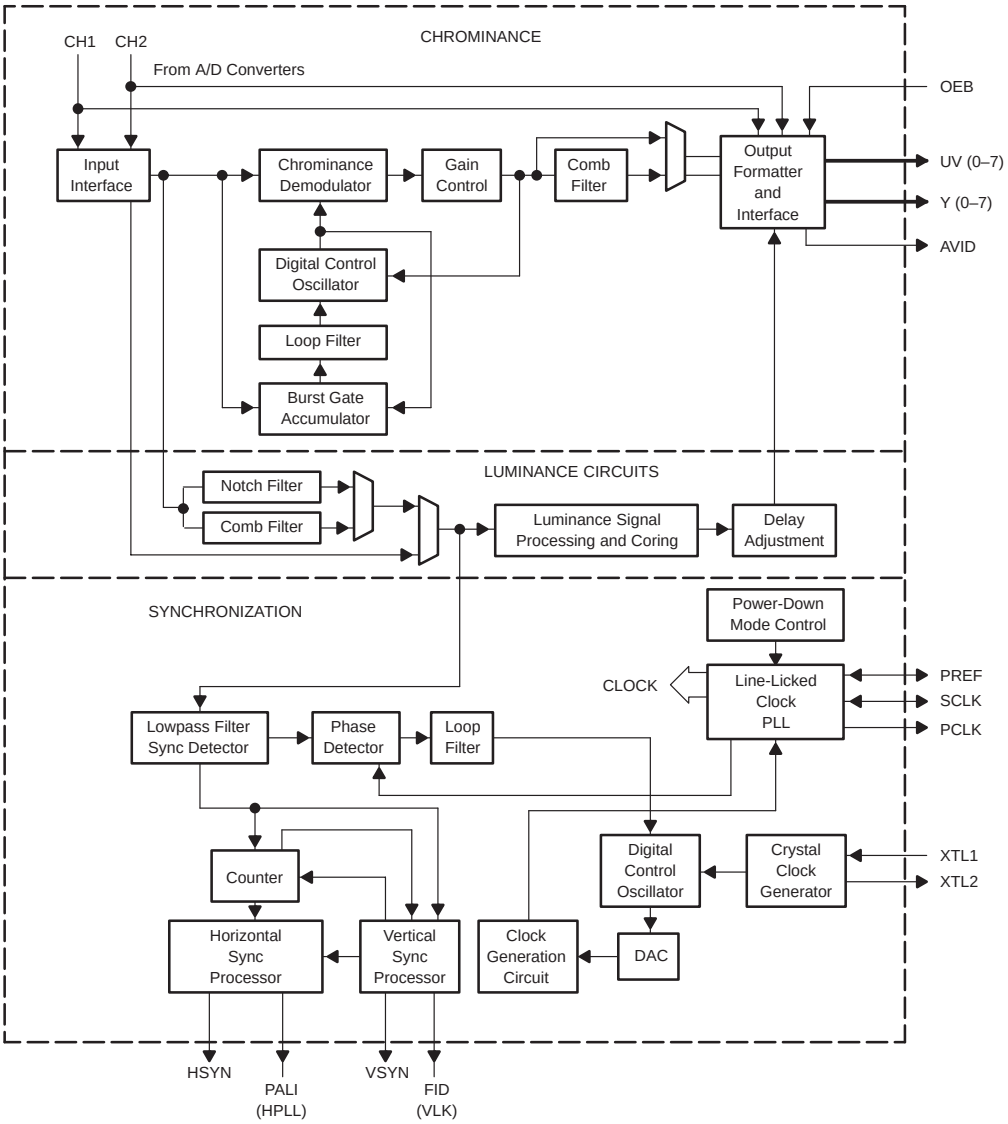


Figure 2–2. Digital Video Signal Processing Block Diagram

2.2.1 Y/C Separation

Luma/chroma separation may be done using either 2-line (1–H delay) comb filtering or a chroma trap filter. Comb filtering is available for both the luminance and the chrominance portion of the data path. The characteristics of the filter are shown in Figure 2–3 and 2–4.

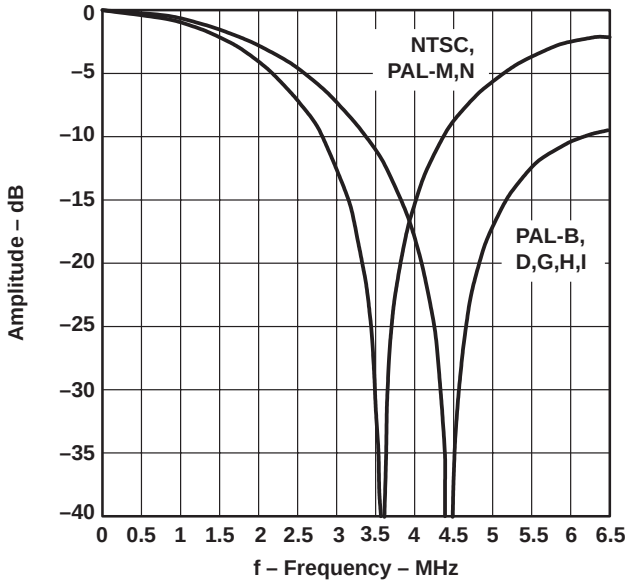


Figure 2–3. Chroma Trap Filter Frequency Response for 13.5 MHz Sampling

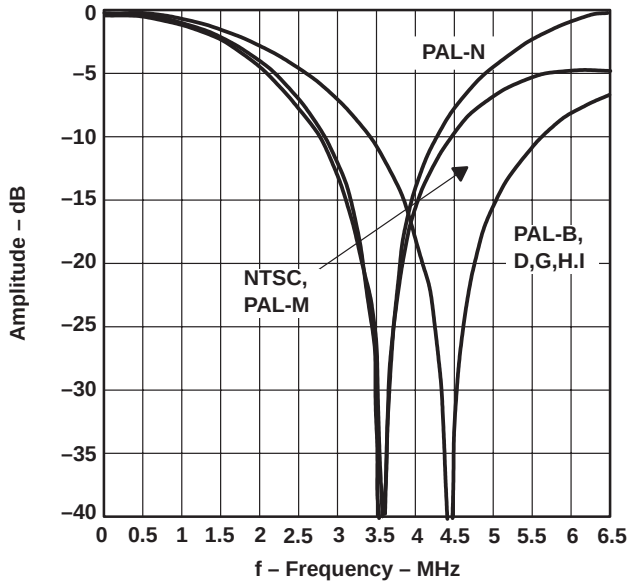


Figure 2–4. Chroma Trap Filter Frequency Response for Square-Pixel Sampling

2.2.2 Luminance Processing

The digitized composite video signal from the output of A/D converters passes through a luminance comb filter or a chroma trap filter that removes the chrominance signal from the composite signal to generate luminance signal. The luminance signal is then fed to the input of luminance signal peaking and coring circuits. Figure 2–5 illustrates the basic functions of the luminance data path. In the case of S-video, the luminance signal will bypass the comb filter or notch filter and be fed to the peaking and coring circuits directly. High frequency components of the luminance signal are enhanced further by the peaking filter (edge

enhancer). Figures 2–6, 2–7, and 2–8 show the characteristic of the peaking filter at maximum gain. The coring circuit reduces the low-level, high -frequency noise. Figure 2–9 shows the transfer curve of the coring function. The peaking frequency, peaking gain, and coring threshold are programmable.

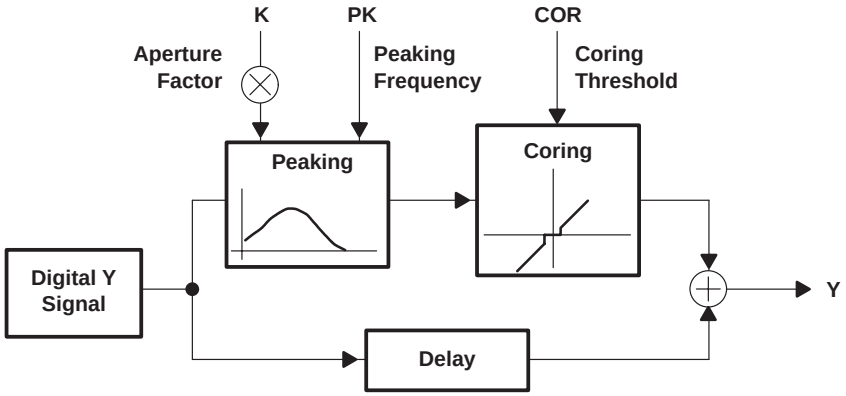


Figure 2–5. Luminance Edge-Enhancer

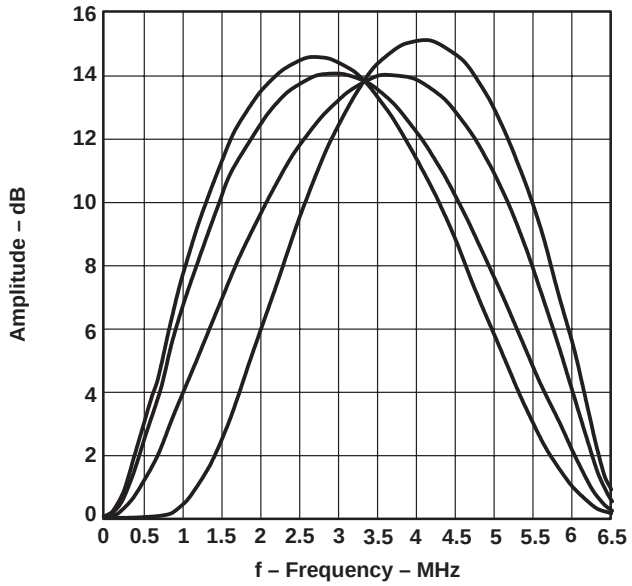


Figure 2–6. Peaking Filter Response, 13.5 MHz Sampling

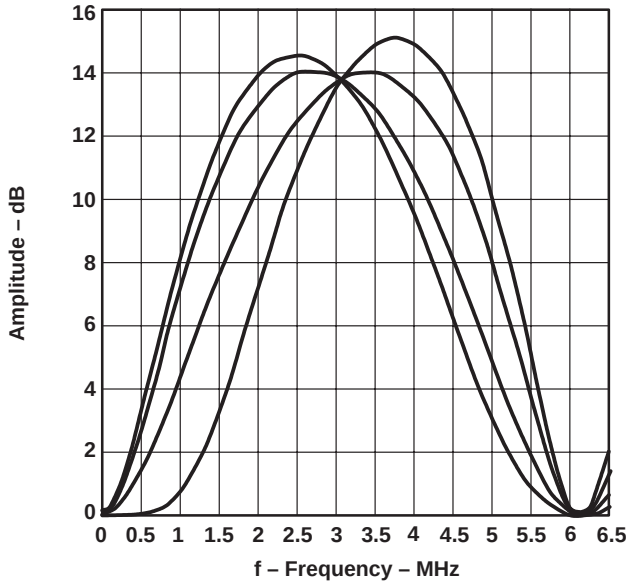


Figure 2–7. Peaking Filter Response, NTSC and PAL-M Square Pixel

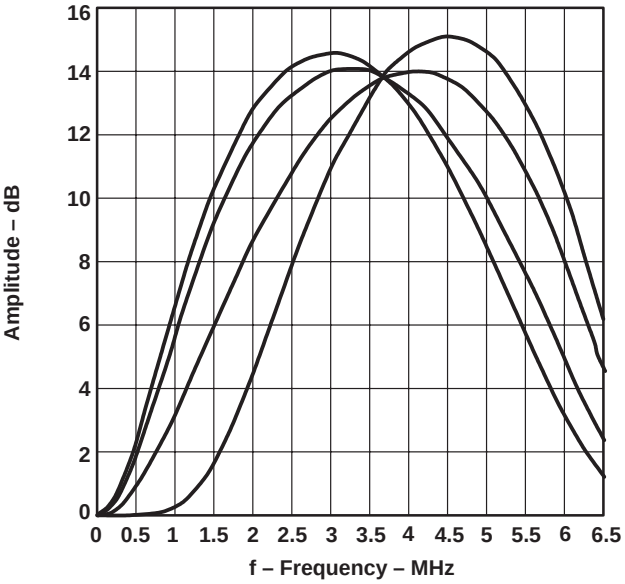


Figure 2–8. Peaking Filter Response, PAL Square Pixel

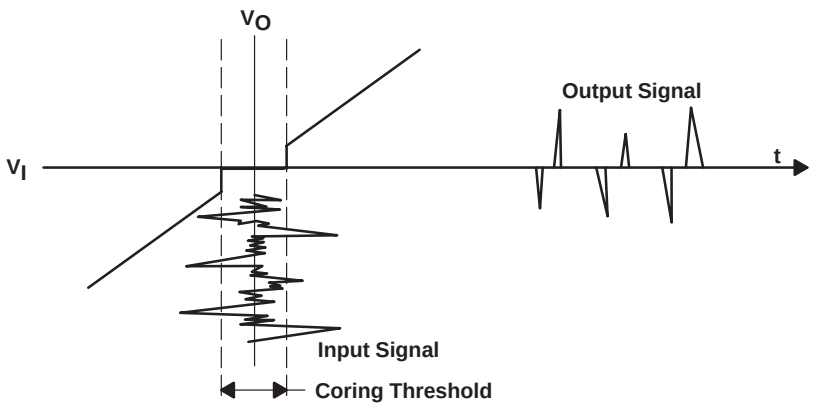


Figure 2–9. Transfer Curve of Coring Circuit

2.2.3 Chrominance Processing

A quadrature demodulator removes the U and V components from the composite signal in composite video mode, or the U and V components from the chroma signal in S-video mode. The U/V signals then pass through the gain control stage for chroma saturation adjustment. The U and V components pass through a comb filter to eliminate cross-chrominance noise. Phase shifting the digitally-controlled oscillator controls hue. The block includes an automatic color killer (ACK) circuit that suppresses the chroma processing when the color burst of the video signal is weak or not present.

2.2.4 Clock Circuits

An Internal line-locked PLL generates the system and pixel clocks. Figure 2–10 shows a simplified clock circuit diagram. The digital control oscillator generates the reference signal for the horizontal PLL.

The DCO outputs a signal that is fed to the D/A converter. The D/A converter outputs a line-locked clock signal (LCLK). The DCO requires a 26.8 or a 24.576 MHz clock as an input. The input for the DCO may enter terminal XTAL1 as TTL. Another input for the DCO may be a 26.8 or 24.576 MHz crystal connected across terminals XTAL1 and XTAL2. The crystal input requires passive tuning circuits to activate the internal crystal oscillator circuitry. Figure 2–11 shows the various reference clock configurations.

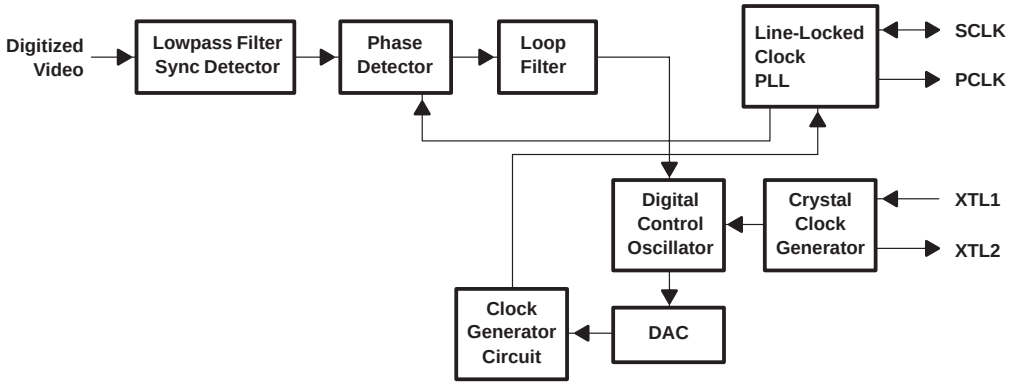


Figure 2–10. Clock Circuit Diagram

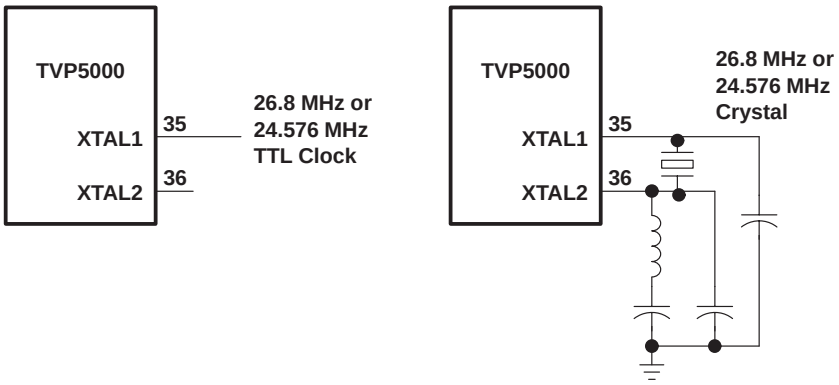


Figure 2–11. Reference Clock Configurations

The sampling frequencies that control the number of pixels per line differ depending on the video format and standards. Table 2–1 shows a summary of the sampling frequencies.

Table 2–1. Summary of the Line Frequencies, Data Rates, and Pixel Counts

STANDARDS	HORIZONTAL LINE RATE (kHz)	PIXELS PER LINE	ACTIVE PIXELS PER LINE	PIXEL PCLK RATE (MHz)	SYSTEM clk2 FREQUENCY (MHz)
NTSC, square-pixel	15.73426	780	640	12.2727	24.54
NTSC, ITU-R BT.601	15.73426	858	720	13.5	27.0
PAL (B,D,G,H,I), square-pixel	15.625	944	768	14.75	29.5
PAL (B,D,G,H,I), ITU-R BT.601	15.625	864	720	13.5	27.0
PAL(M), square-pixel	15.73426	780	640	12.2727	24.54
PAL(M), ITU-R BT.601	15.73426	858	720	13.5	27.0
PAL(N), square-pixel	15.625	944	768	14.75	29.5
PAL(N), ITU-R BT.601	15.625	864	720	13.5	27.0

2.3 I^2C Interface

The I^2C standard consists of two signals, serial input/output data (SDA) line and input/output clock line (SCL), that carry information between the devices connected to the bus. A third signal (I^2CA) is used for slave address selection. Although the I^2C system can be multimastered, the TVP5010 will function as a slave device only.

Both SDA and SCL are bidirectional lines that connect to a positive supply voltage via a pullup resistor. When the bus is free, both lines are high.

The slave address (I^2CA) should be tied high or low to distinguish between two TVP5010 devices commonly on the I^2C bus.

Table 2–3 summarizes the terminal functions of the I^2C mode host interface.

Table 2–2. I^2C Host Port Terminal Description

SIGNAL	TYPE	DESCRIPTION
I^2CA	I	Slave address selection
SCL	I/O (**OD**)	Input/output clock line
SDA	I/O (**OD**)	Input/output data line

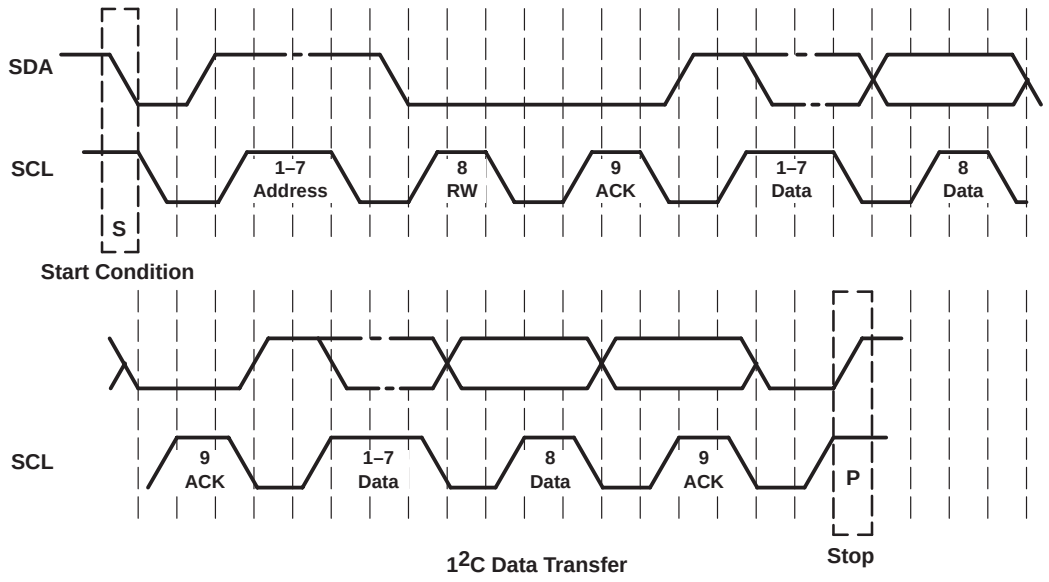


Figure 2–12. I²C Data Transfer Example

Data transfer rate on the bus is up to 400 kbits/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change with the clock signal on the SCL line being low.

- Transferring multiple bytes during one read or write operation, the internal subaddress is not automatically incremented.
- A high to low transition on the SDA line while the SCL is high indicates a start condition.
- A low to high transition on the SDA line while the SCL is high indicates a stop condition
- Acknowledge (SDA low)
- Not–Acknowledge (SDA high)

Every byte placed on the SDA line must be 8 bits long. The number of bytes that can be transferred is unrestricted. An acknowledge bit follows each byte. If the slave can not receive another complete byte of data until it has performed another function, it holds the clock line (SCL) low. An SCL low forces the master into a wait state. Data transfer continues when the slave is ready for another byte of data and releases the clock line (SCL).

Data transfer with acknowledge is necessary. The master generates an acknowledge related clock pulse. The master releases the SDA line high during the acknowledge clock pulse. The slave pulls down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

When a slave does not acknowledge the slave address, the data line is left high. The master then generates a stop condition to abort the transfer.

If a slave acknowledges the slave address, but some time later in the transfer cannot receive any more data bytes, the master again aborts the transfer. The slave indicates a not ready condition by generating the not acknowledge. The slave leaves the data line high and the master generates the stop condition.

If a master-receiver is involved in a transfer, it indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a stop or repeated start condition.

2.3.1 I²C Write Operation

Data transfers occur using the following illustrated formats.

The I²C master initiates a write operation to the TVP5010 by generating a start condition followed by the TVP5010's I²C address (101110X). The address is in MSB first bit order followed by a 0 to indicate a write cycle. After receiving a TVP5010 acknowledge, the I²C master sends a subaddress of the register or the block of registers where it will write. Following the subaddress is one or more bytes of data, with MSB first. The TVP5010 acknowledges the receipt of each byte upon completion of each transfer. The I²C master ends a write operation by generating a stop condition.

The X in the address of the TVP5010 is 0 when the I²CA terminal is low and the X is 1 when the I²CA is high. If the read or write cycle contains more than one byte, the internal subaddress increments automatically.

	0
I²C Start (Master)	S

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General Address (Master)	1	0	1	1	1	0	X	0

	9
I²C Acknowledge (Slave)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write Register Address (Mas)	Addr	Addr	Addr	Addr	Addr	Addr	Addr	Addr

	9
I²C Acknowledge (Slave)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write Data (Master)	Data	Data	Data	Data	Data	Data	Data	Data

	9
I²C Acknowledge (Slave)	A

	0
I²C Stop (Master)	P

2.3.2 I²C Read Operation

The read operation has two phases, the address phase and the data phase. In the address phase, the I²C master initiates a write operation to the TVP5010 by generating a start condition followed by the TVP5010's I²C address (101110X). The address is in MSB first bit order followed by a 0 to indicate a write cycle. After receiving a TVP5010 acknowledge, the I²C master sends a subaddress of the register or the block of registers where it will read. The TVP5010 acknowledges the receipt of the address upon completion of each transfer. The I²C master ends a read operation by generating a stop condition. During the data phase, the I²C master initiates a read operation to the TVP5010 by generating a start condition followed by the TVP5010's I²C address (101110X). The address is in MSB first bit order followed by a 1 to indicate a read cycle. The I²C master acknowledges the receipt of each byte upon completion of each transfer. After the TVP5010 transfers the last byte, the I²C master ends the read operation by generating a not acknowledge followed by a stop condition.

Read Phase 1

	0
I²C Start (Master)	S

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General Address (Master)	1	0	1	1	1	0	X	0

	9
I²C Acknowledge (Slave)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write Register Address (Mas)	Addr	Addr	Addr	Addr	Addr	Addr	Addr	Addr

	9
I²C Acknowledge (Slave)	A

	0
I²C Stop (Master)	P

Read Phase 2

	0
I²C Start (Master)	S

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General Address (Master)	1	0	1	1	1	0	X	1

	9
I²C Acknowledge (Slave)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

	9
I²C Acknowledge (Slave)	/A

	0
I²C Stop (Master)	P

2.3.3 I2C Microcode Write Operation

Data written during the microcode write operation will be written to the TVP5010 program RAM. Upon completion of the microcode download an internal reset will be generated to reset the TVP5010 internal microprocessor and the microprocessor will begin executing microcode from address zero. The internal microprocessor initializes all the I^{2}C registers with their defaults and begins normal operation. All user accesses to I^{2}C registers can proceed from this point.

	0
I^{2}C Start (Master)	S

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^{2}C General Address (Master)	1	0	1	1	1	0	X	0

	9
I^{2}C Acknowledge (Slave)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^{2}C Write Register Address (Mas)	1	1	1	1	0	0	0	0

	9
I^{2}C Acknowledge (Slave)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^{2}C Write Data (Master)	Data	Data	Data	Data	Data	Data	Data	Data

	9
I^{2}C Acknowledge (Slave)	A

	0
I^{2}C Stop (Master)	P

2.3.4 I²C Microcode Read Operation

Data read during the microcode read operation will be read from the TVP5010 Program RAM. Upon completion of the microcode read operation an internal reset will be generated to reset the TVP5010 internal microprocessor and the microprocessor will begin executing microcode from address zero.

	0
I²C Start (Master)	S

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General Address (Master)	1	0	1	1	1	0	X	0

	9
I²C Acknowledge (Slave)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Read Register Address (Master)	1	1	1	1	0	0	0	1

	9
I²C Acknowledge (Slave)	A

	0
I²C Stop (Master)	P

Read Phase 2

	0
I²C Start (Master)	S

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General Address (Master)	1	0	1	1	1	0	X	1

	7
I²C Acknowledge (Slave)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

	7
I²C Acknowledge (Master)	A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Until all data is read from program memory

	9
I²C Acknowledge (Master)	/A

	0
I²C Stop (Master)	P

2.4 Genlock Control

The frequency control word of the internal color subcarrier digital control oscillator (DCO) and the subcarrier phase reset bit are transmitted via the GLCO terminal. The frequency control word is a 23-bit binary number. The frequency of the DCO can be calculated from the following equation:

$$F_{dco} = \frac{F_{ctrl}}{2^{23}} \times F_{sclk}$$

Where F_{dco} is the frequency of the DCO, F_{ctrl} is the 23-bit DCO frequency control, and F_{sclk} is the frequency of the SCLK.

The last bit (bit 0) of the DCO frequency control is always 0.

A write of 1 to bit 4 of the chrominance control register at host port subaddress 1Ah causes the subcarrier DTO phase reset bit to be sent on the next scan line on GLCO. The active low reset bit occurs 8 SCLKs after the transmission of the last bit of DCO frequency control. Upon the transmission of the reset bit, the phase of the TVP5010 internal subcarrier DCO is reset to zero.

A genlocking slave device connected to the GLCO terminal can use the information on GLCO to synchronize its internal color phase DCO to achieve clean line and color lock.

Figure 2–13 shows the timing of GLCO.

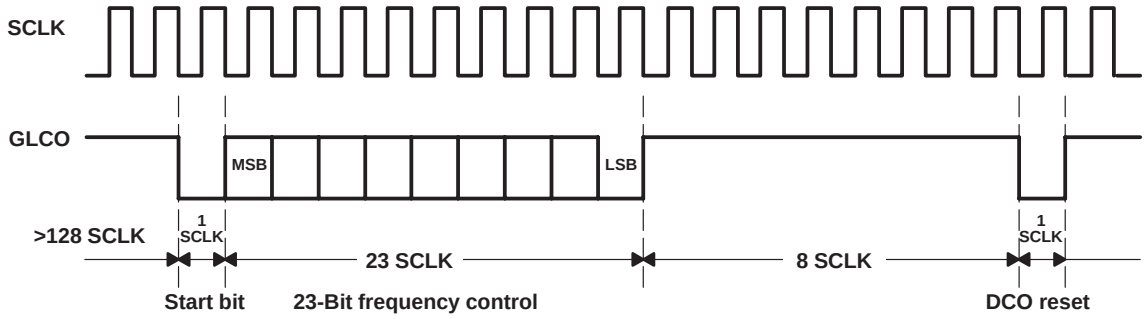


Figure 2–13. GLCO Timing

2.5 Video Port Timing/Formatting

Applying the control signal to the OEB terminal and/or via host port control activates the YUV data outputs or sets them to high–impedance. When the host configures OEB to control the YUV outputs, then a logic 0 on OEB enables the output and a logic 1 puts the YUV output bus in a high impedance state. Alternately, OEB can be tied to ground and host port bus alone controls the YUV terminals. Figure 2–14 shows digital outputs, YUV, and the clock and control timing with OEB as the output control. PCLK and SCLK are the pixel clock and the system clock respectively. The active video indicator (AVID) signal defines which pixels in each horizontal video line contain picture information.

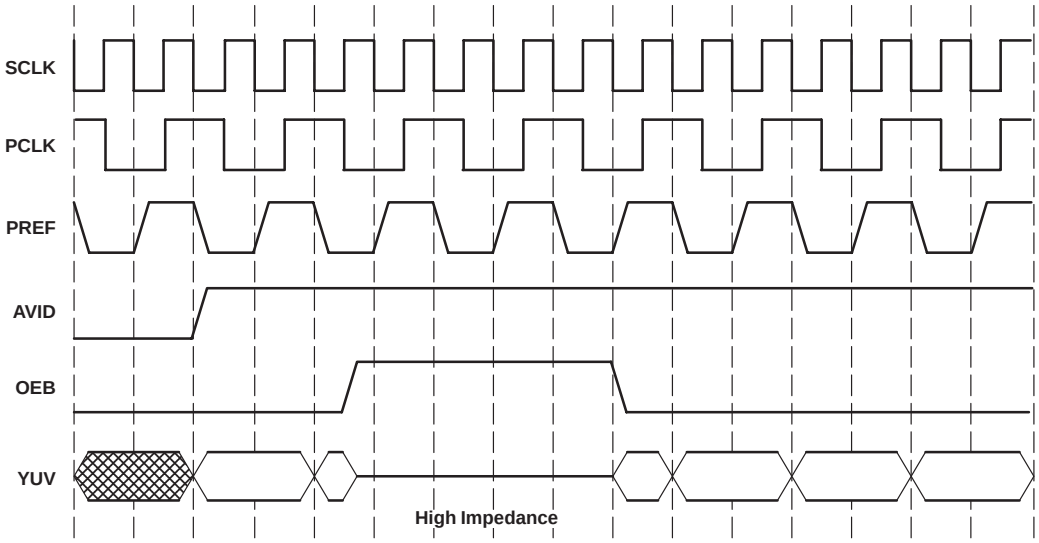


Figure 2–14. Functional Timing

The TVP5010 supports both square–pixel and ITU–R BT.601 sampling formats and multiple Y–UV output formats:

- 16-bit 4:2:2 See Table 2–3
- 12-bit 4:1:1 See Table 2–4
- 8-bit 4:2:2 See Table 2–5
- ITU–R BT.656 bit–parallel interface.

2.6 Video Port 16-bit 4:2:2 Mode

Table 2–3. Output Format: 16-Bit 4:2:2

Y BUS

MSB **LSB**

y	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	Y07	Y06	Y05	Y04	Y03	Y02	Y01	Y00
1	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10
2	Y27	Y26	Y25	Y24	Y23	Y22	Y21	Y20
3	Y37	Y36	Y35	Y34	Y33	Y32	Y31	Y30
4	Y47	Y46	Y45	Y44	Y43	Y42	Y41	Y40
5	Y57	Y56	Y55	Y54	Y53	Y52	Y51	Y50
6	Y67	Y66	Y65	Y64	Y63	Y62	Y61	Y60
7	Y77	Y76	Y75	Y74	Y73	Y72	Y71	Y70
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	Yn–3 7	Yn–3 6	Yn–3 5	Yn–3 4	Yn–3 3	Yn–3 2	Yn–3 1	Yn–3 0
:	Yn–2 7	Yn–2 6	Yn–2 5	Yn–2 4	Yn–2 3	Yn–2 2	Yn–2 1	Yn–2 0
:	Yn–17	Yn–1 6	Yn–1 5	Yn–1 4	Yn–1 3	Yn–1 2	Yn–1 1	Yn–1 0
n†	Yn7	Yn 6	Yn 5	Yn 4	Yn 3	Yn 2	Yn 1	Yn 0

U/V BUS

MSB **LSB**

UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0	uv
U07	U06	U05	U04	U03	U02	U01	U00	
V07	V06	V05	V04	V03	V02	V01	V00	0
U27	U26	U25	U24	U23	U22	U21	U20	
V27	V26	V25	V24	V23	V22	V21	V20	2
U47	U46	U45	U44	U43	U42	U41	U40	
V47	V46	V45	V44	V43	V42	V41	V40	4
U67	U66	U65	U64	U63	U62	U61	U60	
V67	V66	V65	V64	V63	V62	V61	V60	6
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
Un–3 7	Un–3 6	Un–3 5	Un–3 4	Un–3 3	Un–3 2	Un–3 1	Un–3 0	n–3
Vn–3 7	Vn–3 6	Vn–3 5	Vn–3 4	Vn–3 3	Vn–3 2	Vn–3 1	Vn–3 0	
Un–1 7	Un–1 6	Un–1 5	Un–1 4	Un–1 3	Un–1 2	Un–1 1	Un–1 0	
Vn–1 7	Vn–1 6	Vn–1 5	Vn–1 4	Vn–1 3	Vn–1 2	Vn–1 1	Vn–1 0	n–1

† The last pixel number of each active line; n = 639 for NTSC square-pixel, n = 767 for PAL square-pixel, and n = 719 for ITU-R BT.601 (NTSC and PAL).

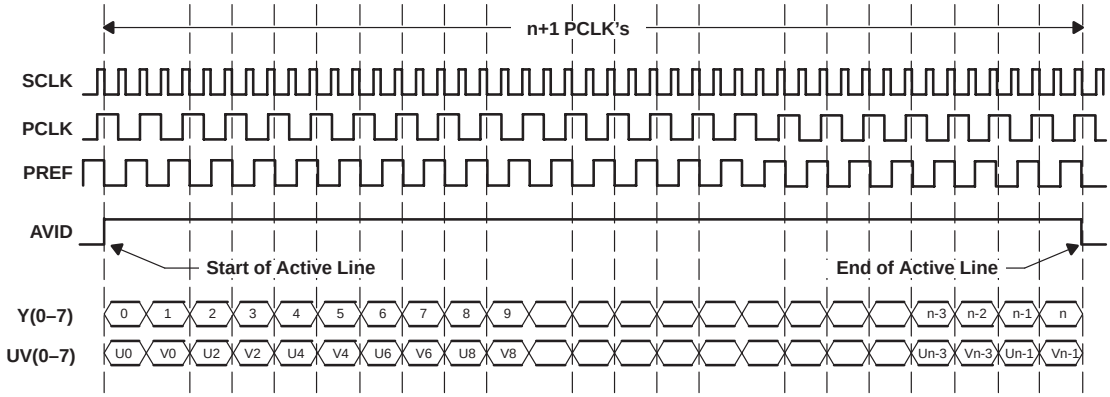


Figure 2–15. 16-Bit 4:2:2 Functional Timing

2.7 Video Port 12-Bit 4:1:1 Mode

Table 2–4. Output Format: 12-Bit 4:1:1

Y BUS

	MSB							LSB
y	**Y7**	**Y6**	**Y5**	**Y4**	**Y3**	**Y2**	**Y1**	**Y0**
0	Y07	Y06	Y05	Y04	Y03	Y02	Y01	Y00
1	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10
2	Y27	Y26	Y25	Y24	Y23	Y22	Y21	Y20
3	Y37	Y36	Y35	Y34	Y33	Y32	Y31	Y30
4	Y47	Y46	Y45	Y44	Y43	Y42	Y41	Y40
5	Y57	Y56	Y55	Y54	Y53	Y52	Y51	Y50
6	Y67	Y66	Y65	Y64	Y63	Y62	Y61	Y60
7	Y77	Y76	Y75	Y74	Y73	Y72	Y71	Y70
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	Y**n–3** 7	Y**n–3** 6	Y**n–3** 5	Y**n–3** 4	Y**n–3** 3	Y**n–3** 2	Y**n–3** 1	Y**n–3** 0
:	Y**n–2** 7	Y**n–2** 6	Y**n–2** 5	Y**n–2** 4	Y**n–2** 3	Y**n–2** 2	Y**n–2** 1	Y**n–2** 0
:	Y**n–1**7	Y**n–1** 6	Y**n–1** 5	Y**n–1** 4	Y**n–1** 3	Y**n–1** 2	Y**n–1** 1	Y**n–1** 0
n†	Y**n**7	Y**n** 6	Y**n** 5	Y**n** 4	Y**n** 3	Y**n** 2	Y**n** 1	Y**n** 0

U/V BUS

MSB								**LSB**
UV7	**UV6**	**UV5**	**UV4**	**uv**	**UV3**	**UV2**	**UV1**	**UV0**
U07	U06	V07	V06	0	These terminals are logic 0 outputs.			
U05	U04	V05	V04					
U03	U02	V03	V02					
U01	U00	V01	V00					
U47	U46	V47	V46	4				
U45	U44	V45	V44					
U43	U42	V43	V42					
U41	U40	V41	V40					
:	:	:	:	:				
:	:	:	:	:				
:	:	:	:	:				
U**n–3** 7	U**n–3** 6	V**n–3** 7	V**n–3** 6	n–3				
U**n–3 5**	U**n–3** 4	V**n–3** 5	V**n–3** 4					
U**n–3 3**	U**n–3** 2	V**n–3** 3	V**n–3** 2					
U**n–3 1**	U**n–3** 0	V**n–3** 1	V**n–3** 0					

† The last pixel number of each active line; n = 639 for NTSC square-pixel, n = 767 for PAL square-pixel, and n = 719 for ITU-R BT.601 (NTSC and PAL).

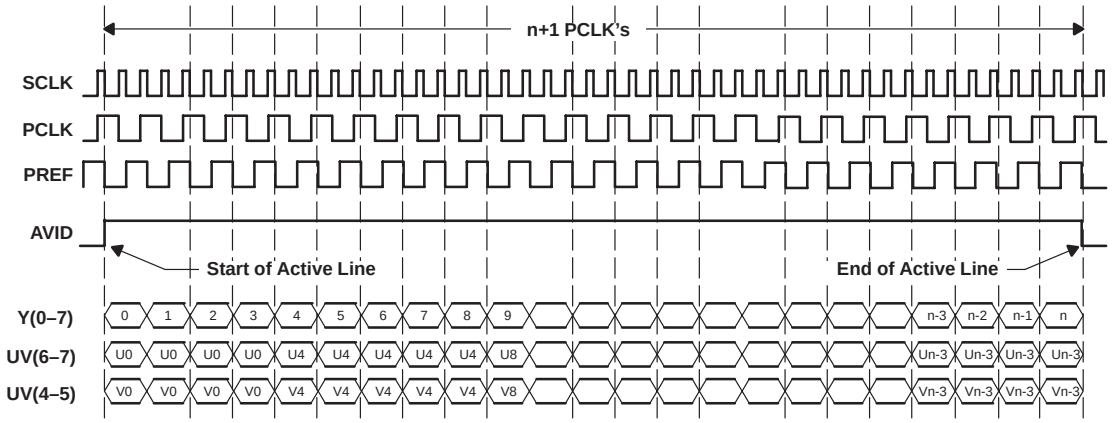


Figure 2–16. 12-bit 4:1:1 Functional Timing

2.8 Video Port 8-Bit 4:2:2 Mode

Table 2–5. Output Format: 8-bit 4:2:2 $U_0Y_0V_0Y_1U_2Y_2V_2Y_3$.....

Y BUS (output)

	MSB							**LSB**
	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	U07	U06	U05	U04	U03	U02	U01	U00
	Y07	Y06	Y05	Y04	Y03	Y02	Y01	Y00
	V07	V06	V05	V04	V03	V02	V01	V00
	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10
	U27	U26	U25	U24	U23	U22	U21	U20
	Y27	Y26	Y25	Y24	Y23	Y22	Y21	Y20
	V27	V26	V25	V24	V23	V22	V21	V20
	Y37	Y36	Y35	Y34	Y33	Y32	Y31	Y30
	U47	U46	U45	U44	U43	U42	U41	U40
	Y47	Y46	Y45	Y44	Y43	Y42	Y41	Y40
	V47	V46	V45	V44	V43	V42	V41	V40
	Y57	Y56	Y55	Y54	Y53	Y52	Y51	Y50
	U67	U66	U65	U64	U63	U62	U61	U60
	Y67	Y66	Y65	Y64	Y63	Y62	Y61	Y60
	V67	V66	V65	V64	V63	V62	V61	V60
	Y77	Y76	Y75	Y74	Y73	Y72	Y71	Y70
	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:
	Un–3 7	Un–3 6	Un–3 5	Un–3 4	Un–3 3	Un–3 2	Un–3 1	Un–3 0
	Yn–3 7	Yn–3 6	Yn–3 5	Yn–3 4	Yn–3 3	Yn–3 2	Yn–3 1	Yn–3 0
	Vn–3 7	Vn–3 6	Vn–3 5	Vn–3 4	Vn–3 3	Vn–3 2	Vn–3 1	Vn–3 0
	Yn–2 7	Yn–2 6	Yn–2 5	Yn–2 4	Yn–2 3	Yn–2 2	Yn–2 1	Yn–2 0
	Un–1 7	Un–1 6	Un–1 5	Un–1 4	Un–1 3	Un–1 2	Un–1 1	Un–1 0
	Yn–1 7	Yn–1 6	Yn–1 5	Yn–1 4	Yn–1 3	Yn–1 2	Yn–1 1	Yn–1 0
	Vn–1 7	Vn–1 6	Vn–1 5	Vn–1 4	Vn–1 3	Vn–1 2	Vn–1 1	Vn–1 0
	Yn 7	Yn 6	Yn 5	Yn 4	Yn 3	Yn 2	Yn 1	Yn 0

UV BUS

UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0
These terminals are high-impedance, or inputs if an external A/D converter is used.							

† The last pixel number of each active line; n = 639 for NTSC square-pixel, n = 767 for PAL square-pixel, and n = 719 for ITU-R BT.601 (NTSC and PAL).

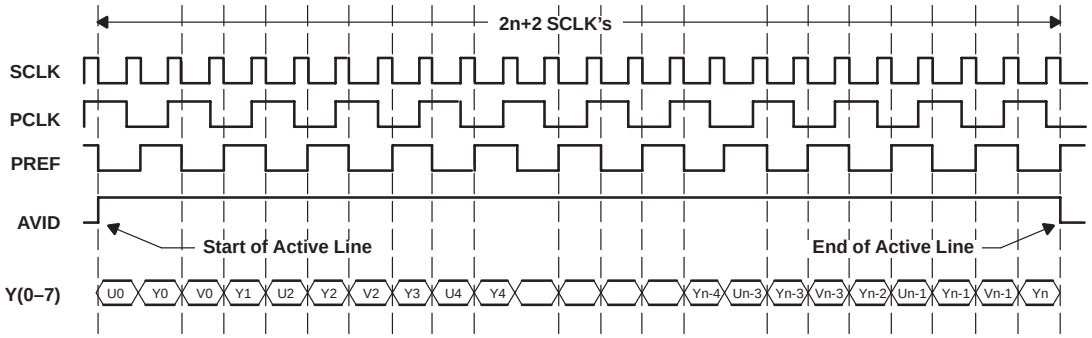


Figure 2–17. 8-Bit (uYvYuYvY) 4:2:2 Functional Timing

2.9 Video Port 8-Bit 656 Mode

Table 2–6. Output Format: 8-bit 656 $U_0Y_0V_0Y_1U_2Y_2V_2Y_3$.....

Y BUS (output)

	MSB							**LSB**
	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	U**0**7	U**0**6	U**0**5	U**0**4	U**0**3	U**0**2	U**0**1	U**0**0
	Y**0**7	Y**0**6	Y**0**5	Y**0**4	Y**0**3	Y**0**2	Y**0**1	Y**0**0
	V**0**7	V**0**6	V**0**5	V**0**4	V**0**3	V**0**2	V**0**1	V**0**0
	Y**1**7	Y**1**6	Y**1**5	Y**1**4	Y**1**3	Y**1**2	Y**1**1	Y**1**0
	U**2**7	U**2**6	U**2**5	U**2**4	U**2**3	U**2**2	U**2**1	U**2**0
	Y**2**7	Y**2**6	Y**2**5	Y**2**4	Y**2**3	Y**2**2	Y**2**1	Y**2**0
	V**2**7	V**2**6	V**2**5	V**2**4	V**2**3	V**2**2	V**2**1	V**2**0
	Y**3**7	Y**3**6	Y**3**5	Y**3**4	Y**3**3	Y**3**2	Y**3**1	Y**3**0
	U**4**7	U**4**6	U**4**5	U**4**4	U**4**3	U**4**2	U**4**1	U**4**0
	Y**4**7	Y**4**6	Y**4**5	Y**4**4	Y**4**3	Y**4**2	Y**4**1	Y**4**0
	V**4**7	V**4**6	V**4**5	V**4**4	V**4**3	V**4**2	V**4**1	V**4**0
	Y**5**7	Y**5**6	Y**5**5	Y**5**4	Y**5**3	Y**5**2	Y**5**1	Y**5**0
	U**6**7	U**6**6	U**6**5	U**6**4	U**6**3	U**6**2	U**6**1	U**6**0
	Y**6**7	Y**6**6	Y**6**5	Y**6**4	Y**6**3	Y**6**2	Y**6**1	Y**6**0
	V**6**7	V**6**6	V**6**5	V**6**4	V**6**3	V**6**2	V**6**1	V**6**0
	Y**7**7	Y**7**6	Y**7**5	Y**7**4	Y**7**3	Y**7**2	Y**7**1	Y**7**0
	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:
	U**n–3** 7	U**n–3** 6	U**n–3** 5	U**n–3** 4	U**n–3** 3	U**n–3** 2	U**n–3** 1	U**n–3** 0
	Y**n–3** 7	Y**n–3** 6	Y**n–3** 5	Y**n–3** 4	Y**n–3** 3	Y**n–3** 2	Y**n–3** 1	Y**n–3** 0
	V**n–3** 7	V**n–3** 6	V**n–3** 5	V**n–3** 4	V**n–3** 3	V**n–3** 2	V**n–3** 1	V**n–3** 0
	Y**n–2** 7	Y**n–2** 6	Y**n–2** 5	Y**n–2** 4	Y**n–2** 3	Y**n–2** 2	Y**n–2** 1	Y**n–2** 0
	U**n–1** 7	U**n–1** 6	U**n–1** 5	U**n–1** 4	U**n–1** 3	U**n–1** 2	U**n–1** 1	U**n–1** 0
	Y**n–1** 7	Y**n–1** 6	Y**n–1** 5	Y**n–1** 4	Y**n–1** 3	Y**n–1** 2	Y**n–1** 1	Y**n–1** 0
	V**n–1** 7	V**n–1** 6	V**n–1** 5	V**n–1** 4	V**n–1** 3	V**n–1** 2	V**n–1** 1	V**n–1** 0
	Y**n** 7	Y**n** 6	Y**n** 5	Y**n** 4	Y**n** 3	Y**n** 2	Y**n** 1	Y**n** 0

U/V BUS

UV7	**UV6**	**UV5**	**UV4**	**UV3**	**UV2**	**UV1**	**UV0**
These terminals are high-impedance, or inputs if an external A/D converter is used.							

† The last pixel number of each active line; n = 639 for NTSC square-pixel, n = 767 for PAL square-pixel, and n = 719 for ITU-R BT.601 (NTSC and PAL).

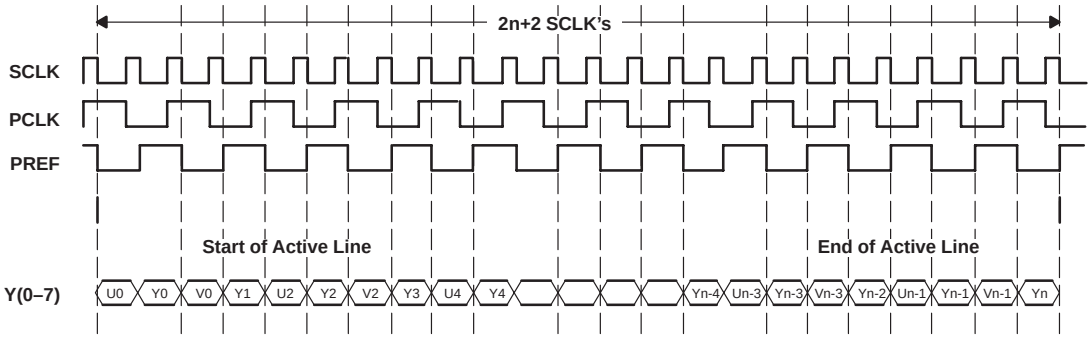


Figure 2–18. 8-Bit (uYvYuYvY) 656 Functional Timing

2.10 Reset

A two-stage reset sequence is initiated at power up or any time the RSTIB pin is brought low. In the first stage all output pins are in high-impedance state, I/O pins are in input mode, and the RSETB pin is low. For a power up reset the device remains in the first stge until an internal low-voltage detect goes away. For a reset inititated by the RSTIB pin the device remains in the first stage until the RSTIB pin goes high. Table 2–7 describes the states of the I/O pins during and after the reset sequence.

Table 2–7. Power-Up Reset Sequence

SIGNAL NAMES	FIRST STAGE	SECOND STAGE	POWER-UP RESET COMPLETED
Duration		128 SCLK	
Y[7:0], UV[7:0], HSYN, VSYN, HBLC, HSIN, AVID	High-impedance	High-impedance	High-impedance
LCLk, SCLK, PCLK, PREF, PALI, GLCO	High-impedance	Active	Active
RSTIB, SDA, SCL, I^2CA, OEB, GPCL	Input	Input	Input
RSETB	Low	Low	High

2.11 Internal Control Registers

A set of internal registers initializes and controls the TVP5010. These registers set all the device operating parameters. Communication between the external controller and TVP5010 is through a standard I^2C interface port. Table 2–8 shows the summary of these registers. The reserved bits must be written with 0. The detailed programming information of each register is described in the following sections.

Table 2–8. Registers Summary

REGISTER FUNCTION	I^2C	R/W
Video input source selection	00h	W
Analog channel controls	01h	W
Operation mode controls	02h	W
Miscellaneous controls	03h	W
Reserved	04 – 5h	W
Color killer threshold control	06h	W
Luminance processing controls–#1	07h	W
Luminance processing controls–#2	08h	W
Brightness control	09h	W
Color saturation control	0Ah	W
Color hue control	0Bh	W

Table 2–8. Registers Summary (Continued)

REGISTER FUNCTION	I^2C	R/W
Contrast control	0Ch	W
Outputs and data rate select	0Dh	W
Reserved	0E – 15h	W
Horizontal sync start NTSC	16h	W
Horizontal sync start PAL	17h	W
Vertical blanking start	18h	W
Vertical blanking stop	19h	W
Chroma processing control #1	1Ah	W
Reserved	1B – 1Fh	W
Analog input source selection	20h	W
Reserved	21 – 7Fh	
Device ID	80h	R
Status #1	81h	R
Status #2	82h	R
Status #3	83h	R
Status #4	84h	R
Reserved	85 – EFh	
Program RAM write	F0	W
Program RAM read	F1	R
Reserved	F2 – FFh	

2.11.1 Analog Input Source Selection #1 Sub-Address = 00

7	6	5	4	3	2	1	0
Reserved						Channel 1 source selection	Channel 2 source selection

Channel 1 source selection:

0 = VI1A selected (default)

1 = VI1B selected

Channel 2 source selection:

0 = VI2A selected (default)

1 = VI2B selected

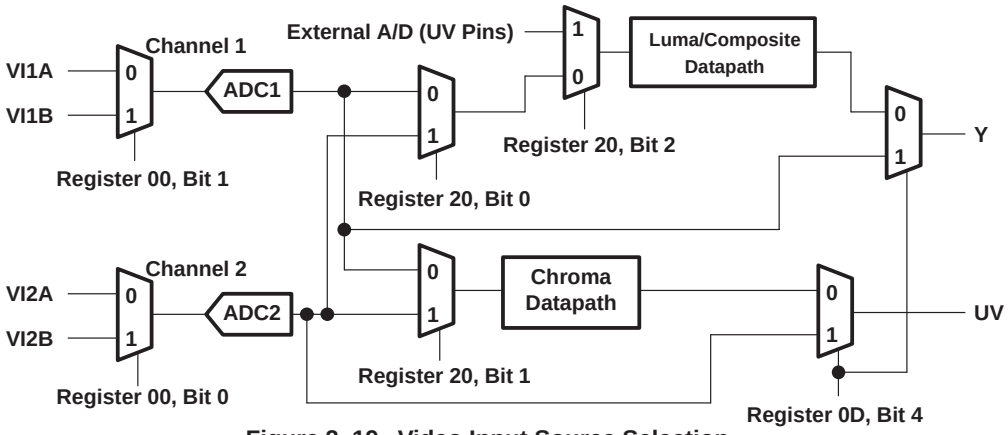


Figure 2–19. Video Input Source Selection

Table 2–9. Video Input Source Selection

	INPUT(s) SELECTED	ADDRESS 00		ADDRESS 20	
		BIT 1	BIT 0	BIT 1	BIT 0
Composite	1A	0	x	x	0
	1B	1	x	x	0
	2A	x	0	x	1
	2B	x	1	x	1
S-video	1A luma, 2A chroma	0	0	1	0
	1A luma, 2B chroma	0	1	1	0
	1B luma, 2A chroma	1	0	1	0
	1B luma, 2B chroma	1	1	1	0
	2A luma, 1A chroma	0	0	0	1
	2A luma, 1B chroma	1	0	0	1
	2B luma, 1A chroma	0	1	0	1
	2B luma, 1B chroma	1	1	0	1

2.11.2 Analog Channel Controls

This register (Sub-Address = 01h) defines the AGCs and static gain controls of both analog channels.

- d1:d0 AGC for analog channels 1 and 2
- d3:d2 automatic clamping active channel 1
- d5:d4 automatic clamping active channel 2
- d7:d6 reserved

7	6	5	4	3	2	1	0
Reserved		Automatic clamping control. Channel 2		Automatic clamping control. Channel 1		Automatic gain control	

Automatic clamping control, channel 2:

00 = Reserved

01 = Automatic clamping enabled (default)

10 = Reserved

11 = Clamping level frozen

Automatic clamping control, channel 1:

00 = Reserved

01 = Automatic clamping enabled (default)

10 = Reserved

11 = Clamping level frozen

Automatic gain control:

00 = Reserved

01 = AGC enabled using luma input as the reference.

10 = Reserved

11 = AGC frozen

2.11.3 **Operation Mode Controls** Sub-Address = 02h

This register defines the various operational modes for this device.

- d0 – activates the power-down mode
- d3:d1 reserved
- d5:d4 specify TV/VCR mode (Standard/non-standard video)
- d7:d6 defines video bus width from external A/D and functionality of terminals OEB and GPCL

VIP address	102h
VMI address	02h
I2C address	02h

7	6	5	4	3	2	1	0
External A/D width		TV/VCR mode		Reserved	Reserved	Reserved	Power down mode

External A/D width:

00 = 8-bit external A/D

01 = 9-bit external A/D terminal OEB is the LSB of the 9-bit input data

10 = 10-bit external A/D terminal GPCL is the LSB of the 10–bit input data, and terminal OEB is the next–to–LSB (default)

11 = Reserved

TV/VCR mode:

00 = Automatic mode determined by the internal detection circuit (default)

01 = Reserved

10 = VCR (nonstandard video) mode

11 = TV (standard video) mode

Power down mode:

0 = Normal operation (default)

1 = Power down mode

2.11.4 Miscellaneous Controls

This register (Sub-Address = 03h) defines various control functions.

- d0 clock enable
- d1 vertical banking on/off control
- d2 unused
- d3 activates the Horizontal sync (HSYN), vertical sync (VSYN), and active video indicator (AVID)
- d4 activates YUV outputs
- d5 specify the functions of terminal PALI and terminal FID
- d7:d6 selects the function of terminal GPCL

7	6	5	4	3	2	1	0
Terminal GPCL function select		Terminals PALI and FID function select	YUV output enable	HSYN, VSYN, AVID enable	Reserved	Vertical blanking on/off	Clock enable

Terminal XX (GPCL) function select:

00 = Terminal # GPCL is logic 0 output (default)

01 = Terminal # GPCL is logic 1 output

10 = Terminal # GPCL is vertical blank output

11 = Terminal # GPCL is external sync lock control input

Terminals PALI and FID function select:

0 = Terminal PALI outputs PAL indicator signal and Terminal FID outputs field ID signal (default)

1 = Terminal PALI outputs horizontal lock indicator (HLK) and Terminal FID outputs vertical lock indicator (VLK)

YUV output enable:

0 = YUV high impedance (default)

1 = YUV active

Horizontal sync (HSYN) ,Vertical sync (VSYN) and Active video indicator (AVID) outputs enable:

0 = HSYN, VSYN, and AVID disabled, (high impedance state) (default)

1 = HSYN, VSYN, and AVID active

Vertical blanking on/off control:

0 = Vertical blanking off (default)

1 = Vertical blanking on

Clock enable:

0 = SCLK and PCLK outputs are high impedance (default)

1 = SCLK and PCLK outputs are enabled

Table 2–10. Digital Output Controls

YUV Output Enable	OEB	YUV OUTPUT
0	0	High impedance
0	1	High impedance
1	0	Active
1	1	High impedance

NOTE:
The YUV outputs are unaffected by OEB when OEB is defined to be a data input terminal. OEB is a data input terminal when ABDY = 1 (subaddress 20, bit 2) and SLK1:0 = 00 (sub-address 02, bits 7:6) When OEB is a data input terminal the YUV outputs can only be switched between the active and high impedance states with the YUV output enable bit under host control.

2.11.5 Color Killer Threshold Control

This register (Sub-Address = 06h) sets the color killer threshold level.

- d4:d0 set threshold level of color killer
- d6:d5 set automatic color killer
- d7 reserved, logical 0

7	6	5	4	3	2	1	0
Reserved	Automatic color killer		Color killer threshold				

Automatic color killer:

00 = Automatic mode (default)
10 = Color killer enabled
11 = Color killer disabled
01 = Reserved

Color killer threshold (ref. 0 dB = nominal burst amplitude):

1 1 1 1 1 = – 30 dB
1 0 0 0 0 = – 24 dB (default)
0 0 0 0 0 = –18 dB

2.11.6 Luminance Processing Control 1

This register (Sub-Address = 07h) sets the characteristics of the luminance signal processing.

- d3:d0 adjust the luminance signal delay time
- d4 luminance in bypass during vertical blanking period
- d5 set function of VSYN terminal
- d7 reserved bits, logical 0

7	6	5	4	3	2	1	0
Reserved	Pedestal	Vertical sync polarity select	Luma bypass during vertical blank	Luminance signal delay with respect to chrominance signal			

Pedestal:

0 = Incoming NTSC signal includes pedestal. (default)

1 = Incoming NTSC signal includes no pedestal.

Vertical sync polarity:

0 = Vertical sync. VSYN is high for 6 lines each field (default)

1 = Vertical sync (active low). VSYN is low for 6 lines each field.

Luminance bypass mode during vertical blanking:

0 = No (default)

1 = Yes

Luma signal delay with respect to chroma signal in pixel clock increments (range –8 to 7 pixel clocks):

1 1 1 1 = –8 pixel clocks delay

1 0 1 1 = –4 pixel clocks delay

1 0 0 0 = –1 pixel clocks delay

0 0 0 0 = 0 pixel clocks delay (default)

0 0 1 1 = 3 pixel clocks delay

0 1 1 1 = 7 pixel clocks delay

2.11.7 Luminance Processing Control 2

This register (Sub-Address = 08h) sets the characteristics of the luminance signal processing-peaking bandpass and peaking factors.

- d1:d0 control the luminance peaking bandpass frequencies
- d3:d2 set the peaking gain
- d5:d4 set the threshold of coring circuits
- d6:d7 select luminance filter

7	6	5	4	3	2	1	0
Luma filter select		Coring threshold		Peaking gain		Peaking frequency	

Luminance filter select:

00 = Automatic select (default)
01 = Reserved
10 = Notch filter
11 = Comb filter

Coring threshold:

00 = Coring off (default)
01 = ±1 LSB
10 = ±2 LSB
11 = ±3 LSB

Peaking gain:

00 = Peaking disabled (default)
01 = 6 dB
10 = 12 dB
11 = 18 dB

Peaking frequency:

Square-pixel sampling rate:

	NTSC	PAL	PAL M	PAL N	
00 =	3.8 MHz	4.5 MHz	3.8 MHz	4.5 MHz	(default)
01 =	3.4 MHz	4.1 MHz	3.4 MHz	4.1 MHz	
10 =	2.5 MHz	3.0 MHz	2.5 MHz	3.0 MHz	
11 =	2.7 MHz	3.2 MHz	2.7 MHz	3.2 MHz	

ITU-R BT.601 sampling rate:

	ALL STANDARDS	
00 =	4.1 MHz	(default)
01 =	3.7 MHz	
10 =	2.8 MHz	
11 =	3.0 MHz	

2.11.8 Brightness Control

This register (Sub-Address = 09h) sets the brightness level.

7	6	5	4	3	2	1	0
Brightness control							

Brightness:

1 1 1 1 1 1 1 1 = 255 (bright)
1 0 0 0 1 0 1 1 =139 (ITU-R BT.601 level)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (dark)

2.11.9 Color Saturation Control

This register (Sub-Address = 0Ah) sets the color saturation level.

7	6	5	4	3	2	1	0
Saturation control							

Saturation:

1 1 1 1 1 1 1 1 = 255 (maximum)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (no color)

2.11.10 Hue Control

This register (Sub-Address = 0Bh) sets the hue of the color signal.

7	6	5	4	3	2	1	0
Hue control							

Hue:

0 1 1 1 1 1 1 1 = 180 degrees
0 0 0 0 0 0 0 0 = 0 degrees (default)
1 0 0 0 0 0 0 0 = –180 degrees

2.11.11 Contrast Control

This register (Sub-Address = 0Ch) sets the contrast level.

7	6	5	4	3	2	1	0
Contrast control							

Contrast:

1 1 1 1 1 1 1 1 = 255 (maximum contrast)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (minimum contrast)

2.11.12 Outputs and Data Rates Select

This register (Sub-Address = 0Dh) selects the output formats and the data rates.

- d2:d0–define the output formats : 4:2:2, 4:1:1, or special formats
- d3–reserved
- d4–output selection: bypass or nonbypass of decoder function
- d5–UV in straight binary or offset binary
- d6–YUV coding range
- d7–reserved , logical 0

7	6	5	4	3	2	1	0
Reserved	YUV output code range	UV code format	YUV data path bypass	Reserved	YUV output format		

YUV output code range:

0 = ITU-R BT.601 coding range (Y ranges from 16 to 235, Cr and Cb range from 16 to 240) (default)

1 = Extended coding range (Y, Cr, and Cb range form 1 to 254)

UV code format:

0 = Offset binary code (2's complement + 128) (default)

1 = Straight binary code (2's complement)

YUV data path bypass:

0 = Normal operation (default)

1 = YUV output terminals connected to A–D output, decoder function bypassed, for test purpose only

YUV output format:

000 = 16-bit 4:2:2 YUV (default)

001 = Reserved

010 = 12-bit 4:1:1 YUV

011 = Reserved

100 = 8-bit 4:2:2 uYvYuYvY

101 = Reserved

110 = Reserved

111 = 8-bit ITU-R BT. 656 interface

2.11.13 Horizontal Sync (HSYN) Start for NTSC

This register (Sub-Address = 16h) adjusts the position of horizontal sync pulse, HSYN for NTSC.

7	6	5	4	3	2	1	0
HSYN start							

HSYN start:

1 1 1 1 1 1 1 1 = –127 × 4 pixel clocks

1 1 1 1 1 1 1 0 = –126 × 4 pixel clocks

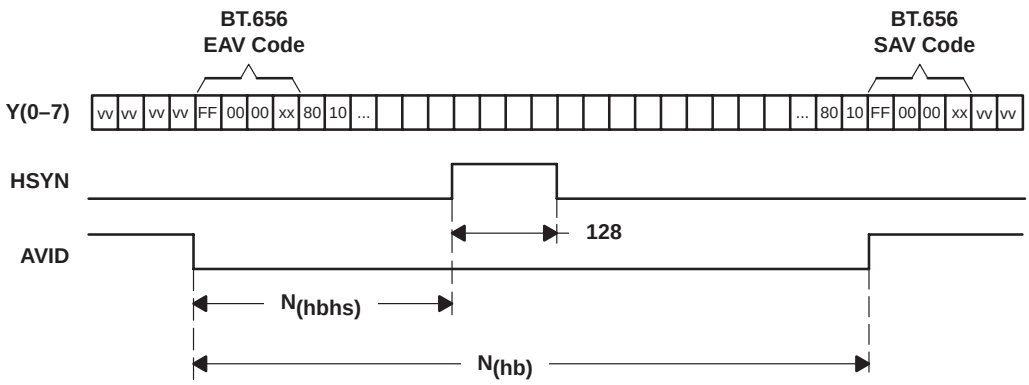
1 1 1 1 1 1 0 1 = –125 × 4 pixel clocks

1 0 0 0 0 0 0 0 = 0 pixel clocks (default)

0 1 1 1 1 1 1 1 = 1 × 4 pixel clocks

0 1 1 1 1 1 1 0 = 2 × 4 pixel clocks

0 0 0 0 0 0 0 0 = 128 × 4 pixel clocks



Clock Delays (SCLK's)

Standard	$N_{(hbhs)}$	$N_{(hb)}$
NTSC 13.5 MHz	32	272
PAL 13.5 MHz	24	284
NTSC Square Pixel	44	276
PAL Square Pixel	52	348

2.11.14 Horizontal Sync (HSYN) Start for PAL

This register (Sub-Address = 17h) adjusts the position of horizontal sync pulse, HSYN for PAL.

BIT	Mnemonic	FUNCTION DESCRIPTIONS								
d7:d0	HSP7:HSP0	d7	d6	d5	d4	d3	d2	d1	d0	Delay time in # of 4 pixel clock cycles time
		1	1	1	1	1	1	1	1	–127
		1	1	1	1	1	1	1	0	–126
		1	1	1	1	1	1	0	1	–125
		..	..	..	..	..	..	..	..	..
		1*	0	0	0	0	0	0	0	0 (* indicates the default setting)
		0	1	1	1	1	1	1	1	1
		0	1	1	1	1	1	1	0	2
		..	..	..	..	..	..	..	..	..
		0	0	0	0	0	0	0	0	128

2.11.15 Vertical Blanking (VBLK) Start

This register (Sub-Address = 18h) adjusts the start position of vertical blanking signal VBLK.

7	6	5	4	3	2	1	0
VBLK start							

VBLK start:

0 1 1 1 1 1 1 1 = 127 lines after start of vertical blanking interval
0 0 0 0 0 0 0 1 = 1 line after start of vertical blanking interval
0 0 0 0 0 0 0 0 = Same time as start of vertical blanking interval (default)
0 1 1 1 1 1 1 1 = 1 line before start of vertical blanking interval
1 0 0 0 0 0 0 0 = 128 lines before start of vertical blanking interval

Table 2–11. Vertical Blanking Interval Start and End

STANDARD	FIELD	START LINE NUMBER	END LINE NUMBER
NTSC	Odd	1	21
	Even	263.5	284.5
PAL	Odd	623.5	23.5
	Even	311	335
MPAL	Odd	523	21
	Even	260.5	284.5
NPAL	Odd	623.5	23.5
	Even	311	335

2.11.16 Vertical Blanking VBLK Stop

This register (Sub-Address = 19h) adjusts the stop position of vertical blanking signal VBLK.

7	6	5	4	3	2	1	0
VBLK end							

VBLK start:

0 1 1 1 1 1 1 1 = 127 lines after end of vertical blanking interval
0 0 0 0 0 0 0 1 = 1 line after end of vertical blanking interval
0 0 0 0 0 0 0 0 = Same time as end of vertical blanking interval (default)
0 1 1 1 1 1 1 1 = 1 line before end of vertical blanking interval
1 0 0 0 0 0 0 0 = 128 lines before end of vertical blanking interval

2.11.17 Chrominance Control 1

This register (Sub-Address = 1Ah) sets the characteristics of the chrominance signal processing.

- d1:d0 activates the automatic color gain control circuits
- d3:d2 chrominance comb filter control
- d4 color reset
- d7:d5 reserved, logical 0

7	6	5	4	3	2	1	0
Reserved			Color reset	Chrominance comb filter control		Automatic color gain control	

YUV output code range:

0 = Color not reset (default)

1 = Color reset. When this bit is set, the subcarrier DTO phase reset bit is transmitted on the next scan line of the genlock control signal GLCO. When the reset bit has been transmitted on GLCO, the phase of the internal subcarrier DCO is reset to zero. The color reset control bit (this bit) is then reset to zero.

Chrominance comb filter control:

00 = Automatic select (default)

01 = Reserved

10 = Comb filter on

11 = Comb filter bypassed

Automatic color gain control

00 = ACC enabled (default)

01 = Reserved

10 = ACC disabled

11 = ACC frozen

2.11.18 Analog Input Source Selection Sub–Address=20h

This register selects various analog input sources (see Figure 2–19 for the details).

- d0 selects ADC1 or ADC2 for luma/composite channel
- d1 selects ADC1 or ADC2 for chroma channel
- d2 external A/D converter select
- d7:d3 reserved. logical 0.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	External A/D select	Chroma channel select	Luma/composite channel select

External A/D select

0 = Use internal A/D converters

1 = Use external A/D converter (default)

Chroma channel select

0 = ADC1 selected (default)

1 = ADC2 selected

Luma/Composite channel select:

0 = ADC1 selected (default)

1 = ADC2 selected

2.11.19 Device ID Register Sub-Address = 80h

This register contains the firmware revision number for TVP5020.

7	6	5	4	3	2	1	0
Device ID							

2.11.20 Status Register 1 Sub–Address = 81h

This register contains the internal status of TVP5020

- d0 TVP5020 is receiving video source from TV or VCR
- d1 horizontal sync lock condition
- d2 vertical sync lock condition
- d3 color sub-carrier lock condition
- d4 lost lock indicator
- d5 field rate identifier
- d6 line-alternating status
- d7 peak white detect status

7	6	5	4	3	2	1	0
Peak white detect status	Line-alternating status	Field rate status	Lost lock detect	Color subcarrier lock status	Vertical sync lock status	Horizontal sync lock status	TV/VCR status

Peak white detect status:

0 = Peak white is not detected

1 = Peak white is detected

Line-alternating status:

0 = Non line alternating

1 = Line alternating

Field rate status:

0 = 60 Hz

1 = 50 Hz

Lost lock detect:

0 = No lost lock since status register 1 was last read

1 = Lost lock since status register 1 was last read

Color subcarrier lock status:

0 = Color subcarrier is not locked

1 = Color subcarrier is locked

Vertical sync lock status:

0 = Vertical sync is not locked

1 = Vertical sync is locked

Horizontal sync lock status:

0 = Horizontal sync is not locked

1 = Horizontal sync is locked

TV/VCR status:

0 = TV

1 = VCR

2.11.21 Status Register 2 Sub–Address = 82h

This register contains the internal status of TVP5020

- d0 reserved
- d1 reserved
- d2 reserved
- d3 AGC and clamping lock condition
- d4 field sequence indicator
- d5 PAL switch polarity of line one of odd field
- d7:d6 reserved

7	6	5	4	3	2	1	0
Reserved		PAL switch polarity	Field sequence status	AGC and clamping lock status	Reserved	Reserved	Reserved

PAL switch polarity of first line of odd field:

0 = PAL switch is zero (color burst phase = 135 degree)

1 = PAL switch is one (color burst phase = 225 degree)

Field sequence status:

0 = Even field

1 = Odd field

Automatic gain and clamping lock status:

0 = Automatic gain and clamping is not locked

1 = Automatic gain and clamping is locked

Video present status:

0 = Video is not present

1 = Video is present

Color detect status:

0 = No color is detected

1 = Color is detected

2.11.22 Status Register 3 Sub-Address = 83h

This register contains the current AGC gain.

– d7:d0 – Current AGC gain.

7	6	5	4	3	2	1	0
AGC gain							

AGC gain (step size = 0.831%):

0 0 0 0 0 0 0 0 = 70.7%(–3 dB)

0 1 0 0 0 0 0 0 = 100% (0 dB)

1 0 0 1 0 0 0 0 = 141% (3 dB)

1 1 0 0 0 0 0 0 = 200% (6 dB)

1 1 1 1 1 1 1 1 = 28.3% (9 dB)

2.11.23 Status Register 4 Sub-Address = 84h

This register contains SCH (color DTO subcarrier phase at 50% of the falling edge of horizontal sync of line one of odd field)

– d7:d0 – Current SCH

7	6	5	4	3	2	1	0
Subcarrier to horizontal (SCH) phase							

SCH (color DTO subcarrier phse at 50% of the falling edge of horizontal sync of line one of odd field; step size 360°/256):

0 0 0 0 0 0 0 0 = 0.00 degree

0 0 0 0 0 0 0 1 = 1.41 degree

0 0 0 0 0 0 1 0 = 2.81 degree

1 1 1 1 1 1 1 0 = 357.2 degree

1 1 1 1 1 1 1 1 = 358.6 degree

3 Electrical Specifications

3.1 Absolute Maximum Ratings†

Supply voltage , AV_{DD} . . . . . 7 V
Supply voltage, DV_{DD} . . . . . 5.5 V
Input voltage range, A_{VI} . . . . . –0.5 V to 7 V
Input voltage range, D_{VI} . . . . . –0.3 V to DV_{DD} + 0.3 V
Storage temperature range . . . . . –65°C to 150°C
Operating free-air temperature . . . . . 0°C to 70°C
Total power dissipation (Watts) . . . . . 3.5 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, digital, DV_{DD}	4.5	5	5.5	V
Supply voltage, analog, AV_{DD}	4.75	5	5.25	V
Input voltage, analog (ac coupling necessary), $V_{I\ (p-p)}$	0.5	1	1.26	V
Input voltage high, digital, V_{IH}	2			V
Input voltage low, digital, V_{IL}			0.8	V
Input voltage high, VCO and VC1 in I2C mode, V_{IH} I2C	3			V
Input voltage low, VCO and VC1 in I2C mode, V_{IL}I2C			1.5	V
Output current, Vout=2.4V, I_{OH}	–4	–8		mA
Output current, Vout=0.4V, I_{OL}	4	8		mA
Operating free-air temperature, T_A	0		70	°C
Crystal Specifications				
Frequency (ITU.601 sampling – 13.5 MHz)		24.576		MHz
Frequency (square pixel sampling)		26.800		MHz
Frequency tolerance			±40	ppm

3.3 Electrical Characteristics

NOTE 1: Test Conditions: DV_{DD} = 5 V, AV_{DD} = 5 V, T_A = 70°C unless otherwise specified

3.3.1 Analog Processing and Analog-to-Digital Converters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_i	Input impedance, analog video inputs	By design	200			kΩ
C_i	Input capacitance, analog video inputs	By design			10	pF
ΔG	Gain control range		–2		6	dB
DNL	DC differential nonlinearity	A/D only			1.5	LSB
INL	DC integral nonlinearity	A/D only			1.5	LSB
Fr	Frequency response	6 MHz		–0.9	–3	dB
XTALK	Crosstalk	1 MHz			–50	dB
SNR	Signal-to-noise ratio	1 MHz, 1 Vpp		41		dB
NS	Noise spectrum	50% flat field		52		dB
DP	Differential phase			1		deg
DG	Differential gain			4		%

3.3.2 DC Electrical Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IN(DIG)}$	Digital supply current				380	400	mA
$I_{IN(AN)}$	Analog supply current				81	105	mA
I Ii	Input leakage current					10	µA
C_i	Input capacitance digital inputs		By design			8	pF
V_{OL}	Output voltage	Low				0.4	V
V_{OH}		High		2.4			

NOTE 2: Measured with a load of 10 kΩ in parallel to 15 pF.

3.4 Timing

3.4.1 Clocks, Video Data, Sync Timing

PARAMETER		TEST CONDITIONS (see NOTE 2)	MIN	TYP	MAX	UNIT
δ_{CLK}	Duty cycle PCLK, SCLK		40	50	60	%
$t_{r(SCLK)}$	Rise time SCLK	10% to 90%		3		ns
$t_{f(SCLK)}$	Fall time SCLK	90% to 10%		2		ns
$t_{r(PCLK)}$	Rise time PCLK	10% to 90%		3		ns
$t_{f(PCLK)}$	Fall time PCLK	90% to 10%		2		ns
$t_{d(PCLK)}$	Delay time, SCLK rising edge to PCLK				4	ns
$t_{d(PREF)}$	Delay time, SCLK falling edge to PREF	See Note 3			3	ns
$t_{d(Y:UV)}$	Delay time, SCLK falling edge to Y, UV	See Note 3			5	ns
$t_{d(OUT)}$	Delay time, SCLK falling edge to digital outputs except PCLK, PREF, Y, UV				5	ns
$t_{su(UV)}$	Setup time, UV pins (in input mode) to SCLK falling edge, when PREF high		10			ns
$t_{h((UV)}$	Hold time, UV pins (in input mode) from SCLK falling edge, when PREF high				2	ns
$f_{(I2C)}$	I^2C clock frequency				400	kHz

NOTES: 3. C_L = 50 pF
4. SCLK falling edge may occur up to 2 ns after PREF, Y, UV output transitions.

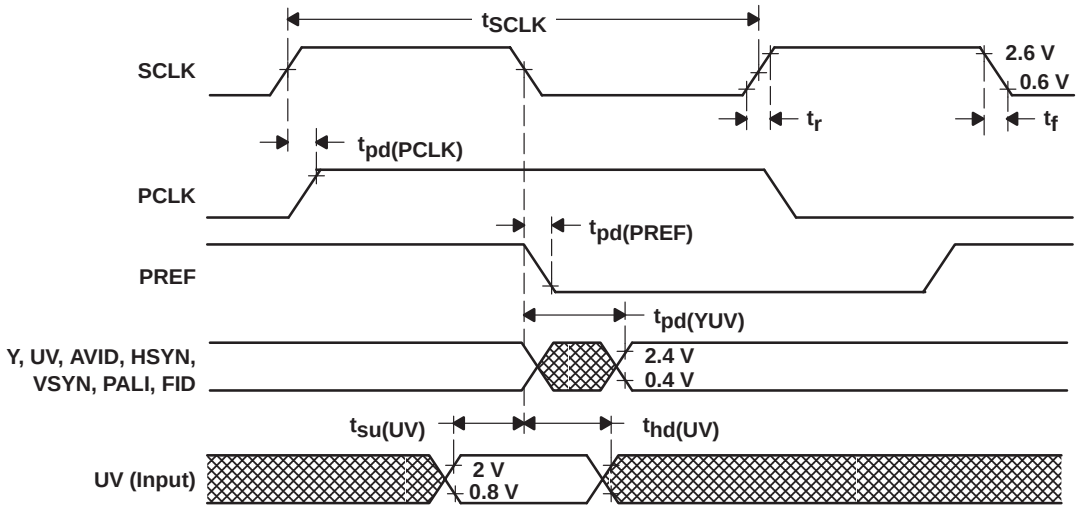


Figure 3–1. Clock, Video, Sync Timing

3.4.2 I²C Host Bus Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BUF}	Bus free time between STOP and START		1.3			µS
$t_{SU:STA}$	Set-up time for a (repeated) START condition		0.6			µS
$t_{HD:STA}$	Hold time (repeated) START condition		0.6			µS
$t_{SU:STO}$	Setup time for a STOP condition		0.6			µS
$t_{SU:DAT}$	Data set-up time		100			nS
$t_{HD:DAT}$	Data hold time		0		0.9	µS
t_R	Rise time VC1 (SDA) and VC0 (SCL) signal				250	nS
t_F	Fall time VC1 (SDA) and VC0 (SCL) signal				250	nS
C_b	Capacitive load for each bus line				400	pF
f_{I2C}	I²C clock frequency				400	kHz

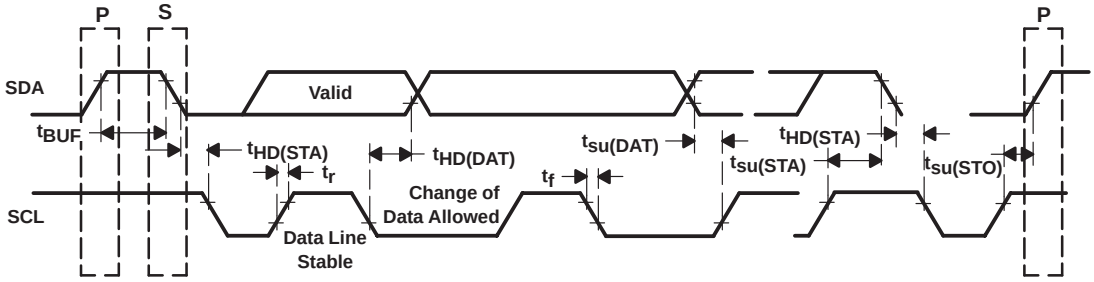
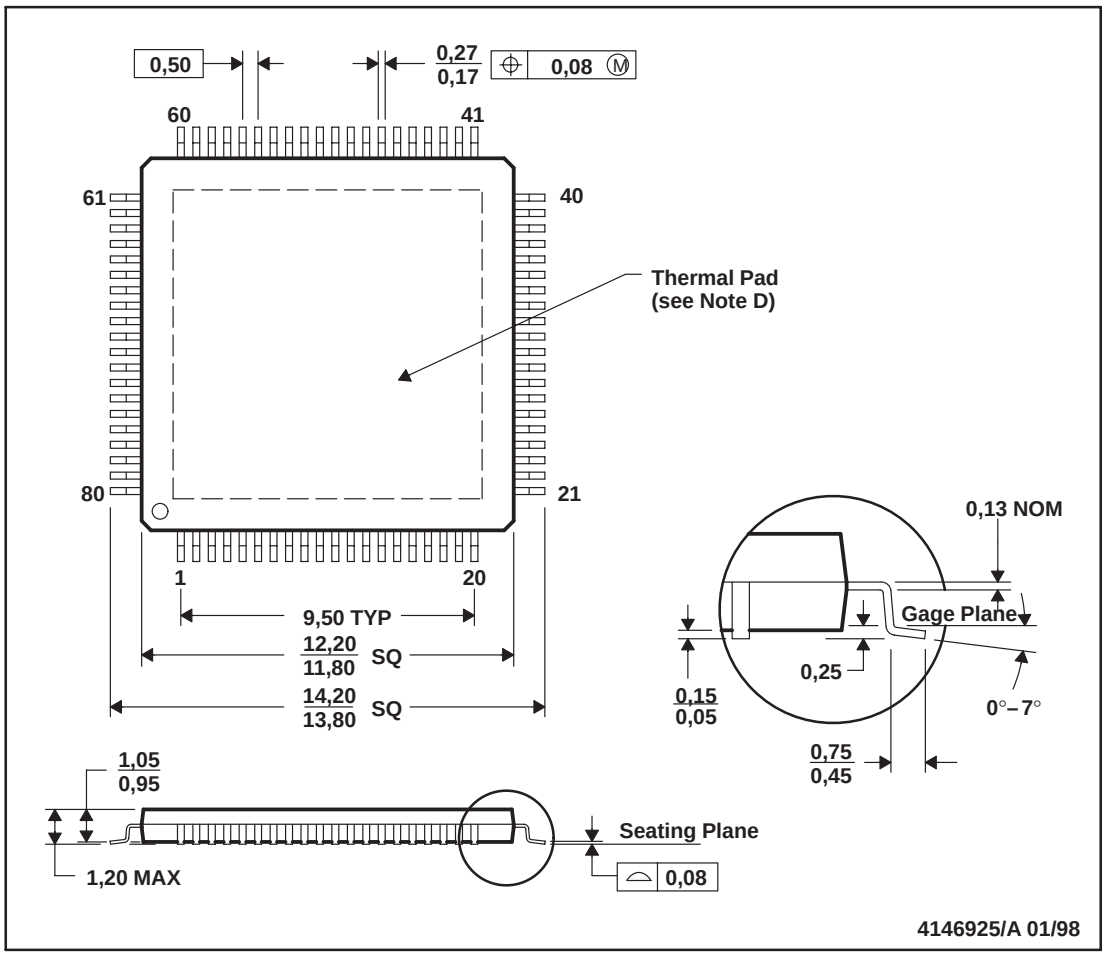


Figure 3–2. I²C Bus Timing

4 Mechanical Data

PFP (S-PQFP-G80) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments Incorporated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TVP5010CPFP	OBSOLETE	HTQFP	PFP	80		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.