International
IOR Rectifier

IRF6702M2DTRPbF
IRF6702M2DTR1PbF

DirectFET™ Power MOSFET ②

Applications

- Dual Common Drain Control MOSFETs for Multiphase DC-DC Converters

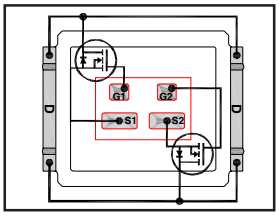
Features

- Replaces Two discrete high side MOSFETs
- Optimized for High Frequency Switching
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible
- Ultra Low Package Inductance
- Compatible with existing Surface Mount Techniques
- RoHS Compliant and Halogen Free
- 100% Rg tested

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$	$R_{DS(on)}$
30V max	±20V max	5.2mΩ@ 10V	8.6mΩ@ 4.5V

$Q_{g\ tot}$	Q_{gd}	Q_{gs2}	Q_{rr}	Q_{oss}	$V_{gs(th)}$
9.4nC	3.3nC	1.2nC	17nC	6.3nC	1.8V



Applicable DirectFET Outline and Substrate Outline ①

S1	S2	SB		M2	M4	MA	L4	L6	L8	

Description

The IRF6702M2DPbF combines two MOSFET switches optimized for high side applications into a single medium can DirectFET package. The switches have low gate resistance and low charge along with ultra low package inductance providing significant reduction in switching losses. The reduced losses make this product ideal for high efficiency multiphase DC-DC converters that power the latest generation of processors operating at higher frequencies.

The IRF6702M2DPbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the highest power density for two MOSFETs in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

Absolute Maximum Ratings (each die operating consecutively)

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V ③	15	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V ③	13	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V ④	47	
I_{DM}	Pulsed Drain Current ⑤	130	
E_{AS}	Single Pulse Avalanche Energy ⑥	71	mJ
I_{AR}	Avalanche Current ⑤	12	A

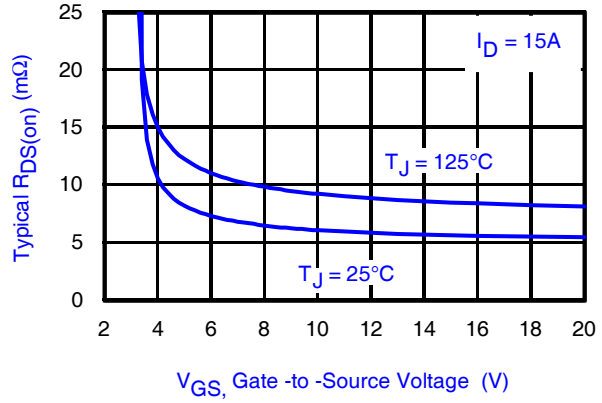


Fig 1. Typical On-Resistance vs. Gate Voltage

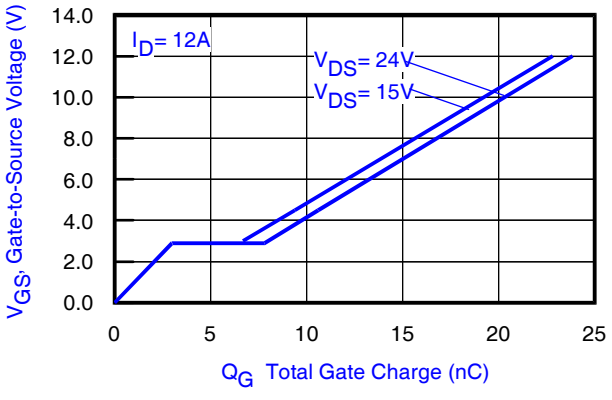


Fig 2. Typical Total Gate Charge vs Gate-to-Source Voltage

Notes:

① Click on this section to link to the appropriate technical paper.
② Click on this section to link to the DirectFET Website.
③ Surface mounted on 1 in. square Cu board, steady state.
④ T_C measured with thermocouple mounted to top (Drain) of part.
⑤ Repetitive rating; pulse width limited by max. junction temperature.
⑥ Starting T_J = 25°C, L = 0.99mH, R_G = 25Ω, I_{AS} = 12A.

Static @ T_J = 25°C (each die unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	20	—	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.2	6.6	mΩ	V_{GS} = 10V, I_D = 15A ⑦
		—	8.6	11.3		V_{GS} = 4.5V, I_D = 12A ⑦
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	V_{DS} = V_{GS}, I_D = 25µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-7.2	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		—	—	150		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	34	—	—	S	V_{DS} = 15V, I_D =12A
Q_g	Total Gate Charge	—	9.4	14		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	2.2	—		V_{DS} = 15V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	1.2	—	nC	V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	—	3.3	—		I_D = 12A
Q_{godr}	Gate Charge Overdrive	—	2.7	—		See Fig. 2
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	4.5	—		
Q_{oss}	Output Charge	—	6.3	—	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	—	0.4	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	14	—		V_{DD} = 15V, V_{GS} = 4.5V ⑦
t_r	Rise Time	—	41	—		I_D = 12A
$t_{d(off)}$	Turn-Off Delay Time	—	15	—	ns	R_G= 6.8Ω
t_f	Fall Time	—	20	—		
C_{iss}	Input Capacitance	—	1380	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	290	—	pF	V_{DS} = 15V
C_{rss}	Reverse Transfer Capacitance	—	120	—		f = 1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	32	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	130		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 12A, V_{GS} = 0V ⑦
t_{rr}	Reverse Recovery Time	—	16	24	ns	T_J = 25°C, I_F =12A
Q_{rr}	Reverse Recovery Charge	—	17	26	nC	di/dt = 370A/µs ⑦

Notes:

⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑦ Pulse width ≤ 400µs; duty cycle ≤ 2%.

Absolute Maximum Ratings (each die operating consecutively)

	Parameter	Max.	Units
P_D @T_A = 25°C	Power Dissipation ③	2.7	W
P_D @T_A = 70°C	Power Dissipation ③	1.9	
P_D @T_C = 25°C	Power Dissipation ④	25	
T_P	Peak Soldering Temperature	270	°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	

Thermal Resistance (each die operating consecutively)

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③⑩	—	56	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑧⑩	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨⑩	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑩	—	5.9	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.018		W/°C

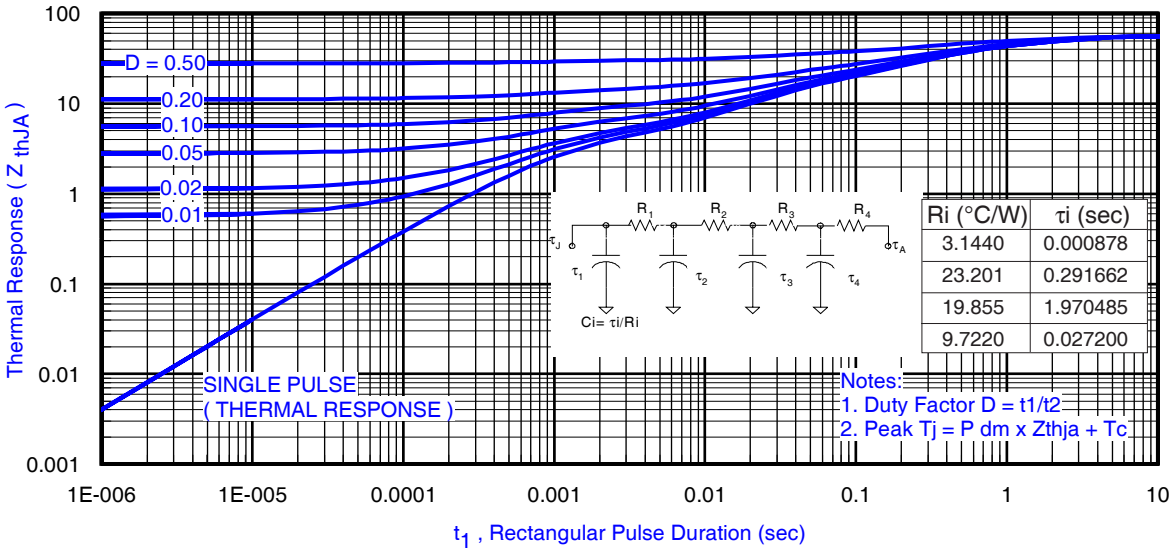


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①

Notes:

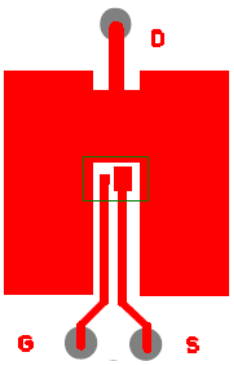
③ Surface mounted on 1 in. square Cu board, steady state.

④ T_C measured with thermocouple incontact with top (Drain) of part.

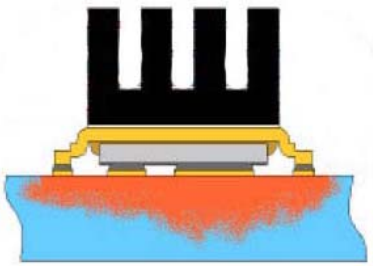
⑧ Used double sided cooling, mounting pad with large heatsink.

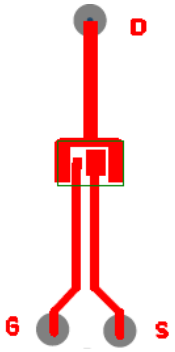
⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

⑩ R_θ is measured at T_J of approximately 90°C.



③ Surface mounted on 1 in. square Cu board (still air).





⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink. (still air)

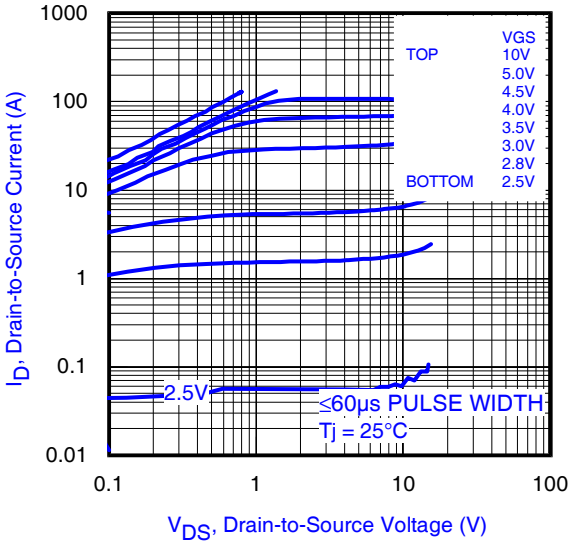


Fig 4. Typical Output Characteristics

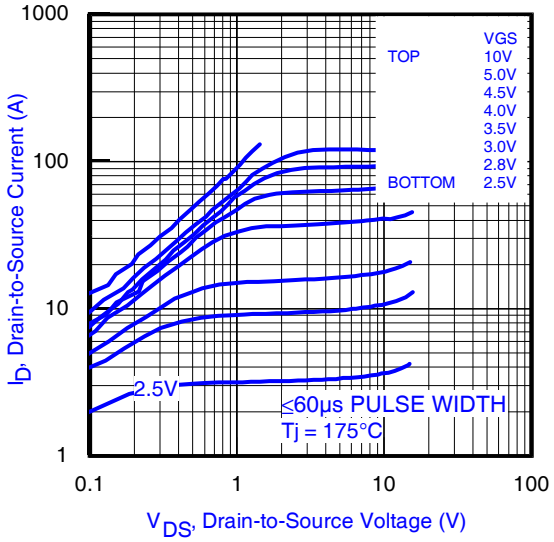


Fig 5. Typical Output Characteristics

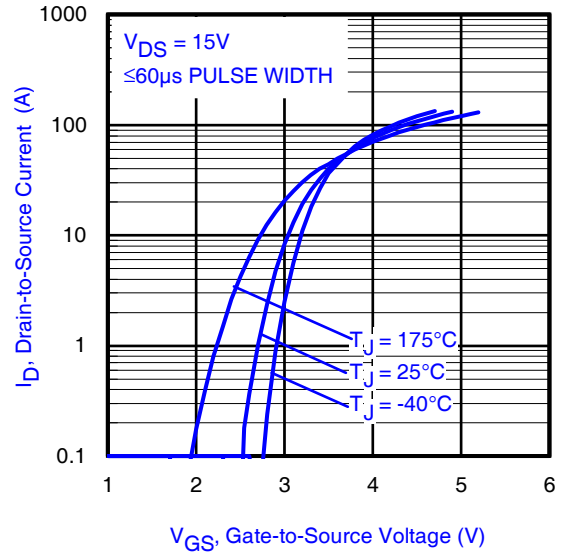


Fig 6. Typical Transfer Characteristics

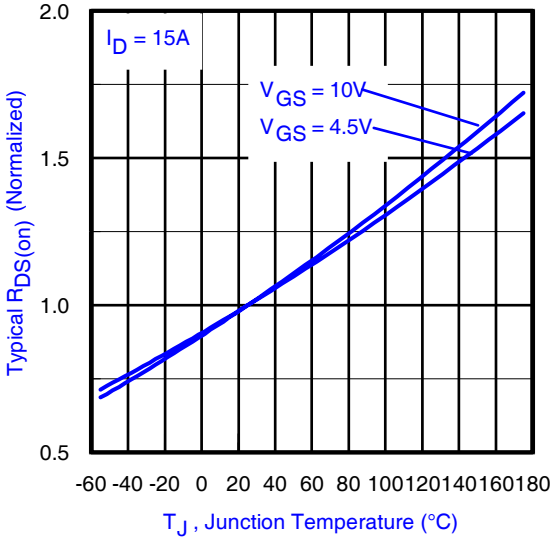


Fig 7. Normalized On-Resistance vs. Temperature

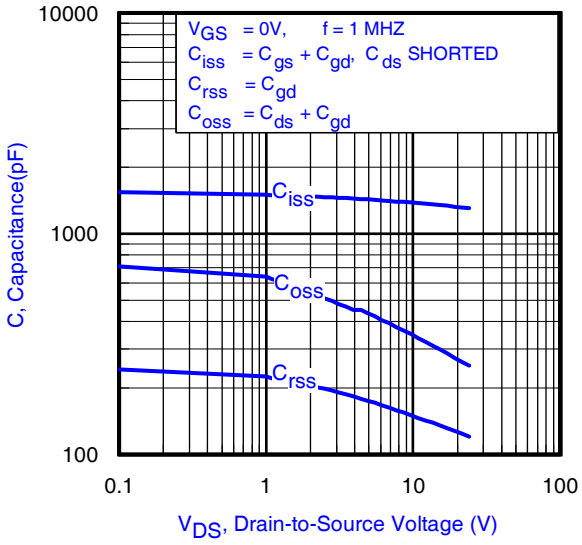


Fig 8. Typical Capacitance vs.Drain-to-Source Voltage

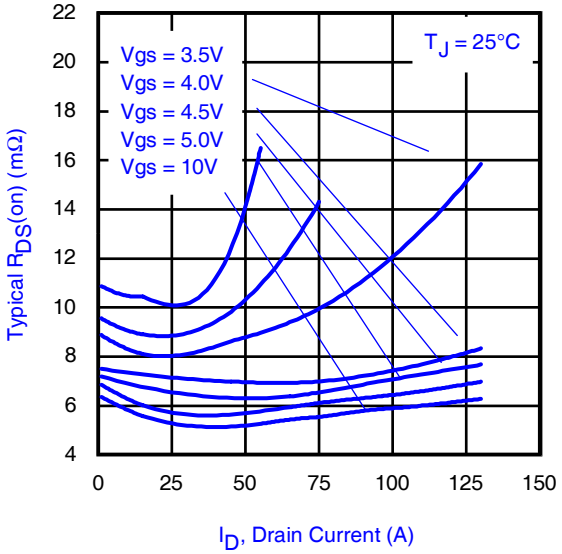


Fig 9. Typical On-Resistance vs. Drain Current and Gate Voltage

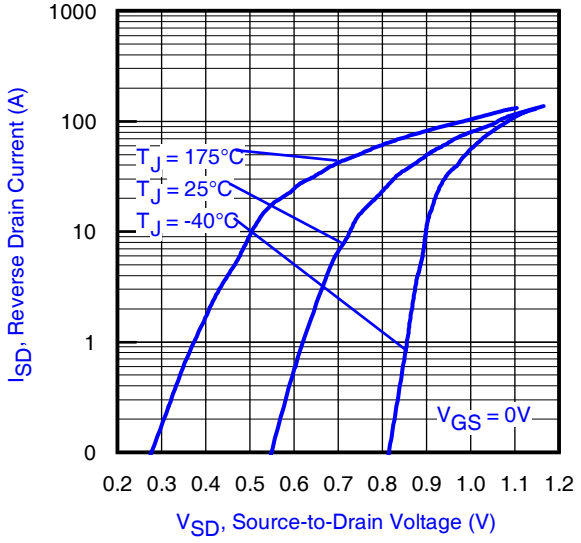


Fig 10. Typical Source-Drain Diode Forward Voltage

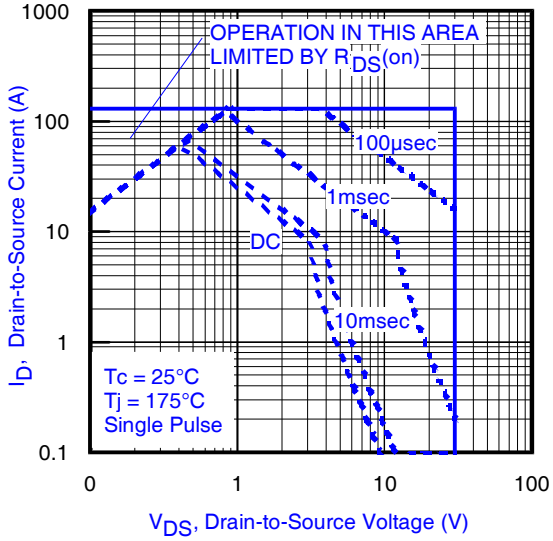


Fig 11. Maximum Safe Operating Area

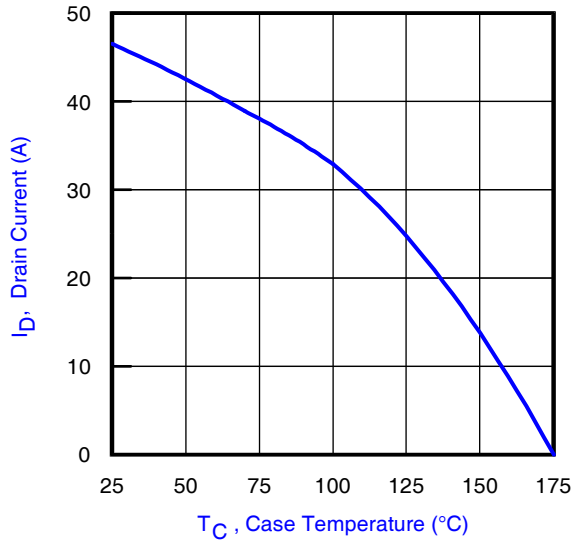


Fig 12. Maximum Drain Current vs. Case Temperature

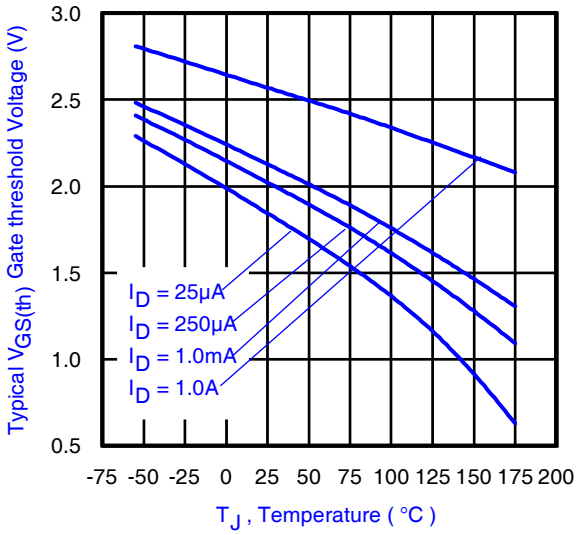


Fig 13. Typical Threshold Voltage vs. Junction Temperature

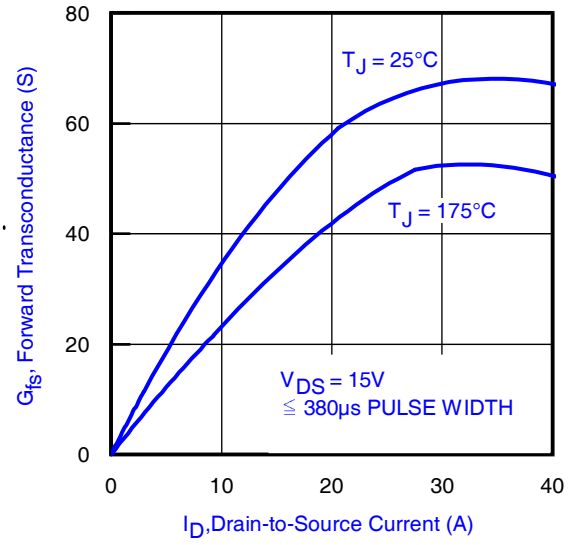


Fig 14. Typ. Forward Transconductance vs. Drain Current

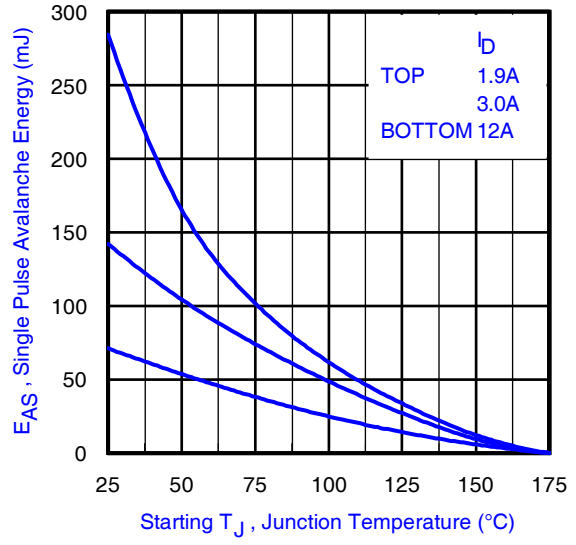


Fig 15. Maximum Avalanche Energy vs. Drain Current

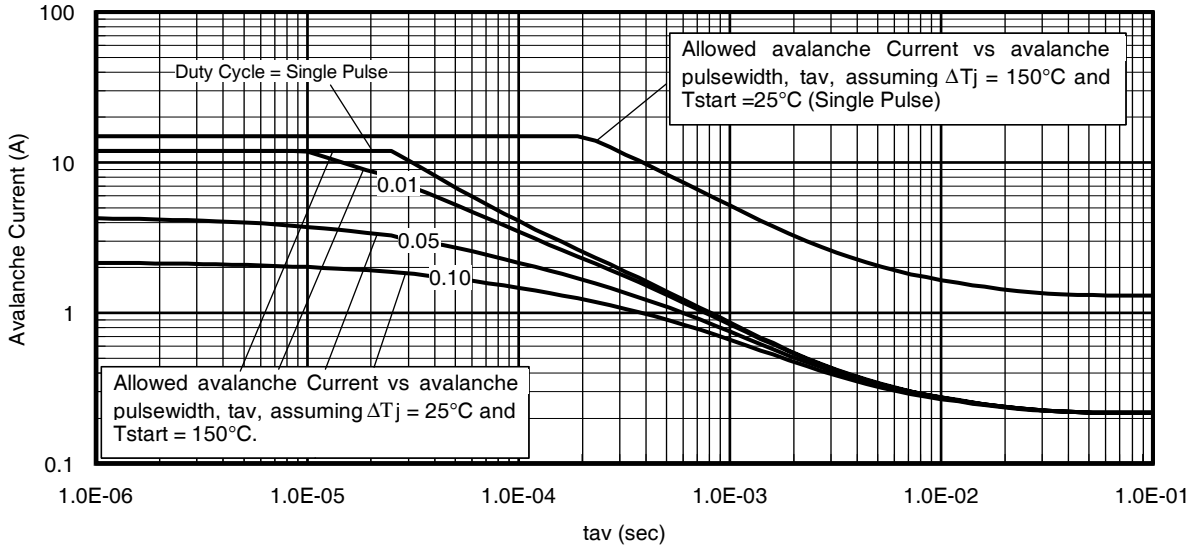


Fig 16. Typical Avalanche Current vs.Pulsewidth

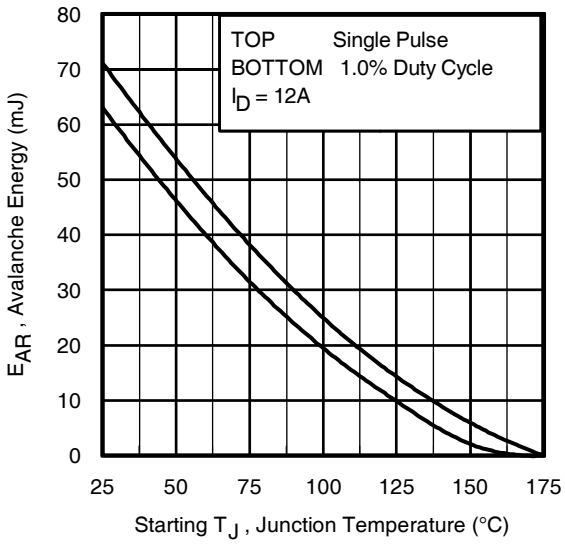


Fig 17. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 16, 17:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 19a, 19b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 16, 17).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

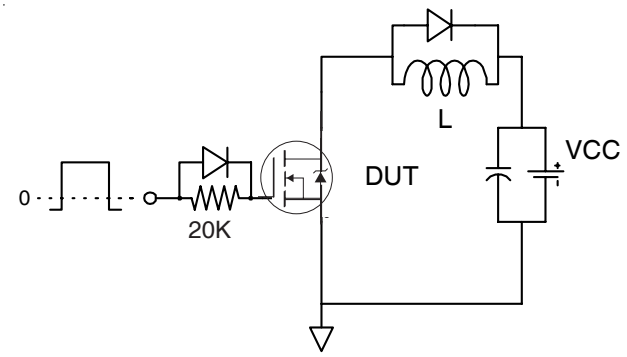


Fig 18a. Gate Charge Test Circuit

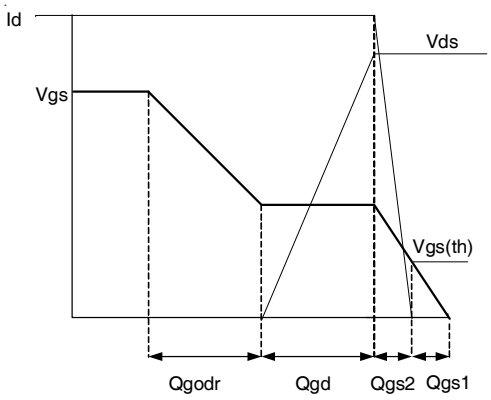


Fig 18b. Gate Charge Waveform

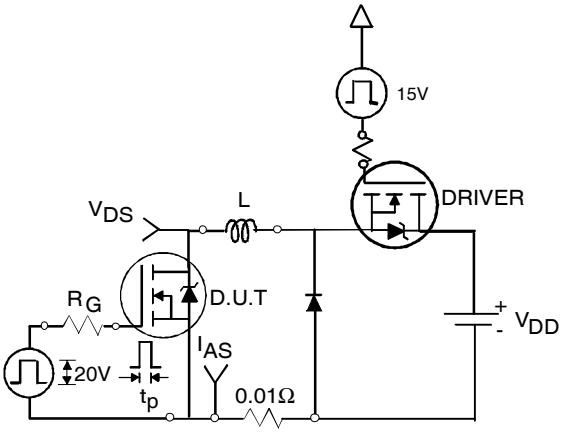


Fig 19a. Unclamped Inductive Test Circuit

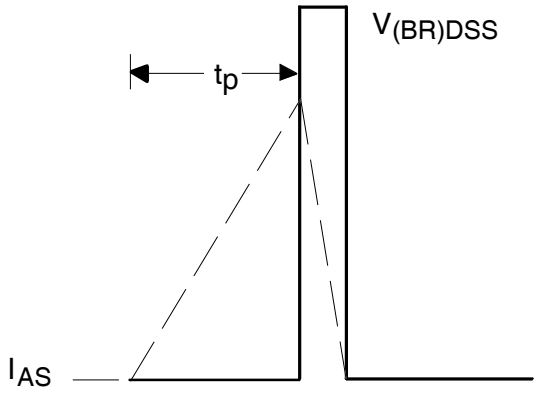


Fig 19b. Unclamped Inductive Waveforms

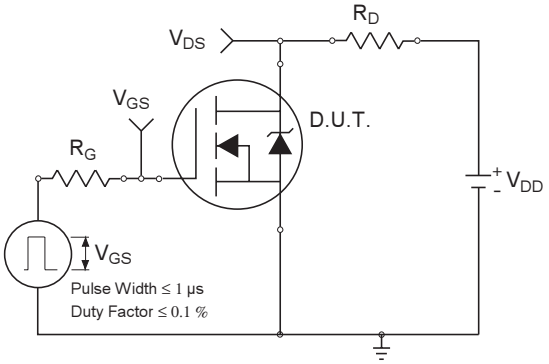


Fig 20a. Switching Time Test Circuit

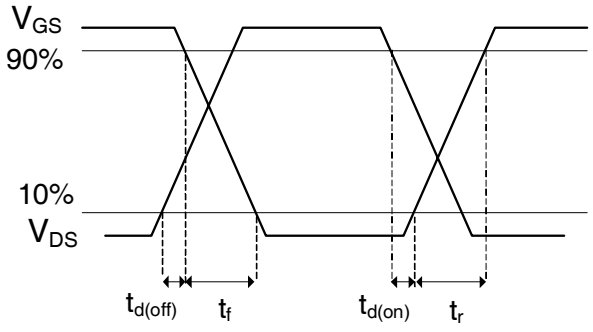


Fig 20b. Switching Time Waveforms

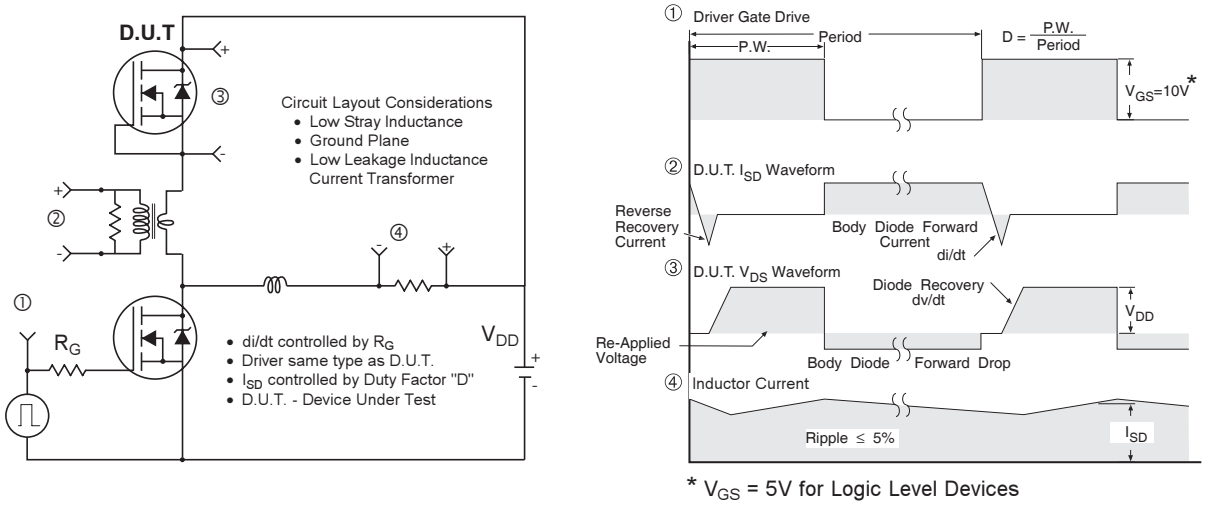
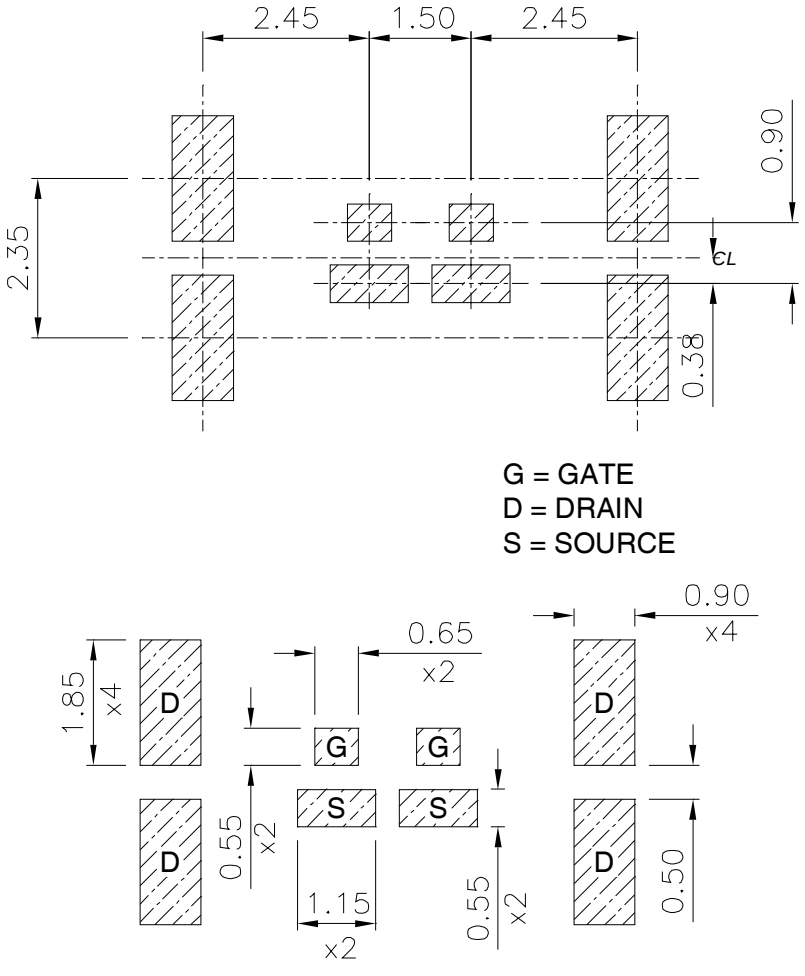


Fig 19. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

DirectFET™ Board Footprint, MA Outline (Medium Size Can).

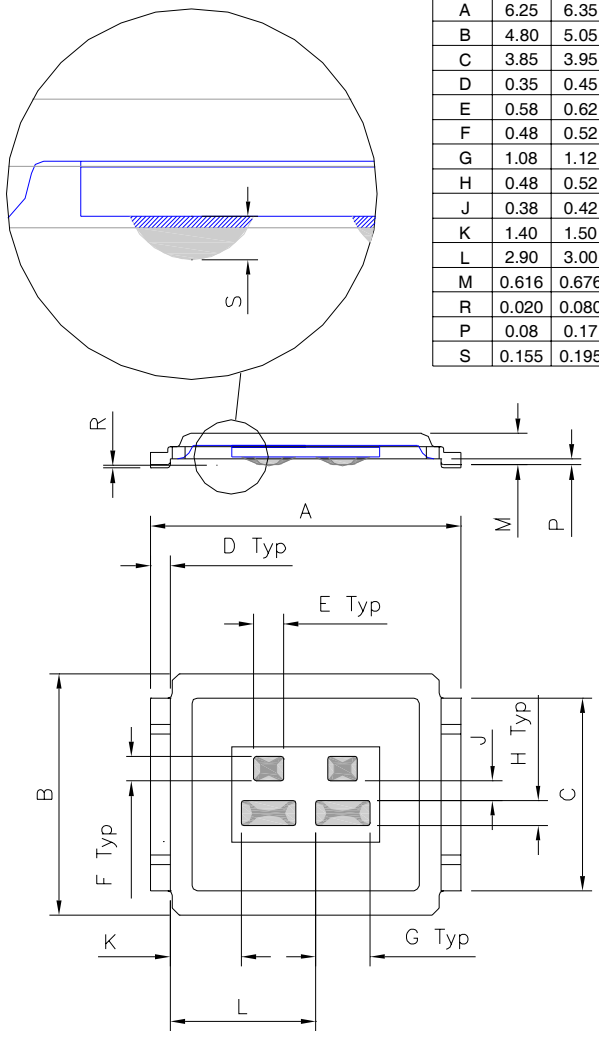
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



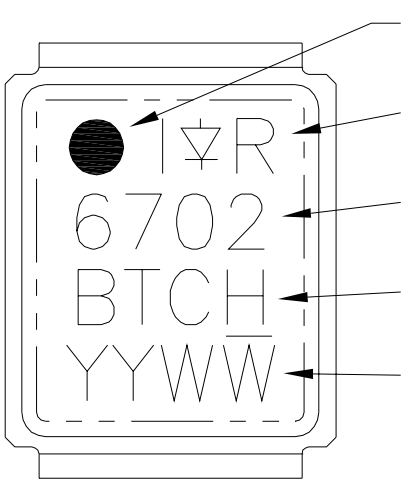
DirectFET™ Outline Dimension, MA Outline (Medium Size Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	0.48	0.52	0.019	0.020
G	1.08	1.12	0.043	0.044
H	0.48	0.52	0.019	0.020
J	0.38	0.42	0.015	0.017
K	1.40	1.50	0.055	0.059
L	2.90	3.00	0.114	0.118
M	0.616	0.676	0.0235	0.0274
R	0.020	0.080	0.0008	0.0031
P	0.08	0.17	0.003	0.007
S	0.155	0.195	0.006	0.008



DirectFET™ Part Marking



GATE MARKING

LOGO

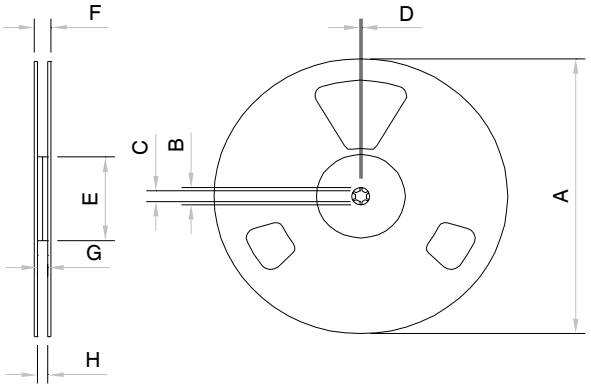
PART NUMBER

BATCH NUMBER

DATE CODE

Line above the last character of
the date code indicates "Lead-Free"

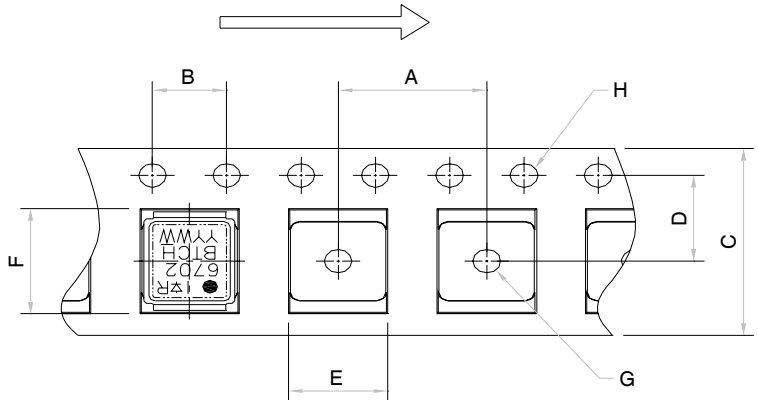
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6702M2DTRPBF). For 1000 parts on 7" reel, order IRF6702M2DTR1PBF

REEL DIMENSIONS								
STANDARD OPTION **(QTY 4800)**					TR1 OPTION **(QTY 1000)**			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.
This product has been designed and qualified to MSL1 rating for the Consumer market.
Additional storage requirement details for DirectFET products can be found in application note AN1035 on IR's Web site.
Qualification Standards can be found on IR's Web site.

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