



Ultra-Low Offset Voltage Operational Amplifier

T-79-06-10

OP-07**FEATURES**

- Low V_{OS} 25 μV Max.
- Low V_{OS} Drift 0.6 $\mu V/^{\circ}C$ Max.
- Very Stable 1.0 μV /Month Max.
- Replaces 725, 108A/308A, AD510
- Wide Input Voltage Range $\pm 14V$

APPLICATIONS

- High-Stability Instrumentation Amplifiers
- Precision Absolute Value Circuits
- Adjustment-Free Precision Summing Amplifiers

DESCRIPTION

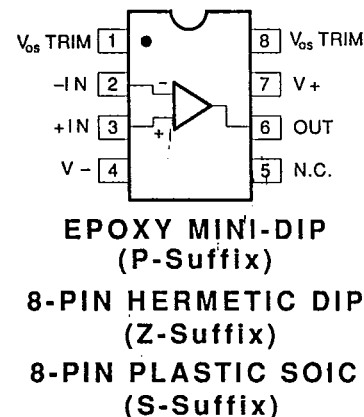
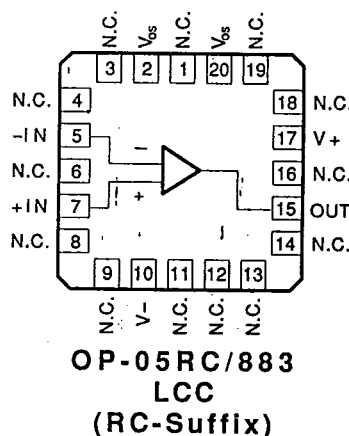
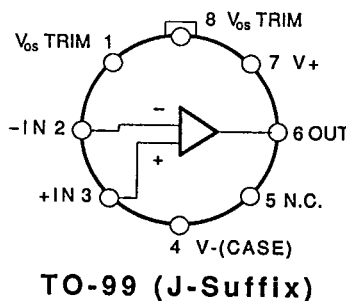
The OP-07 is a very low offset (25 μV max. for OP-07A), very low drift operational amplifier. Because of this low offset voltage, in many applications the OP-07 does not require external nulling. OP-07 also exhibits a very low input bias current ($\pm 2nA$ for OP-07A) and high gain (300,000). The OP-07 can be used as a direct replacement for 725 and 108A/308A (in TO-99 package) amplifiers, as well as for unnuled 741 amplifiers. Military temperature devices, OP-07 and OP-07A are available in TO-99 metal can and in 8-pin hermetic DIP packages. Commercial temperature range devices, OP-07C, OP-07D and OP-07E are also available in 8-pin plastic DIP packages.

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ $\Delta V_{OS} \text{ MAX}$ (μV)	PACKAGE					OPER. TEMP. RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	PLASTIC SOIC 8-PIN	LCC	
25	OP07AJ*	OP07AZ*				MIL
75	OP07EJ	OP07EZ	OP07EP	OP07ES		COM
75	OP07J*	OP07Z*			OP07RC/883	MIL
150	OP07CJ	OP07CZ	OP07CP	OP07CS		COM
150	OP07DJ		OP07DP	OP07DS		COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in.

Pin Connections (Top View)



OP-07

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, RC and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-07A, OP-07, OP-07RC	-55°C to +125°C
OP-07E, OP-07C, OP-07D	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
DICE Junction Temperature (T _j)	-65°C to +150°C

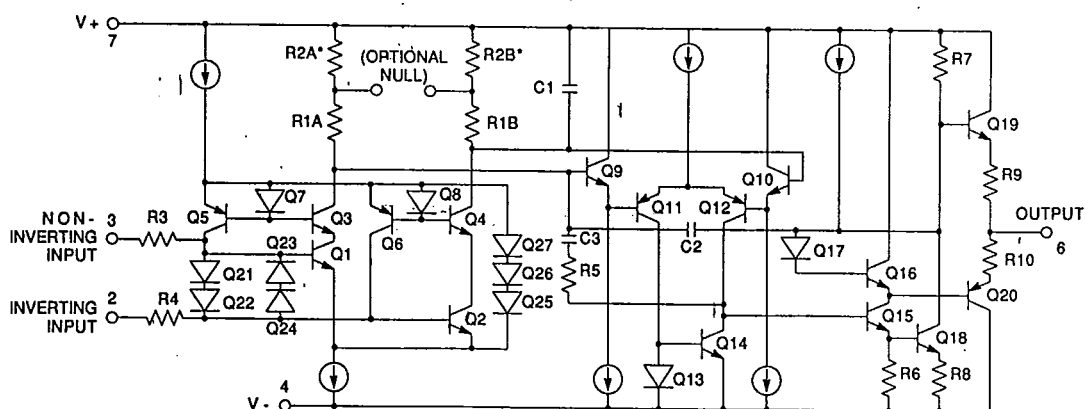
NOTES:

1. See table for maximum ambient temperature rating and derating factor.

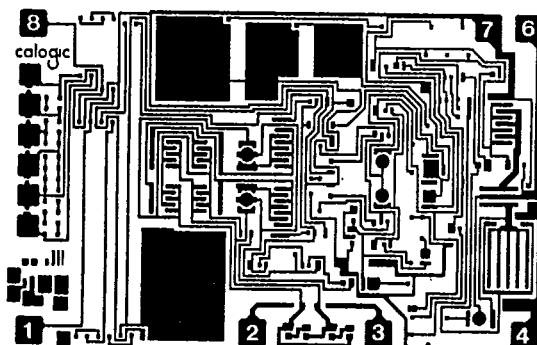
PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
LCC (RC)	72°C	7.8mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Simplified Schematic

*NOTE: R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

Die Characteristics

1. TRIM
2. (-) INPUT
3. (+) INPUT
4. V-
6. OUTPUT
7. V+
8. TRIM

DIE SIZE 0.099×0.066 inch, 6534 sq. mils
(2.515×1.676mm, 4.215 sq. mm)



OP-07

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	OP-07A TYP.	MAX.	MIN.	OP-07 TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	30	75	μV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 2)	—	0.2	1.0	—	0.2	1.0	mV
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	± 0.7	± 2.0	—	± 1.0	± 3.0	nA
Input Noise Voltage	e_{n-p-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 3)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		$f_O = 100\text{Hz}$ (Note 3)	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$ (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{n-p-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Note 3)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		$f_O = 100\text{Hz}$ (Note 3)	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$ (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance—Differential-Mode	R_{IN}	(Note 4)	30	80	—	20	60	—	M Ω
Input Resistance—Common-Mode	R_{INCM}		—	200	—	—	200	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 4) ¹	150	400	—	150	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.5	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 12.0	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.5	± 12.0	—	± 10.5	± 12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	75	120	—	75	120	mW
		$V_S = \pm 3V$, No load	—	4	6	—	4	6	
Offset Adjustment Range		$R_p = 20k\Omega$	—	± 4	—	—	± 4	—	mV

NOTES:

1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation.

Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ —refer to typical performance curves.

3. Sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	OP-07A TYP.	MAX.	MIN.	OP-07 TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	$\mu V/^\circ C$
		$R_p = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.3	1.3	
Input Offset Current	I_{OS}		—	0.8	4	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1	± 4	—	± 2	± 6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 12.6	—	± 12	± 12.6	—	V

NOTES:

1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.

2. Sample tested.
3. Guaranteed by design.



OP-07

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long-Term V_{OS} Stability	$V_{OS}/Time$	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	± 1.2	± 4.0	—	± 1.8	± 7.0	—	± 2.0	± 12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		$f_O = 1000Hz$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_O = 1000Hz$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance—Differential-Mode	R_{IN}	(Note 4)	15	50	—	8	33	—	7	31	—	$M\Omega$
Input Resistance—Common-Mode	R_{INCM}		—	160	—	—	120	—	—	120	—	$G\Omega$
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$	150	400	—	100	400	—	—	400	—	
		$V_S = \pm 3V$ (Note 3)	—	—	—	—	—	—	—	—	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.0	± 13.0	—	± 12.0	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 11.5	± 12.8	—	± 11.5	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.5	± 12.0	—	—	± 12.0	—	—	± 12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	$V/\mu s$
Closed-Loop Bandwidth	BW	$A_{VOL} = +1.0$ (Note 5)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	75	120	—	80	150	—	80	150	mW
		$V_S = \pm 3V$, No load	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	± 4	—	—	± 4	—	—	± 4	—	mV

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation.

Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ —refer to typical performance curves.

3. Sample tested.
4. Guaranteed by design.



OP07

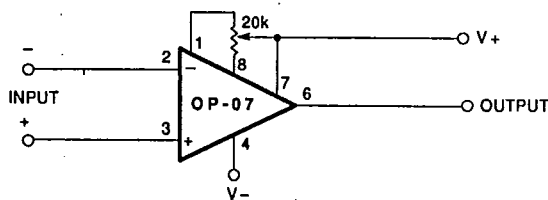
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	OP-07E TYP.	MAX.	MIN.	OP-07C TYP.	MAX.	MIN.	OP-07D TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 3)	—	0.3	1.3	—	0.5	1.8	—	0.7	2.5	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$ (Note 3)	—	0.3	1.3	—	0.4	1.6	—	0.7	2.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	—	12	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1.5	± 5.5	—	± 2.2	± 9.0	—	± 3.0	± 14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	—	18	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 12.6	—	± 11	± 12.6	—	± 11	± 12.6	—	V

NOTES:

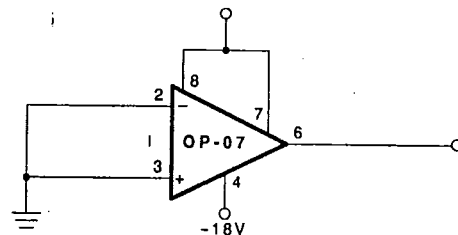
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

Optional Offset Nulling Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Burn-In Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES