

1.1 Scope.

This specification covers the detail requirements for a resolver-to-digital converter with up to 16 bits resolution and accuracies of 8 and 4 arc mins.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD2S80AS(X)/883B
-2	AD2S80AT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-40A	40-Lead Side Brazed Ceramic DIP
E	E-44A	44-Terminal Leadless Ceramic Chip Carrier

1.3 Absolute Maximum Ratings. ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

$+V_S$ to GND ¹		+14.0 V dc
$-V_S$ to GND ¹		-14.0 V dc
$+V_L$ to GND ¹		$+V_S$
Digital Input Voltage to GND ¹		-0.4 V to $+V_L$
Demod I/P		+14.0 V to $-V_S$
Integrator I/P		+14.0 V to $-V_S$
VCO Input		+14.0 V to $-V_S$
V_{REF} to GND ^{2, 3}		+14.0 V to $-V_S$
Analog Input Voltage (SIN, COS) to GND ^{2, 3}		+14.0 V to $-V_S$
Power Dissipation		860 mW
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range		-55°C to +125°C

NOTES

¹GND refers to ANALOG GND; ANALOG GND must be externally connected to DIGITAL GND.

²SIGNAL GND is internally connected to ANALOG GND.

³SIN, COS REF input voltage may be present without $+V_S$, $-V_S$, $+V_L$.

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Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Angular Accuracy ²		-1	±8	±8	±8	±8	+V _S = +10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc SC1 = SC2 = High 16 Bit Resolution	arc min max
							+V _S = +13.2 V dc, V _L = 5.0 V dc -V _S = -13.2 V dc SC1 = SC2 = High 16 Bit Resolution	
Angular Accuracy ²		-2	±4	±4	±4	±4	+V _S = +10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc SC1 = SC2 = High 16 Bit Resolution	arc min max
							+V _S = +13.2 V dc, V _L = 5.0 V dc -V _S = -13.2 V dc SC1 = SC2 = High 16 Bit Resolution	
Resolution	RES	-1, 2	16				10, 12, 14, 16 User Selectable	1 Bit in 16 1 in 65536
Missing Codes ²		-1, 2	4	4	4	4	+V _S = +10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc SC1 = SC2 = High 16 Bit Resolution	Codes max
							+V _S = +13.2 V dc, V _L = 5.0 V dc -V _S = -13.2 V dc SC1 = SC2 = High 16 Bit Resolution	
Signal and Reference Frequency		-1, 2	50 to 20,000					Hz
Total Effective Angular Offset		-1, 2	±800	±800	±800	±800	Output Data Nulled by Application of Offset Current to Integrator Input	nA max
Integrator Output Range		-1, 2	±8	±8	±8	±8	+V _S = +12.0 V dc, V _L = 5.0 V dc -V _S = -12.0 V dc 1 mA Load	V min
Integrator Output Range		-1, 2	±7	±7	±7	±7	+V _S = +10.8 V dc, V _L = 5.0 V dc -V _S = -10.8 V dc 1 mA Load	V min
Integrator Input Offset Voltage	V _{IO}	-1, 2	5					mV max
Integrator Dead Zone Current		-1, 2	110					nA/LSB max
Integrator Input Bias Current	I _{IB}	-1, 2	150					nA max
Integrator Input Impedance	Z _{IN}	-1, 2	1					MΩ min
Demod O/P Scaling		-1, 2	90	90	90	90		nA/Bit min
			110	110	110	110		nA/Bit max
PSD O/P Offset Voltage		-1, 2	12					mV max
PSD Input Bias Current	I _{IB}	-1, 2	150					nA max
PSD Input Impedance	Z _{IN}	-1, 2	1					MΩ min

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
VCO Maximum Rate		-1, 2	1.1	1	1	1		MHz min
VCO Rate Tempco		-1, 2	-0.05					%/°C
VCO Gain Scaling		-1, 2	7110	7110	7110	7110	Measured with VCO Input Current of $\pm 10 \mu\text{A}$	Hz/ μA min
			8690	8690	8690	8690		Hz/ μA max
VCO Input Bias Current	I_{IB}	-1, 2	380					nA max
VCO Input Bias Tempco		-1, 2	-1.22					nA/°C
VCO Linearity ⁴		-1, 2	± 3	± 3	± 3	± 3	VCO Measured at 10 Points over the Frequency Range 0-1 MHz	% max
VCO Total Effective Offset	I_{IO}	-1, 2	380	380	Sub 2 380 Sub 3 400	380	Measured with 68 k Ω Input Resistance	nA max
Tracking Rate Range		-1, 2	1074 268 67 16.7				Comment: 10 Bit RES 12 Bit RES 14 Bit RES 16 Bit RES	rps max (Revolutions per Second)
Reference Input Voltage		-1, 2	1	1				V Peak min
			8					V Peak max
Reference Input Impedance		-1, 2		1				M Ω min
Reference Input Bias Current		-1, 2	150					nA max
Signal Input Voltage (SIN, COS)		-1, 2	$2 \pm 10\%$					V rms
Signal Input Impedance		-1, 2	1					M Ω min
Signal Input Bias Current		-1, 2	150					nA max
Signal Input Phase Shift (wrt Reference)		-1, 2	± 10					Degrees max
Digital Inputs High Voltage	V_{IH}	-1, 2	2.0	2.0	2.0	2.0	DB1-DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT $+V_S = +10.8 \text{ V dc}$, $V_L = 5.0 \text{ V dc}$ $-V_S = -10.8 \text{ V dc}$	V min
Digital Inputs Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8	0.8	DB1-DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT $+V_S = +13.2 \text{ V dc}$, $V_L = 5.0 \text{ V dc}$ $-V_S = -13.2 \text{ V dc}$	V max
Digital Inputs High Current	I_{IH}	-1, 2	± 100	± 100	± 100	± 100	DB1-DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT $V_L = 5.5 \text{ V}$, $V_{IH} = 5.5 \text{ V}$ $+V_S = 13.2 \text{ V dc}$, $-V_S = -13.2 \text{ V dc}$	μA max
Digital Inputs Low Current	I_{IL}	-1, 2	± 100	± 100	± 100	± 100	DB1-DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT $V_L = 5.5 \text{ V}$, $V_{IL} = 0.0 \text{ V}$ $+V_S = 13.2 \text{ V dc}$, $-V_S = -13.2 \text{ V dc}$	μA max
Digital Inputs Low Voltage ³	V_{IL}	-1, 2	1.0	1.0	1.0	1.0	SC1, SC2, DATA LOAD, $+V_S = +12.0 \text{ V dc}$, $-V_S = -12.0 \text{ V}$ $V_L = 5.0 \text{ V}$, $\overline{\text{ENABLE}} = \text{High}$	V max
Digital Inputs Low Current ³	I_{IL}	-1, 2	400	400	400	400	SC1, SC2, DATA LOAD, $+V_S = +12.0 \text{ V dc}$, $-V_S = -12.0 \text{ V}$ $V_L = 5.0 \text{ V}$, $\overline{\text{ENABLE}} = \text{High}$	μA max

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Digital Outputs High Voltage	V _{OH}	-1, 2	2.4	2.4	2.4	2.4	DB1-DB16, RIPPLE CLOCK, DIRECTION +V _S = +12.0 V, V _L = 4.5 V -V _S = -12.0 V, I _{OH} = 100 µA	V min
Digital Outputs Low Voltage	V _{OL}	-1, 2	0.4	0.4	0.4	0.4	DB1-DB16, RIPPLE CLOCK, DIRECTION +V _S = +12.0 V dc, V _L = 5.5 V dc -V _S = -12.0 V, I _{OL} = 1.2 mA	V max
High Level Three State Leakage Current	I _{OZH}	-1, 2	±100	±100	±100	±100	DB1-DB16 Only +V _S = +12.0 V dc, V _L = 5.5 V dc -V _S = -12.0 V dc, V _{OL} = 5.0 V dc	µA max
Low Level Three State Leakage Current	I _{EZL}	-1, 2	±100	±100	±100	±100	DB1-DB16 Only +V _S = +12.0 V dc, V _L = 5.5 V dc -V _S = -12.0 V dc, V _{OL} = 0.0 V dc	µA max
Busy Pulse Width ²	t _{BUSY}	-1, 2	200	200	200	200		ns min
			600	600	600	600		ns max
Power Supply Current from +V _S from -V _S from +V _L	+I _S -I _S +I _L	-1, 2 -1, 2 -1, 2	30 -30 1.5	30 -30 1.5	30 -30 1.5	30 -30 1.5	+V _S = +13.2 V dc -V _S = -13.2 V dc +V _S = +5.5 V dc	mA max

NOTES

¹+V_S = +12.0 V dc, -V_S = -12.0 V dc, V_L = +5.0 V dc.

²V_{SIN}, V_{COS} = 2 V_{RMS} Maximum at 5 kHz. V_{REF} = 2 V_{RMS} at 5 kHz.

³Digital inputs SC1, SC2, DATA LOAD are internally pulled up to +V_S.

⁴VCO linearity is expressed as % (percentage) of reading.

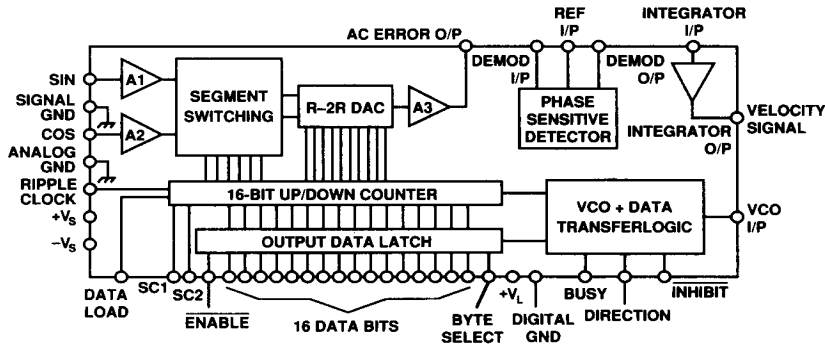
1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 11°C/W for D-40A

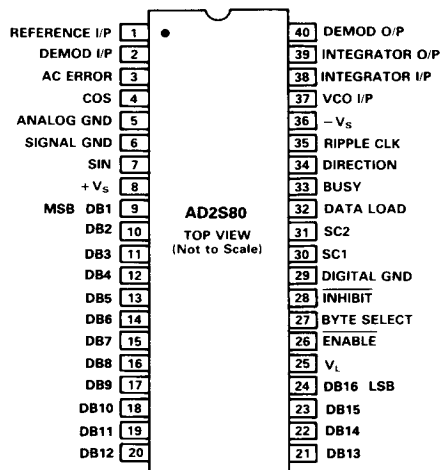
θ_{JC} = 10°C/W for E-44A

In accordance with Appendix C of MIL-M-38510.

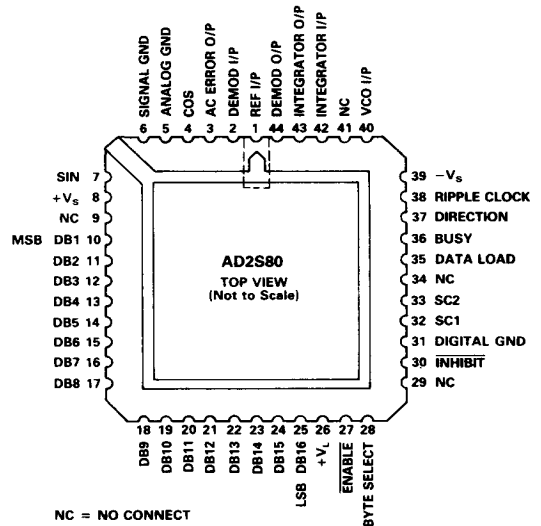
3.2.1 Functional Block Diagram and Terminal Assignments.



D Package (DIP)



E Package (LCC)



NC = NO CONNECT

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

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4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

