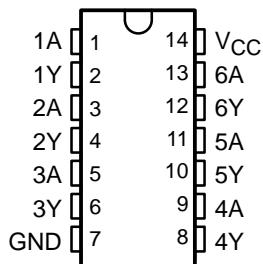
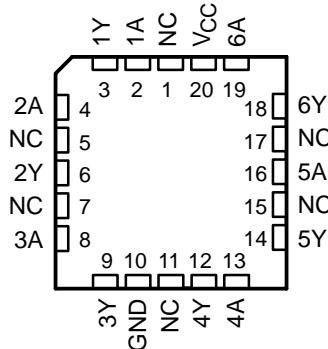


- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible

SN54HCT04 . . . J PACKAGE
SN74HCT04 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain six independent inverters. They perform the Boolean function $Y = \bar{A}$ in positive logic.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HCT04N	SN74HCT04N
		Tube of 50	SN74HCT04D	HCT04
		Reel of 2500	SN74HCT04DR	
		Reel of 250	SN74HCT04DT	
	SOP – NS	Reel of 2000	SN74HCT04NSR	HCT04
	TSSOP – PW	Tube of 90	SN74HCT04PW	HT04
		Reel of 2000	SN74HCT04PWR	
		Reel of 250	SN74HCT04PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT04J	SNJ54HCT04J
	LCCC – FK	Tube of 55	SNJ54HCT04FK	SNJ54HCT04FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



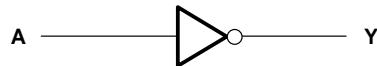
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HCT04, SN74HCT04 HEX INVERTERS

SCLS042D – JULY 1986 – REVISED JULY 2003

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 3)

			SN54HCT04			SN74HCT04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise/fall time				500			500	ns
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCRA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT04	SN74HCT04	UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	4.5 V	4.4	4.499		4.4	4.4	V
			3.98	4.3		3.7	3.84	
V _{OL}	V _I = V _{IH} or V _{IL}	4.5 V		0.001	0.1	0.1	0.1	V
				0.17	0.26	0.4	0.33	
I _I	V _I = V _{CC} or 0	5.5 V		±0.1	±100	±1000	±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	5.5 V			2	40	20	µA
ΔI _{CC} [†]	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5 V		1.4	2.4	3	2.9	mA
C _i		4.5 V to 5.5 V		3	10	10	10	pF

[†]This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT04	SN74HCT04	UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	4.5 V		14	20	30	25	ns
			5.5 V		13	18	27	23	
t _t		Y	4.5 V		9	15	22	19	ns
			5.5 V		8	14	20	17	

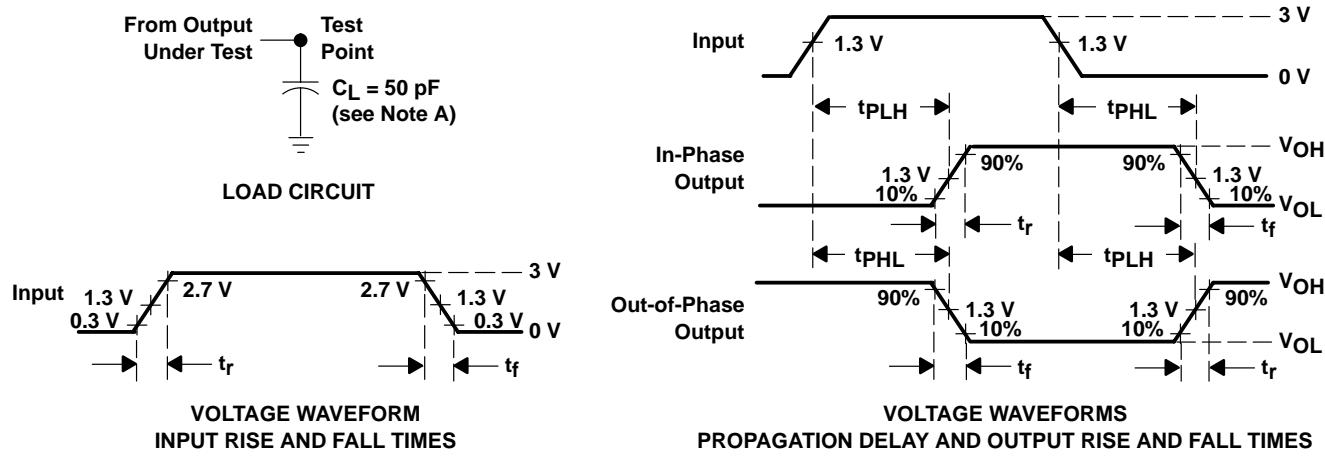
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per inverter	No load	20	pF

SN54HCT04, SN74HCT04 HEX INVERTERS

SCLS042D – JULY 1986 – REVISED JULY 2003

PARAMETER MEASUREMENT INFORMATION



NOTES:

- C_L includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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Microcontrollers	microcontroller.ti.com
Low Power Wireless	www.ti.com/lpw
	Audio www.ti.com/audio
	Automotive www.ti.com/automotive
	Broadband www.ti.com/broadband
	Digital Control www.ti.com/digitalcontrol
	Military www.ti.com/military
	Optical Networking www.ti.com/opticalnetwork
	Security www.ti.com/security
	Telephony www.ti.com/telephony
	Video & Imaging www.ti.com/video
	Wireless www.ti.com/wireless

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-89747012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8974701CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-8974701VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-8974701VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/65751BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN54HCT04J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74HCT04APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74HCT04D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HCT04NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HCT04NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74HCT04PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74HCT04PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT04PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HCT04FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HCT04J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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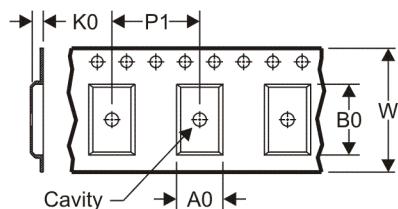
OTHER QUALIFIED VERSIONS OF SN54HCT04, SN54HCT04-SP, SN74HCT04 :

- Automotive: [SN74HCT04-Q1](#)
- Enhanced Product: [SN74HCT04-EP](#)

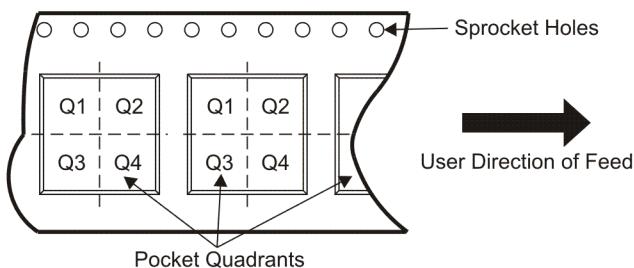
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT04NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HCT04PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



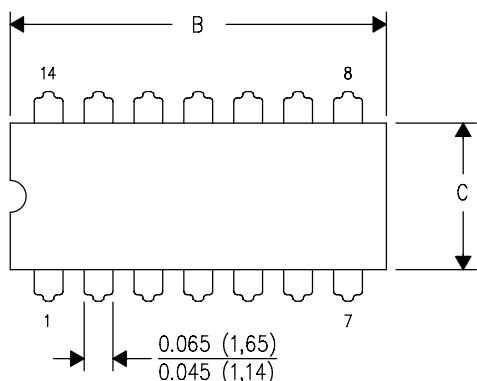
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT04DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74HCT04DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HCT04NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74HCT04PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



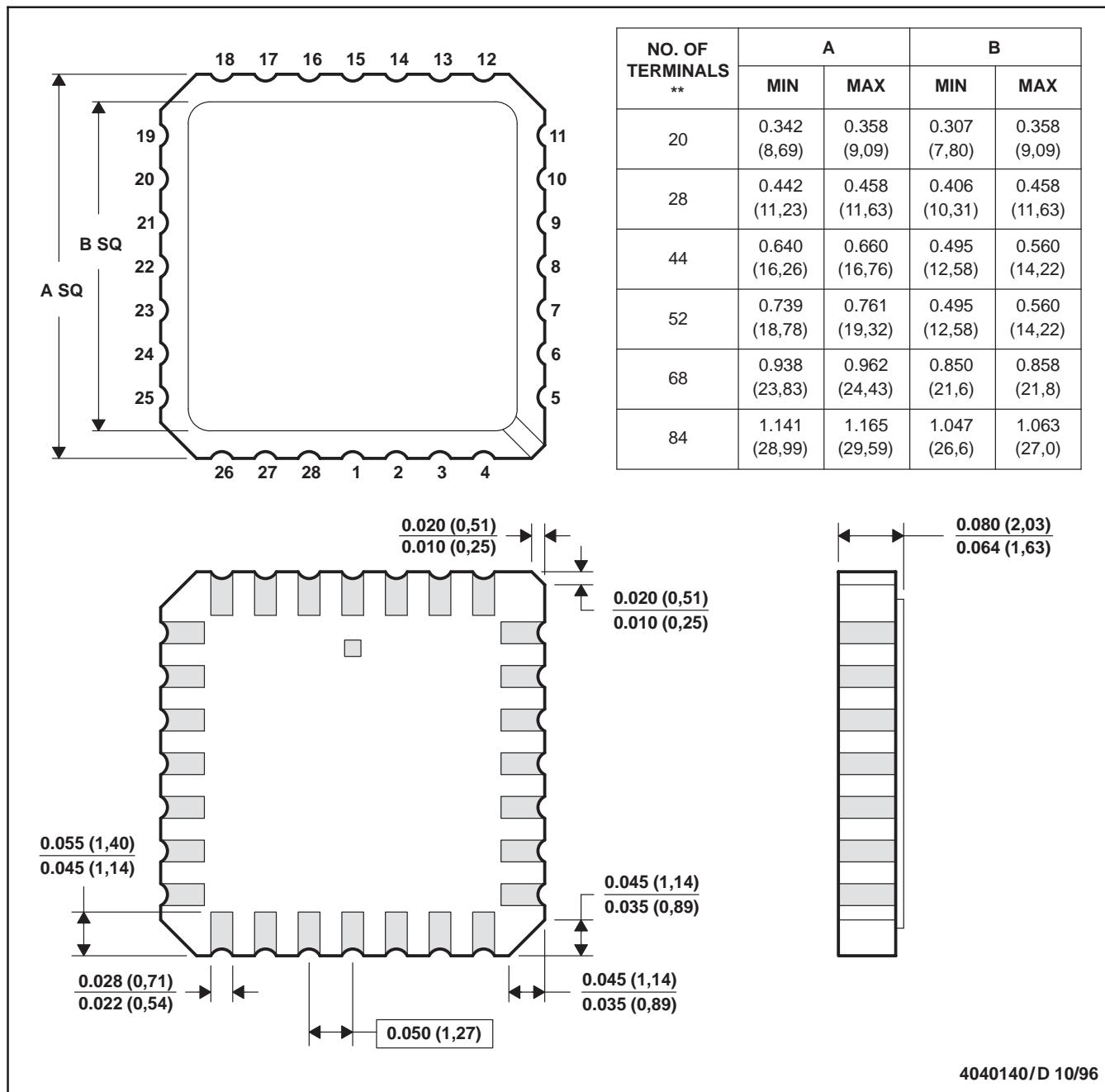
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. The terminals are gold plated.

E. Falls within JEDEC MS-004

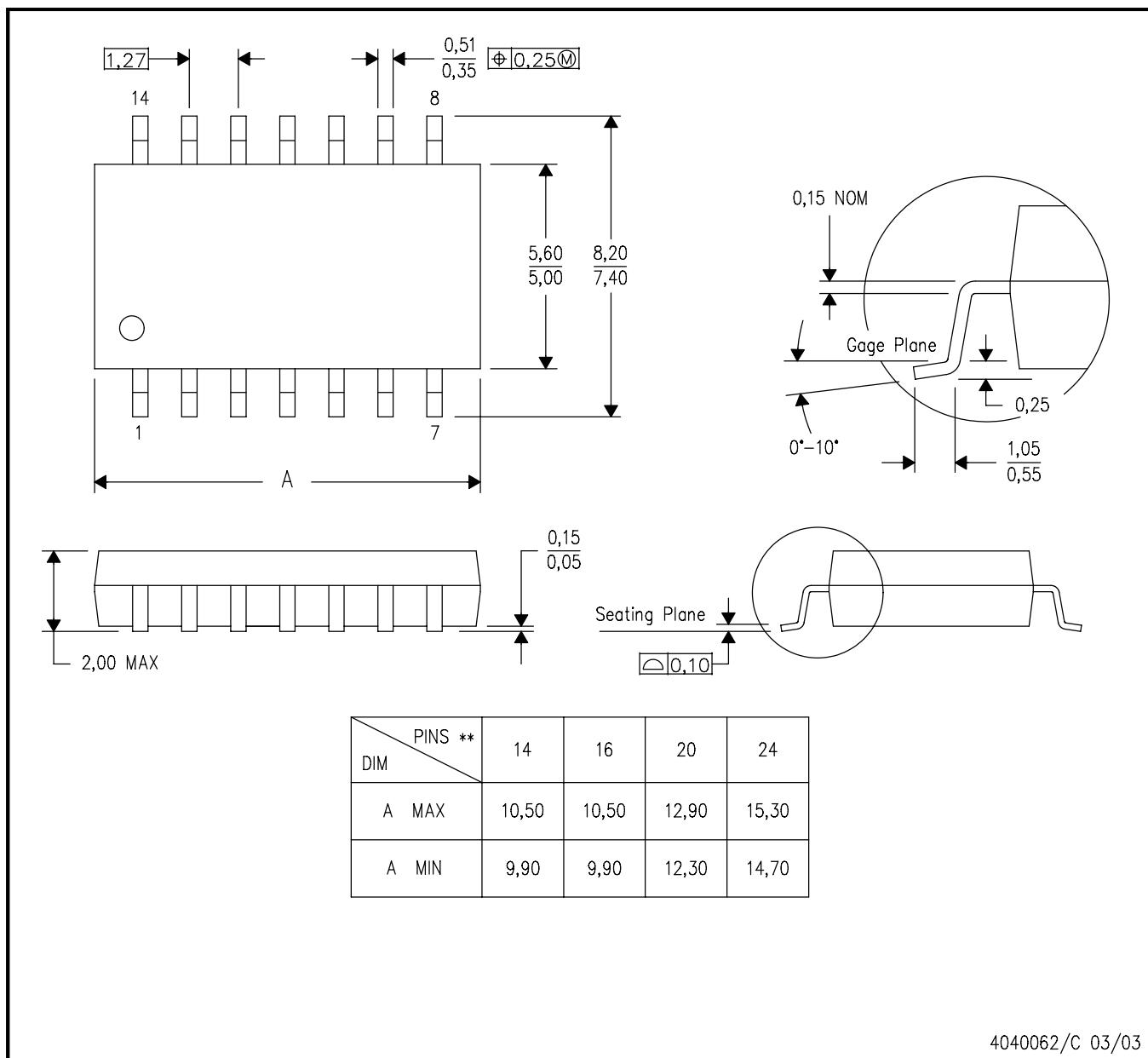
4040140/D 10/96

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

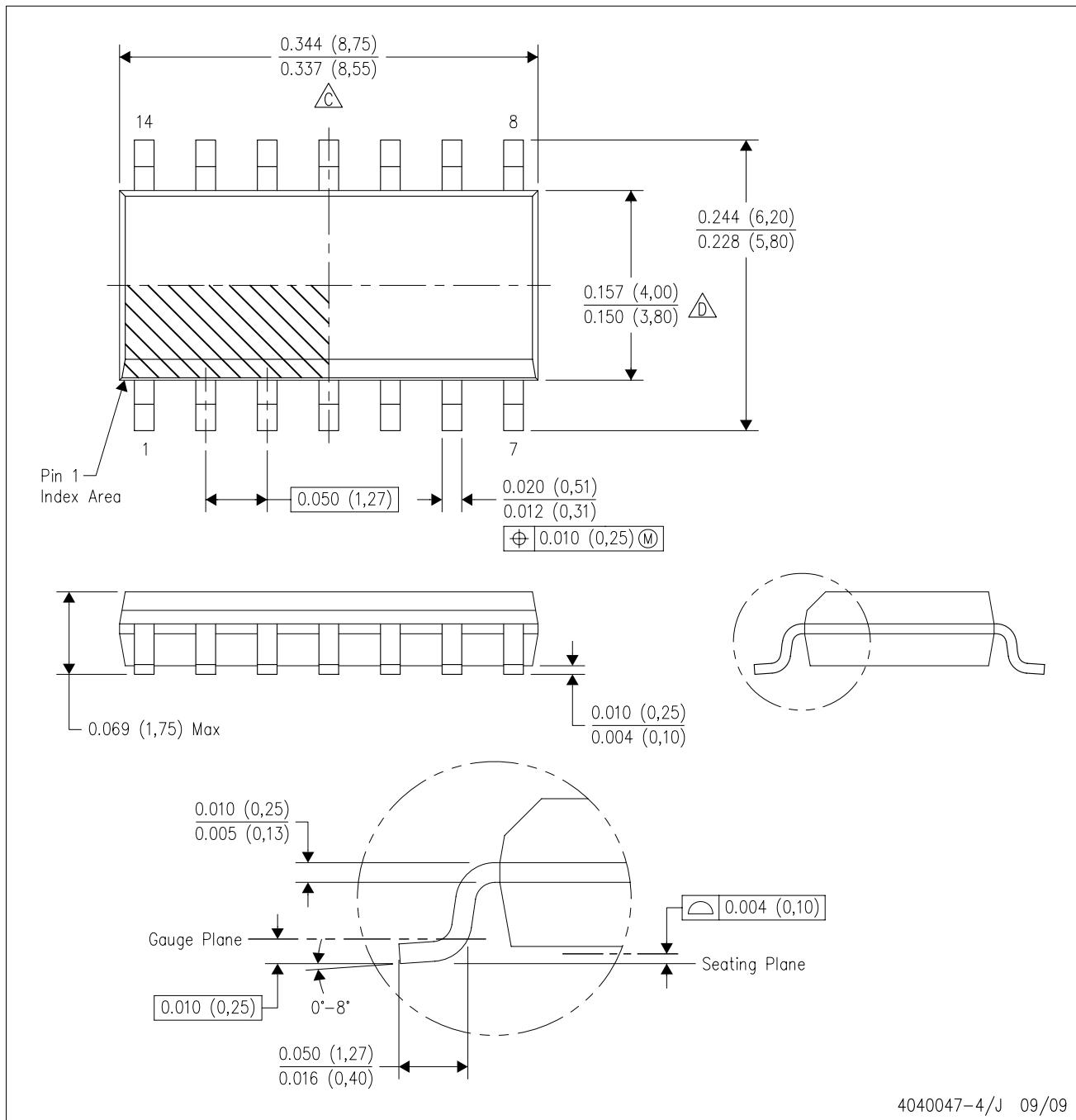


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

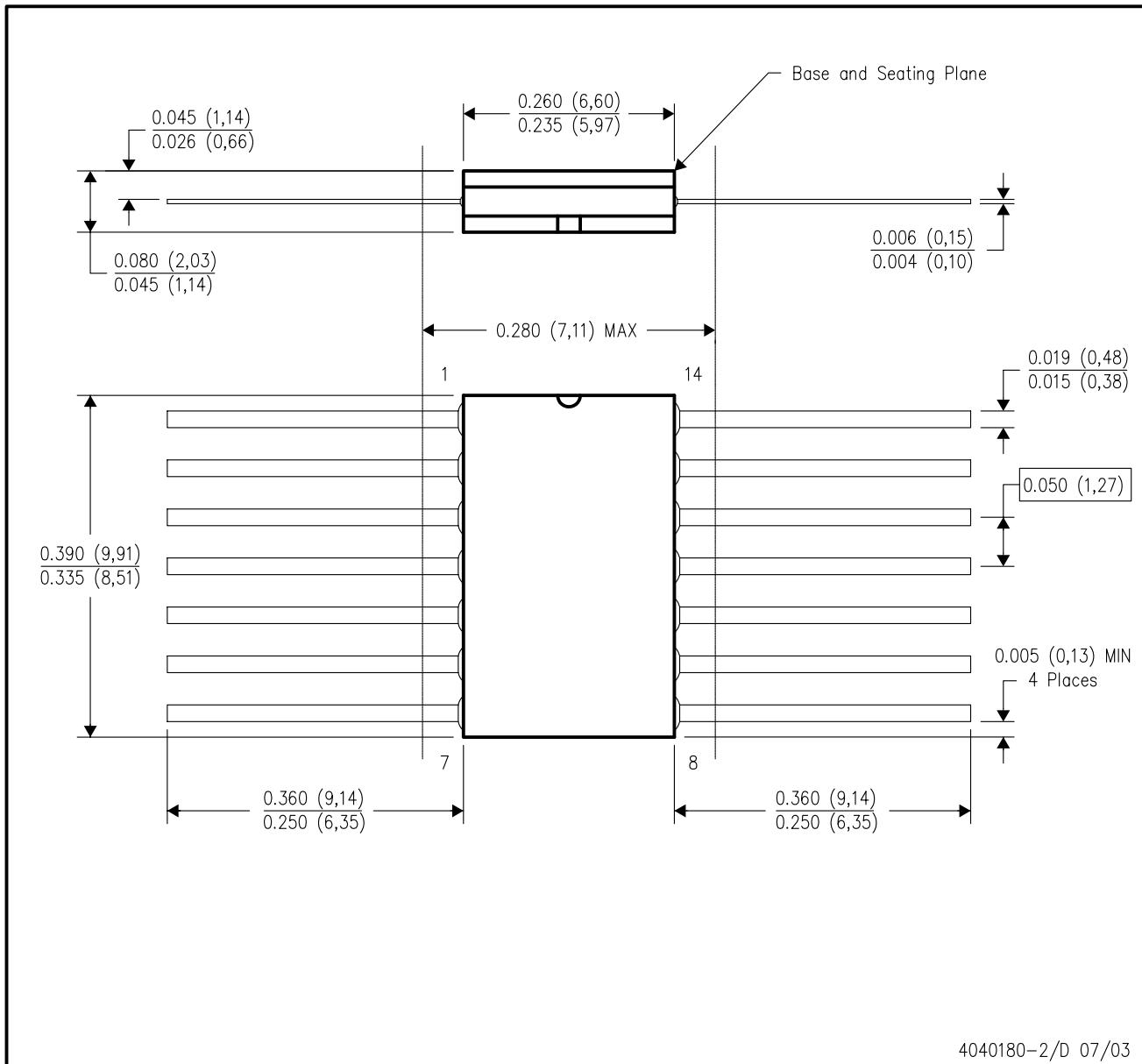
Symbol C: Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Symbol D: Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/D 07/03

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

