GS1678 Dual-Slew-Rate, Cable Driver with HD/SD Capability

The GS1678 is a high-speed BiCMOS integrated circuit designed to drive one or two 75Ω coaxial cables. The GS1678 can drive data rates up to 1.485Gb/s, and provides two selectable slew rates in order to achieve compliance to SMPTE 292M, SMPTE 259M and SMPTE 344M.

The GS1678 accepts industry-standard differential input levels, including LVPECL and CML. The $\overline{\text{DISABLE}}$ pin powers-down the output driver, leaving the serial data output in a high-impedance state. The GS1678 features an adjustable output swing using an external bias resistor. The single-ended output swing is adjustable from 600mVpp to 1200mVpp. The GS1678 can be powered from either a 3.3V or a 2.5V supply. Power consumption is typically 110mW using a 2.5V power supply.

The GS1678 is footprint and drop-in compatible with existing GS1578A and LMH0002 designs, with no additional application changes required.

Key Features

- Pin-compatible with and replaces the LMH0002
- SMPTE 292M, SMPTE 259M and SMPTE 344M compliant
- Supports data rates from 270Mb/s to 1.485Gb/s
- Supports DVB-ASI at 270Mb/s
- Wide common-mode range input buffer
  - 100mV sensitivity
  - Supports DC-coupling to industry-standard differential logic
  - on-chip 100Ω differential data input termination
- Differential coaxial-cable-driving outputs

- selectable slew rates
- adjustable output swing from 600mVpp to 1200mVpp
- $\overline{\text{DISABLE}}$ control
- Robust output signal presence function
- Excellent output eye quality
- Power supply operation at 3.3V or 2.5V
- 110mW power consumption (2.5V supply)
- Operating temperature range: -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
- Drop-in compatible with the GS1578A
- Pb-free and RoHS compliant

Typical Application Circuit
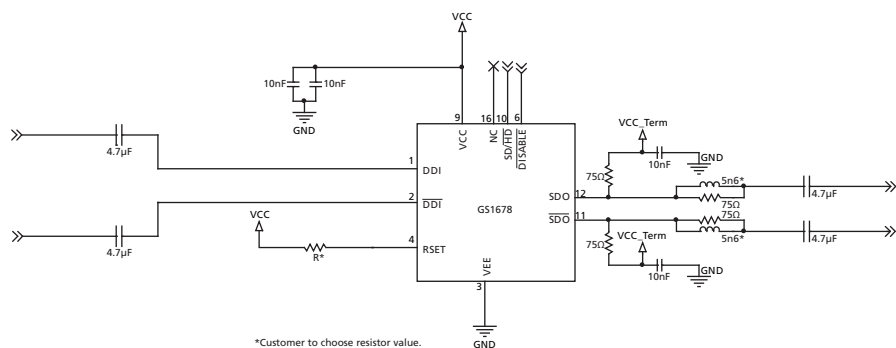
*Customer to choose resistor value.

NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise stated.

*Typical value: varies with layout, and represents a trade-off between good eye shape and output return loss.
5.6nF is the optimum value for an 800mV output swing.
6.8nF is the optimum value for an 1200mV output swing.

Contents

1. Pin Out

1.1 Pin Assignment

Figure 1-1: 16-Pin QFN

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
1, 2	DDI, $\overline{DDI}$	Input	Serial digital differential input.
3	VEE	Power	Most negative power supply connection for the input buffer and core. Connect to GND.
4	RSET	Input	External output amplitude control resistor connection.
5, 7, 8, 13, 14, 15, 16	N/C	–	No Connect. These pins are not connected internally.
6	$\overline{DISABLE}$	Input	Control signal input. When set LOW, the serial digital output is disabled (powered-down) and the SDO/$\overline{SDO}$ pins are set to high-impedance. When set HIGH, the SDO/$\overline{SDO}$ pins will output a serial digital signal. **NOTE:** if this pin is left floating, the serial digital output will be **enabled**.
9	VCC	Power	Most positive power supply connection. Connect to 3.3V or 2.5V.

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
10	SD/$\overline{\text{HD}}$	Input	Control signal input.
			When set HIGH, the serial digital output will meet the SMPTE 259M rise/fall time specification.
			When set LOW, the serial output will meet the SMPTE 292M rise/fall time specification.
			NOTE: if this pin is left floating, the serial digital output will meet the SMPTE 259M rise/fall time specification.
11, 12	$\overline{\text{SDO}}$/ SDO	Output	Serial digital differential output.
–	Center Pad	Power	Connect to most negative power supply plane following the recommendations in Recommended PCB Footprint on page 13.

For 3G migration, pins 14 and 16 are output signal and input select pins respectively.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	2.5kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	3.3V Typical	3.135	3.3	3.465	V	–
		2.5V Typical	2.375	2.5	2.625	V	–
Power Consumption (2.5V)	P_D	SDO/$\overline{SDO}$ enabled	–	110	130	mW	1
		SDO/$\overline{SDO}$ disabled	–	3	5	mW	1
Power Consumption (3.3V)		SDO/$\overline{SDO}$ enabled	–	155	183	mW	1
		SDO/$\overline{SDO}$ disabled	–	4	6	mW	1
Supply Current	I_S	VCC = 3.3V	–	47	53	mA	1
		VCC = 2.5V	–	44	50	mA	1
		Power-down	–	1	1.8	mA	1
Output Voltage	V_{CMOUT}	Common mode	–	V_{CC} - V_{OUT}	–	V	–
Input Voltage	V_{CMIN}	Common mode	1.4 + ΔV_{DDI}/2	–	V_{CC} - ΔV_{DDI}/2	V	–
SD/$\overline{HD}$, $\overline{DISABLE}$ Input	V_{IH}	I_{IH} <= 150µA	1.7	–	–	V	–
	V_{IL}	I_{IL} <= 150µA	–	–	0.8	V	–

NOTES:

1. Power consumed in GS1678 only. Termination resistors draw extra current.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	.27	–	1.485	Gb/s	1
Additive jitter	–	1.485Gb/s	–	20	–	ps_{p-p}	–
	–	270Mb/s	–	16	–	ps_{p-p}	–
Rise/Fall time	t_r, t_f	SD/$\overline{HD}$=0	–	–	135	ps	2
	t_r, t_f	SD/$\overline{HD}$=1	400	–	800	ps	2
Mismatch in rise/fall time	$\triangle t_r$, $\triangle t_f$	HD mode only	–	–	35	ps	–
Duty cycle distortion	–	SD/$\overline{HD}$=0	–	–	20	ps	3, 4
	–	SD/$\overline{HD}$=1	–	–	50	ps	3, 4
Overshoot	–	SD/$\overline{HD}$=0,	–	–	10	%	3
Output Return Loss	ORL	5 MHz – 1.485GHz	17	19	–	dB	5
Output Voltage Swing	V_{OUT}	R_{SET} = 750Ω	750	800	850	mV_{p-p}	3
Input Voltage Swing	$\triangle V_{DDI}$	Guaranteed functional.	100	–	250	mV_{p-pd}	–
		Guaranteed to meet all published specifications.	250		2200	mV_{p-pd}	–
Output Enable Delay	–	–	–	–	100	ns	–
Output Disable Delay	–	–	–	–	80	ns	–

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Rise/Fall time measured between 20% and 80%.
3. Single-ended into 75Ω external load.
4. Calculated as the actual positive bit-width compared to the expected positive bit-width using a 1010 pattern.
5. ORL depends on board design. The GS1678 achieves this specification on Gennum's evaluation boards.
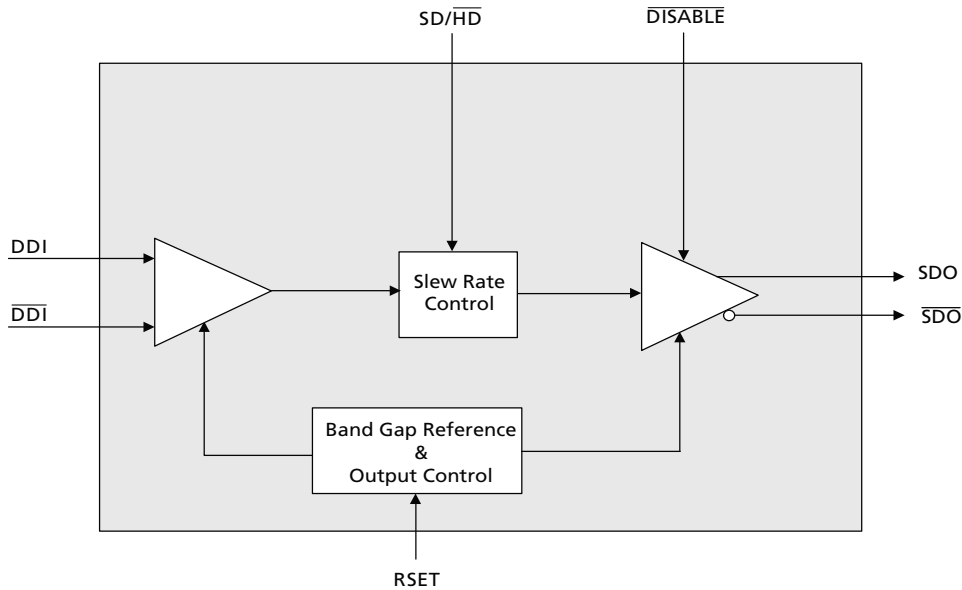
3. Detailed Description

Figure 3-1: GS1678 Functional Block Diagram

3.1 Serial Data Input

The GS1678 features a differential input buffer with on-chip 100Ω differential termination.

The serial data input signal is connected to the DDI and $\overline{DDI}$ input pins of the device.

Input signals can be single-ended or differential, DC or AC-coupled.

The serial digital input buffer is capable of operation with any binary coded signal that meets the input signal level requirements, in the range of 270Mb/s to 1.485Gb/s.

The input circuit is self-biasing to allow for simple AC or DC-coupling of input signals to the device.

3.2 Serial Data Output

The GS1678 features a current-mode differential output driver capable of driving up to 1200mVpp single-ended into a 1m length of 75Ω cable terminated at both ends.

The output signal amplitude or swing is user configurable using an external RSET resistor.

The SDO/$\overline{SDO}$ pin of the device provide the serial digital output.

3.2.1 Slew Rate Selection (Rise/Fall Time Requirement)

The GS1678 supports two user-selectable output slew rates.

Control of the slew rate is determined by the setting of the SD/$\overline{HD}$ input pin.

Table 3-1: Slew Rate Selection

SD/$\overline{\text{HD}}$	Rise/Fall Time
0	SMPTE 292M compliant
1	SMPTE 259M compliant
Floating	SMPTE 259M compliant

3.3 Output Disable

The GS1678 supports an output disable function for the serial digital differential output.

Control of this function is determined by the setting of the $\overline{\text{DISABLE}}$ control pin.

The serial output disable ($\overline{\text{DISABLE}}$), disables power to the current mode serial digital output driver. When asserted LOW, the SDO/$\overline{\text{SDO}}$ output driver is powered-down.

Table 3-2: Output Disable

$\overline{\text{DISABLE}}$	SDO/$\overline{\text{SDO}}$
0	All Chip Power Down
1	Operational
Floating	Operational

3.4 Output Amplitude (RSET)

The output amplitude of the GS1678 can be adjusted by changing the value of the RSET resistor as shown in Figure 3-2. For an 800mV$_{\text{p-p}}$ output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The RSET resistor is part of the high-speed output circuit of the GS1678. The resistor should be placed as close as possible to the RSET pin, and connected directly to the VCC plane (traces/wires may cause instability). In addition, the PCB capacitance should be minimized at this node by removing the PCB ground plane beneath the RSET resistor and the RSET pin.

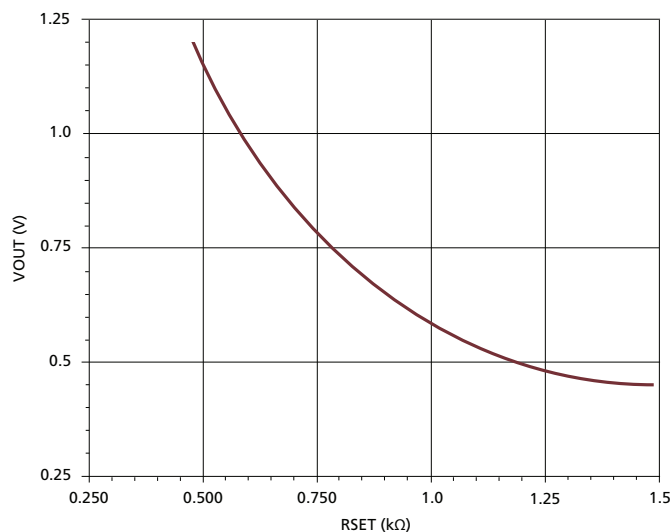NOTE: Care should be taken when considering layout of the RSET resistor. Please refer to Section 4.1 for more details.

Figure 3-2: V_{OUT} vs. RSET

Table 3-3: Typical RSET Values

RSET (Ω)	Output Swing (mV)
500	1200*
750	800
1000	600

*NOTE: In order to generate output swings greater than 1040mV, VCC_TERM must be connected to a 5V supply.

3.5 Output Return Loss (ORL) Measurement

The GS1678 includes a feature which allows users to measure ORL reliably while the device is still powered. The device can be put into a BALANCE mode which prevents the outputs from toggling while the device is powered on, allowing the ORL to be measured while the device is still powered.

When SD/$\overline{\text{HD}}$ is HIGH, the device goes into BALANCE mode. This mode is used during ORL measurement, disabling the AC signal path of the device without powering it down. When in BALANCE mode, the device produces equal pull-down currents in both differential shoulders of both serial digital differential outputs, effectively stopping all outputs at the output common mode voltage level. Gennum recommends using BALANCE mode when measuring ORL with 2.5V termination voltage.

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4. Application Information

4.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance

- The PCB ground plane is removed under the GS1678 output components to minimize parasitic capacitance (NOTE: care should be taken, as removing too much of the plane will make the system susceptible to EMI)

- The PCB ground plane is removed under the GS1678 RSET pin and resistor to minimize parasitic capacitance. The RSET resistor should be directly connected to the VCC plane

- High-speed traces are curved to minimize impedance variations due to change of PCB trace width
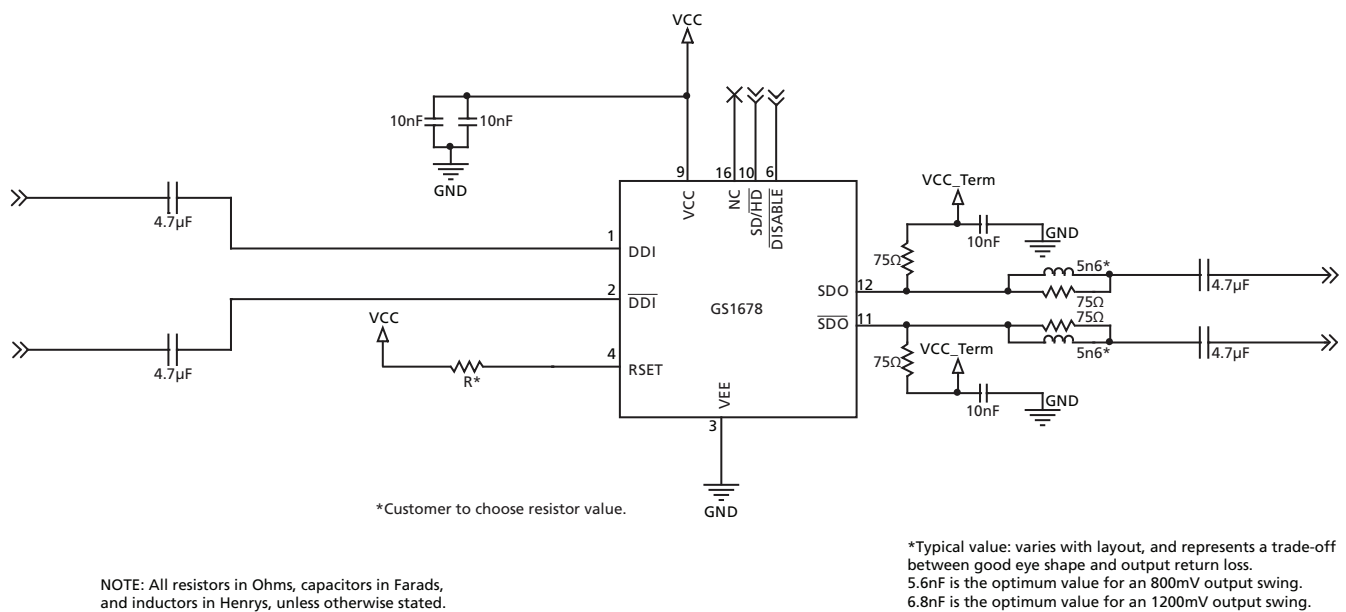
4.2 Typical Application Circuit

*Customer to choose resistor value.

NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise stated.

*Typical value: varies with layout, and represents a trade-off between good eye shape and output return loss.
5.6nF is the optimum value for an 800mV output swing.
6.8nF is the optimum value for an 1200mV output swing.

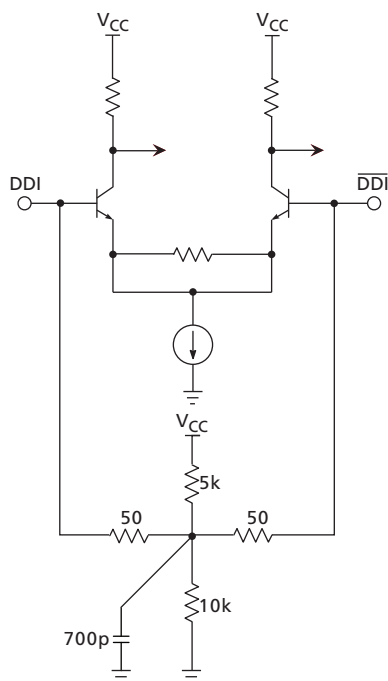Figure 4-1: Typical Application Circuit

5. Input/Output Circuits

Figure 5-1: Differential Input Stage (DDI/$\overline{DDI}$)
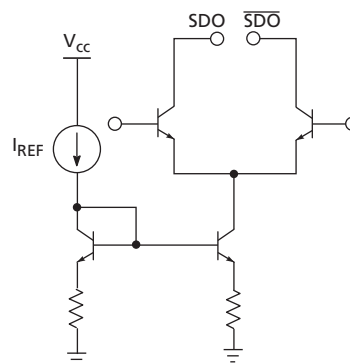
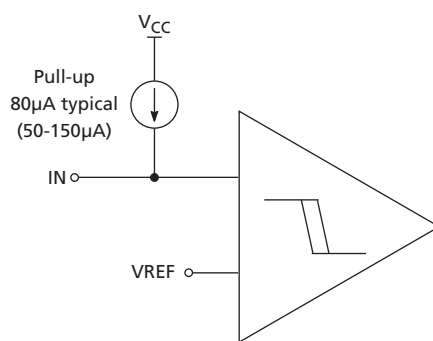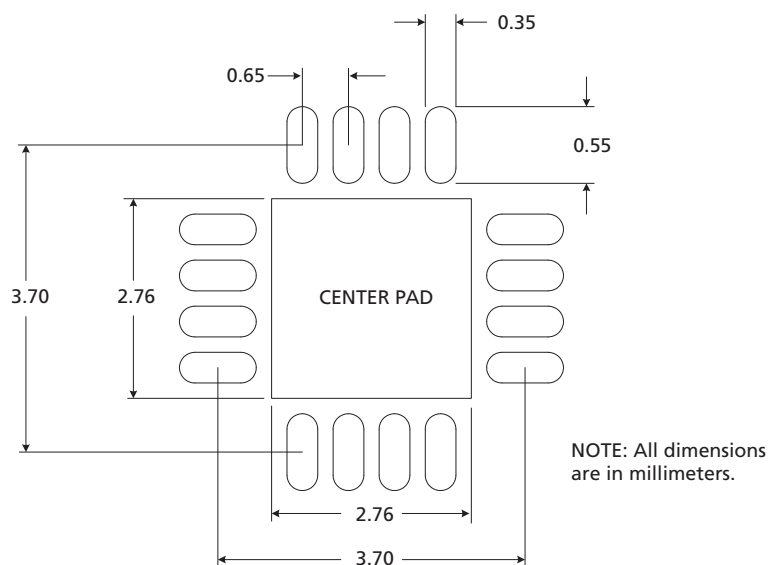Figure 5-2: Differential Output Stage (SDO/$\overline{SDO}$)

Figure 5-3: Control Input ($\overline{DISABLE}$, SD/$\overline{HD}$)

6. Package & Ordering Information

6.1 Package Dimensions

4.00+/-0.05   A

B

PIN 1 AREA

4.00+/-0.05

2X ⌒ 0.15 C

2X ⌒ 0.15 C

DATUM B

DATUM A

2.76+/-0.10

0.40+/-0.05

CENTER TAB

DETAIL B

2.76+/-0.10

0.65

0.35+/-0.05

16X ⊕ 0.10 Ⓜ C A B
0.05 Ⓜ C

0.20 REF   C

// 0.10 C

16X
⌒ 0.08 C
SEATING PLANE

0.85+/-0.05

0.00-0.05

DATUM A OR B

0.65/2

0.65

TERMINAL TIP

DETAIL B
SCALE:NTS

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6.2 Recommended PCB Footprint

CENTER PAD

0.35
0.65
0.55
3.70
2.76
2.76
3.70

NOTE: All dimensions are in millimeters.

The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package type / dimensions / pad pitch	16-pin QFN / 4mm x 4mm / 0.65mm
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, Ψ	11.0°C/W
Pb-free and RoHS compliant, Halogen-free	Yes

6.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 6-1.
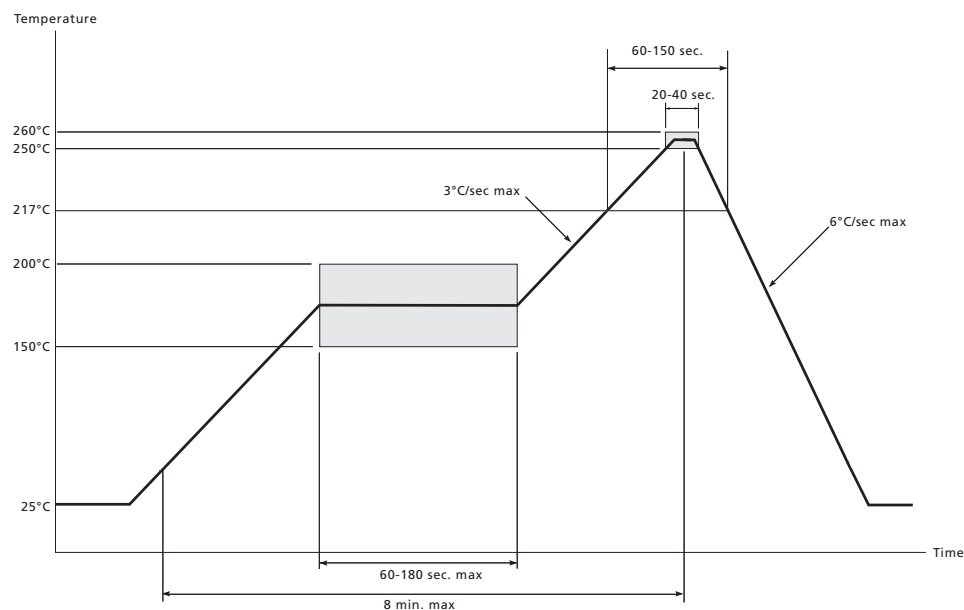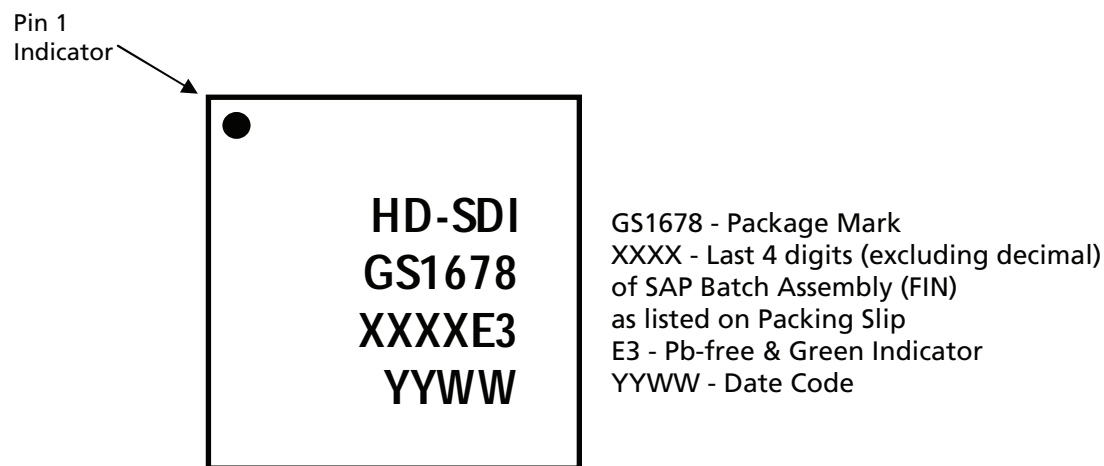
Figure 6-1: Maximum Pb-free Solder Reflow Profile (Preferred)

6.5 Marking Diagram

HD-SDI
GS1678
XXXXE3
YYWW

GS1678 - Package Mark
XXXX - Last 4 digits (excluding decimal)
of SAP Batch Assembly (FIN)
as listed on Packing Slip
E3 - Pb-free & Green Indicator
YYWW - Date Code

6.6 Ordering Information

	Part Number	Package	Temperature Range
GS1678	GS1678-INE3	16-pin QFN	-40°C to 85°C
GS1678	GS1678-INTE3	16-pin QFN 250pc Reel	-40°C to 85°C
GS1678	GS1678-INTE3Z	16-pin QFN 2,500pc Reel	-40°C to 85°C

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Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
1	155931	–	March 2011	Changed pin #16 to N/C in Pin Out and Typical Application Circuit. Updated Figure 3-2: V_{OUT} vs. RSET.
0	154128	–	May 2010	Converted to Data Sheet. Renamed pin 16 in Pin Out and Application Information.
A	153463	–	March 2010	New document.

DOCUMENT IDENTIFICATION
DATA SHEET

The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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