L9375

Eight channel valve driver

Data brief

Features

- Octal low-side output drivers with protection diagnostic
  - 4 x 3A, 160 mΩ typ.
  - 4 x 3A, 200 mΩ typ.
- Programmable channel timer
- Clock monitor
- 4 channels with Integrated recirculation diodes
- 4 channels with 40 V clamp for fast free wheeling of inductive loads.
- Serial peripheral interface with 16 bits, up to 5 MHz with diagnosis
- Battery compatible supply voltage
- Detailed Load diagnosis
  - Over load protection
  - Open load
  - Undercurrent
  - Undervoltage
  - Temperature warning and shutdown
  - Power or signal GND loss
  - Freewheeling diode loss

PowerSO-36

Description

The L9375 s a eight channel low side driver with integrated recirculation diodes for PWM controlled channels 5 to 8. The switching of the channels is programmable via a SPI (serial peripheral interface). The main time base is given by an external clock via CLKin. The clock unit monitors this external clock and provides the system clock for all timings. A synchronization unit is used to monitor the SPI communication and provide a sync signal for the channel activation.

The output duty cycle for each PWM controlled channel can be programmed individually and will be activated by the set point unit. Is possible to program two output duty cycles per channel with a block of 16 SPI commands as well as an individual duration time for each channel actuation. Both information are stored in the PWM and in the counter configuration register respectively.
The PWM Controller translates the programmed digital duty cycle value in a PWM signal which controls the output.

The channels 1 to 4 are configured as switching channels. To achieve a fast switch off a high voltage output clamp is implemented for a rapid free-wheeling if the inductive load. The switch on time can be programmed via SPI.

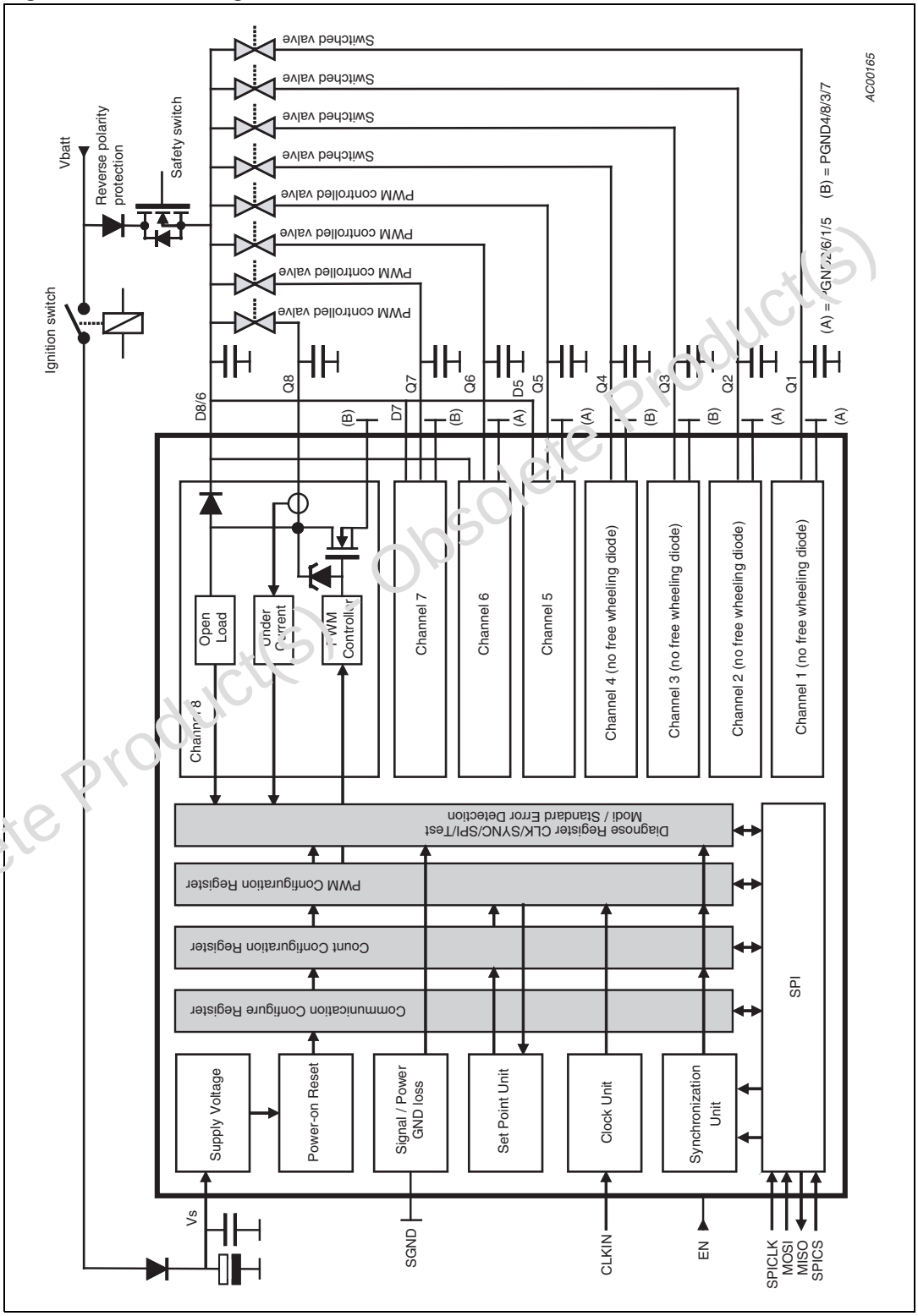
All channels are equipped with a load diagnostic. This allows to detect an open load in off condition as well as a under current in on condition. The power stage is protected against over current and over temperature. A weak connection in power ground, in the recirculation path or in the external clock is monitored and leads to a switch off of the power stages in case an error occurs. All monitored functions can be read out in a serial diagnostic protocol dedicated for each channel via SPI.

Table 1. Device summary

Part number	Package	Packing
L9375LF	PowerSO-36 (slug down)	Tube

1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (top view)

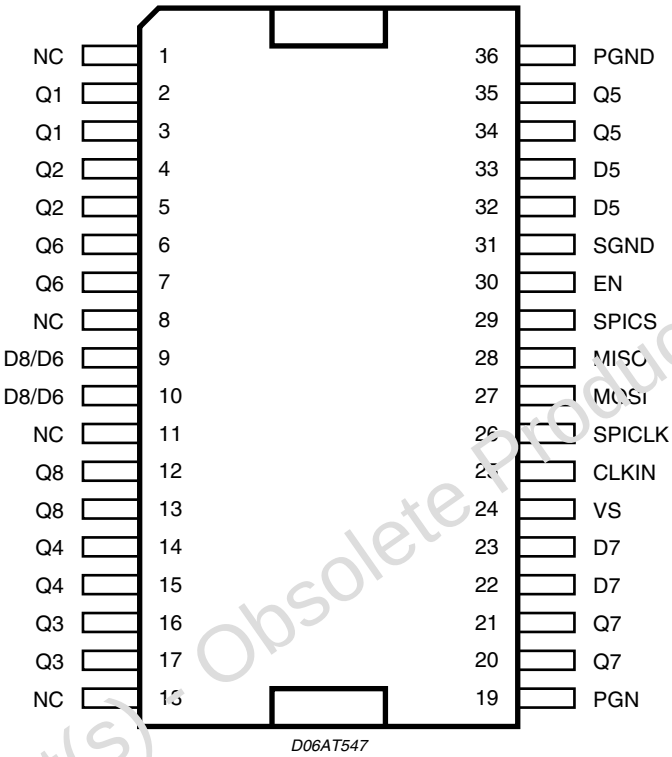


Table 2. Pins description

Pin No.	Name	Description
1	NC	Not connected.
2	Q1	Output.
3	Q1	Output.
4	Q2	Output.
5	Q2	Output.
6	Q6	Output.
7	Q6	Output.
8	NC	Not connected.
9	D8/D66	Free wheeling diode.
10	D8/D66	Free wheeling diode.
11	NC	Not connected.
12	Q8	Output.
13	Q8	Output.

Table 2. Pins description (continued)

Pin No.	Name	Description
14	Q4	Output.
15	Q4	Output.
16	Q3	Output.
17	Q3	Output.
18	NC	Not connected.
19	PGND	Power ground.
20	Q7	Output.
21	Q7	Output.
22	D7	Output.
23	D7	Output.
24	VS	Supply pin
25	CLKIN	Input for precise clock.
26	SPICLK	SPI communication clock
27	MOSI	Input Master Out Slave Input for SPI communication.
28	MISO	Master In Slave Out Out for SPI communication.
29	SPICS	SPI Chip Select.
30	EN	Enable
31	SGND	Signal ground.
32	D5	Free wheeling diode.
33	D5	Free wheeling diode.
34	Q5	Output.
35	Q5	Output.
36	PGND	Power ground.

3 Absolute maximum ratings

3.1 Voltage ratings

Table 3. Voltage ratings

Symbol	Parameter	Min	Max	Unit
V_s	Supply voltage	-0.3	38	V
V_{Dx}	Freewheeling diode voltage	-0.3	35	V
V_{Qx}	Output voltage	-0.3	35	V
V_{EN} V_{SPICLK} V_{SPICS} V_{MOSI} V_{MISO} V_{CLKIN}	Enable voltage SPI clock voltage SPI chip select voltage SPI MOSI voltage SPI MISO voltage SPI clock input voltage	-0.3	6	V

Warning: Transients beyond this limit will cause currents into ESD structures which must be limited externally to ±10 mA (maximum energy to be dissipated: 2 mJ).

3.2 Current ratings

Table 4. Current ratings

Symbol	Parameter	Min	Max	Unit
I_Q	Output current at reversal voltage	-	-2	A
I_{EN_CL} I_{SPICLK_CL} I_{SPICS_CL} I_{MOSI_CL} I_{CLKIN_CL}	Input clamping currents (static) Input clamping currents (dynamic)	- 3 -10	+ 3 +10	mA

Definition: current from outside towards the L9375 -> " + "

Current from L9375 towards ext. components -> " - "

3.3 ESD susceptibility

3.3.1 HBM

ESD susceptibility HBM according to EIA/JESD 22-A 114B

Table 5. HBM

Symbol	Parameter	Condition	Min	Max	Unit
V_{QHBM}	Output pins D_X; Q_X;	PGND12, PGND3, PGND4, LGND and GND are connected together.	± 4	-	kV
V_{LHBM}	Logic Pins	all Pins	± 2	-	kV

3.3.2 MM

ESD susceptibility according to EIA/JESD22-A115-A

Table 6. MM

Symbol	Parameter	Condition	Min	Max	Unit
V_{MM}	Machine Model (MM)	All pins	± 250	-	V

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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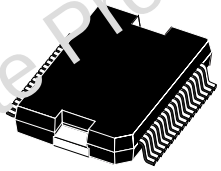
Figure 3. PowerSO-36 (slug down) mechanical data and package dimensions

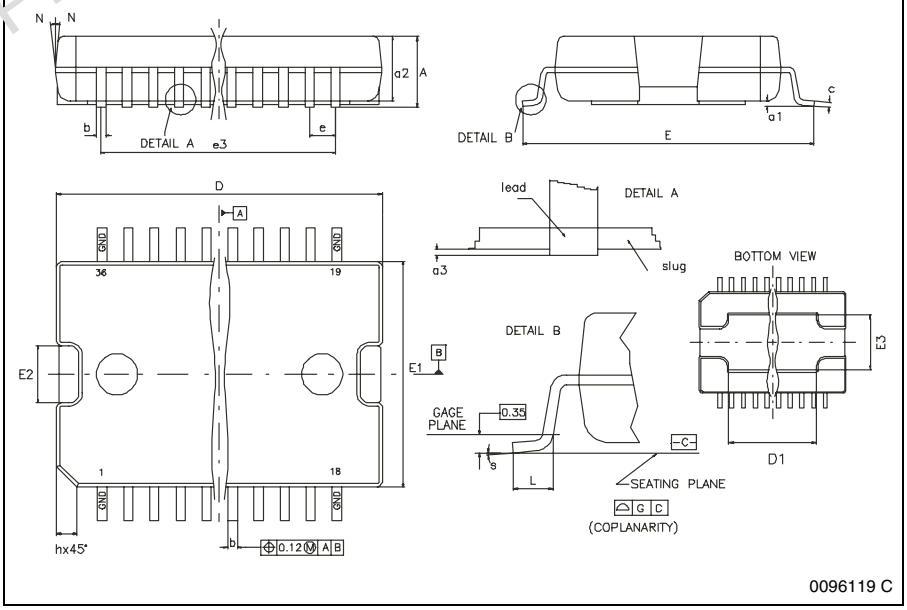
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10			0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.5	0.5472		0.5709
E1	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.80		6.20	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10			0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.8		1.10	0.0315		0.0433
N	10° (max)					
s	8° (max)					

Note: "D and E1" do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006")
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO-36



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
05-Jun-2007	1	Initial release.
19-May-2009	2	Updated *Table 1: Device summary on page 1*. Updated *Section 4: Package information on page 7*.

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