

IRLR8713PbF IRLU8713PbF

Applications

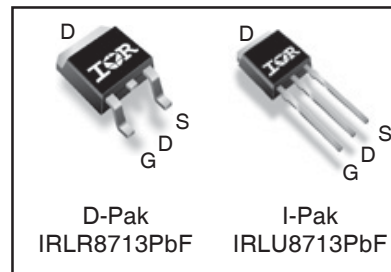
- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	Qg
25V	4.8m Ω	17.4nC



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	100 ^④	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	72 ^④	
I_{DM}	Pulsed Drain Current ^①	410	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation ^⑤	81	W
P_D @ $T_C = 100^\circ\text{C}$	Maximum Power Dissipation ^⑤	40	
	Linear Derating Factor	0.54	W/ $^\circ\text{C}$
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^⑥	—	1.86	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ^{⑤⑥}	—	50	
$R_{\theta JA}$	Junction-to-Ambient ^⑥	—	110	

Notes ^① through ^⑥ are on page 10

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	16	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.8	4.8	m Ω	$V_{GS} = 10V, I_D = 21A$ ③
		—	5.0	6.3		$V_{GS} = 4.5V, I_D = 17A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.85	2.35	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-7.0	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	79	—	—	S	$V_{DS} = 13V, I_D = 17A$
Q_g	Total Gate Charge	—	17.4	26	nC	$V_{DS} = 13V$ $V_{GS} = 4.5V$ $I_D = 17A$ See Fig.16
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	4.0	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	2.2	—		
Q_{gd}	Gate-to-Drain Charge	—	5.8	—		
Q_{godr}	Gate Charge Overdrive	—	5.4	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	8.0	—	nC	$V_{DS} = 10V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	8.6	—		
R_G	Gate Resistance	—	0.9	1.6	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = 13V, V_{GS} = 4.5V$ ③ $I_D = 17A$ Clamped Inductive Load
t_r	Rise Time	—	24	—		
$t_{d(off)}$	Turn-Off Delay Time	—	12	—		
t_f	Fall Time	—	5.9	—		
C_{iss}	Input Capacitance	—	2240	—	pF	$V_{GS} = 0V$ $V_{DS} = 13V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	580	—		
C_{rss}	Reverse Transfer Capacitance	—	270	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	190	mJ
I_{AR}	Avalanche Current ①	—	17	A
E_{AR}	Repetitive Avalanche Energy ①	—	8.1	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	100 ④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	410		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 17A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	16	24	ns	$T_J = 25^\circ\text{C}, I_F = 17A, V_{DD} = 13V$
Q_{rr}	Reverse Recovery Charge	—	15	23	nC	$di/dt = 300A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

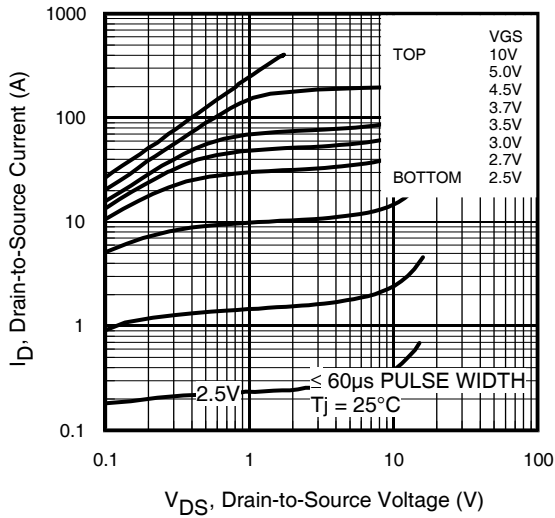


Fig 1. Typical Output Characteristics

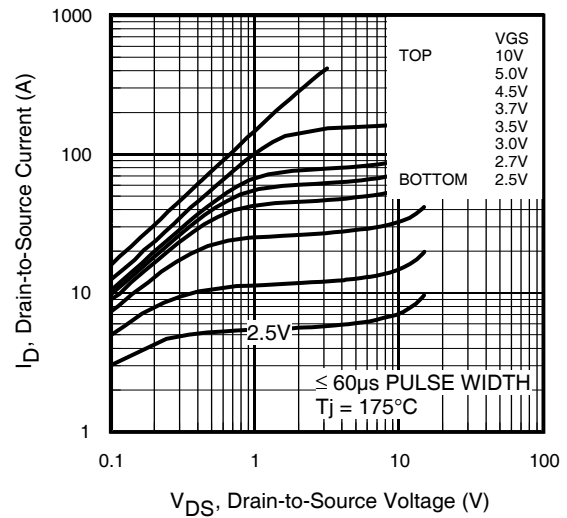


Fig 2. Typical Output Characteristics

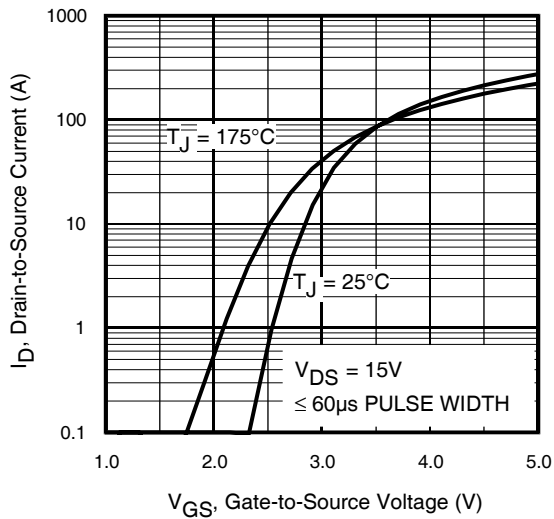


Fig 3. Typical Transfer Characteristics

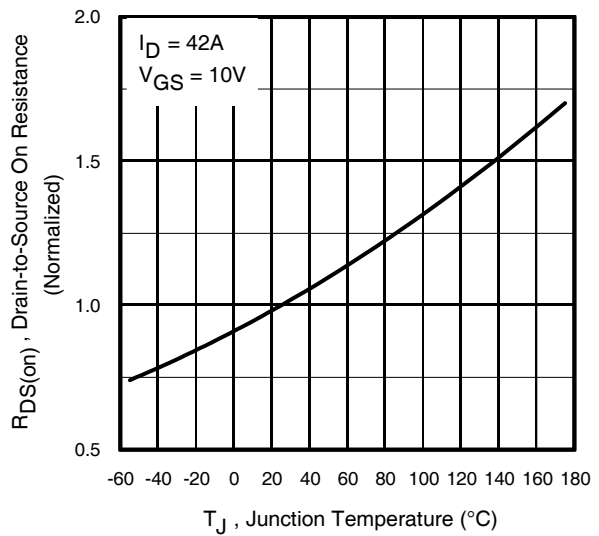


Fig 4. Normalized On-Resistance Vs. Temperature

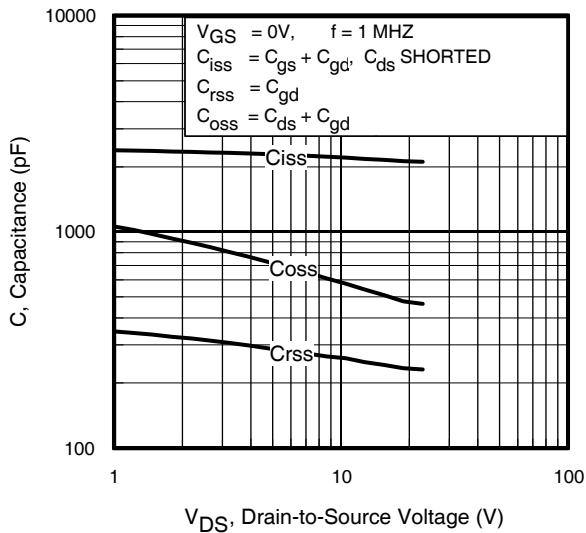


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

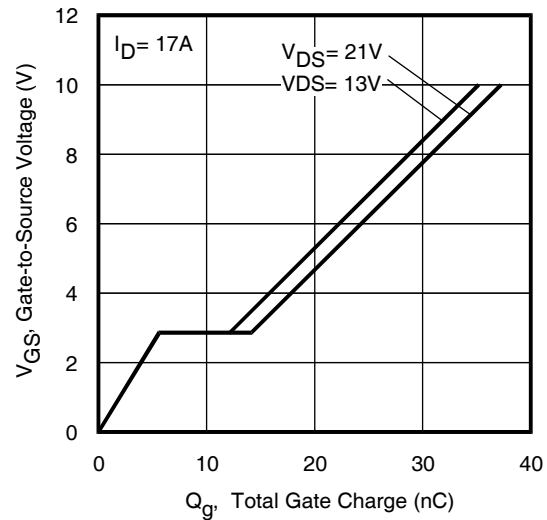


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

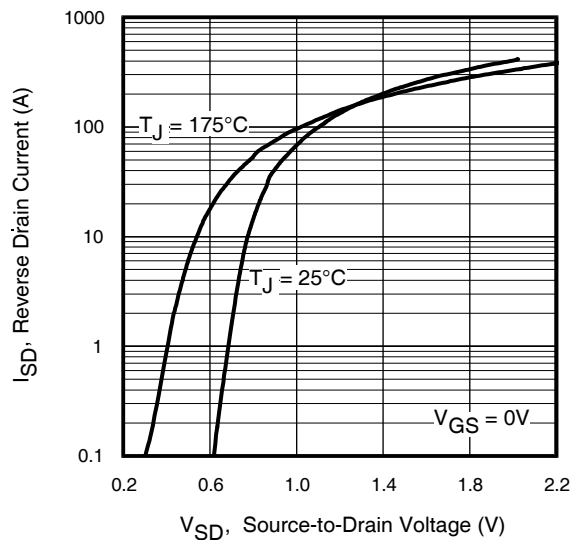


Fig 7. Typical Source-Drain Diode Forward Voltage

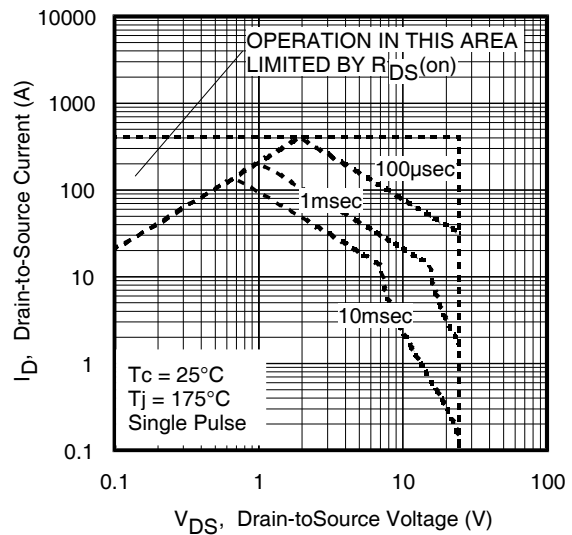


Fig 8. Maximum Safe Operating Area

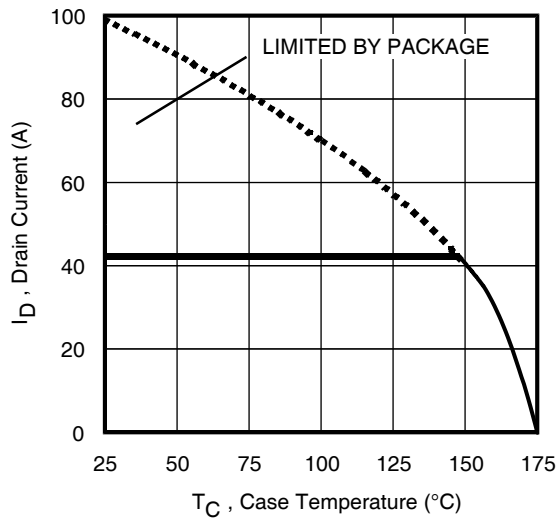


Fig 9. Maximum Drain Current Vs. Case Temperature

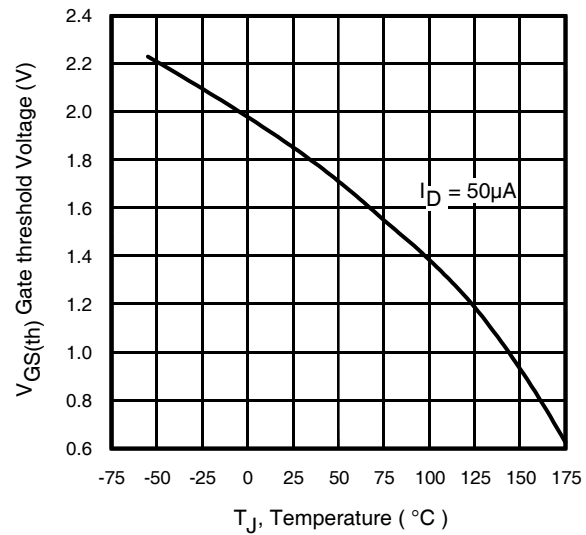


Fig 10. Threshold Voltage Vs. Temperature

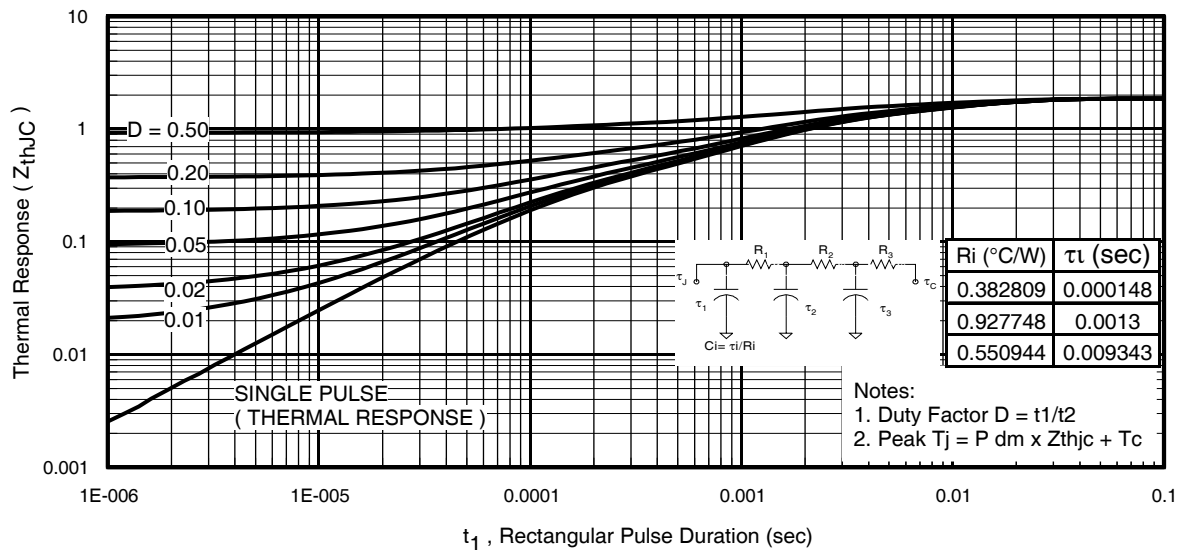


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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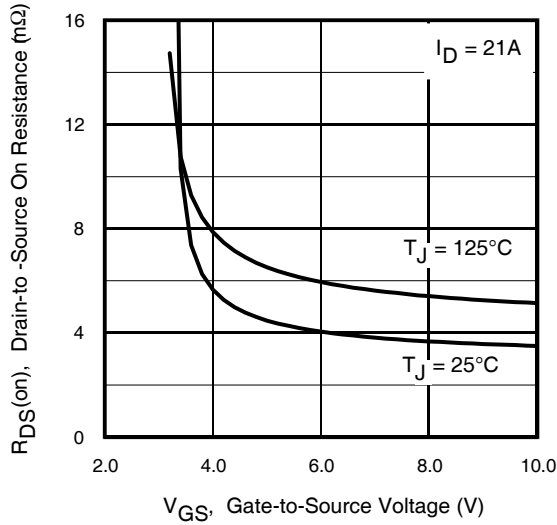


Fig 12. On-Resistance vs. Gate Voltage

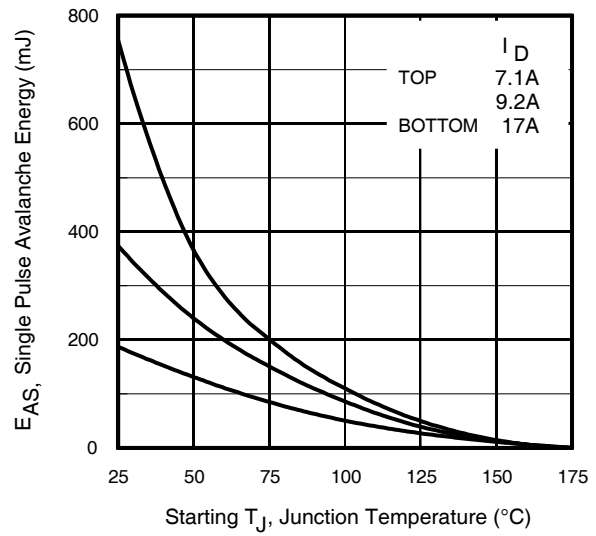


Fig 13. Maximum Avalanche Energy vs. Drain Current

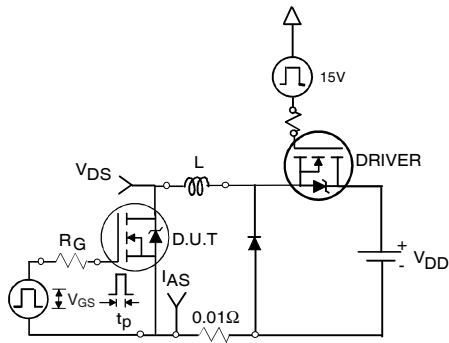


Fig 14a. Unclamped Inductive Test Circuit

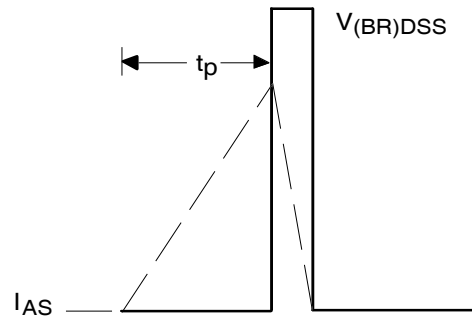


Fig 14b. Unclamped Inductive Waveforms

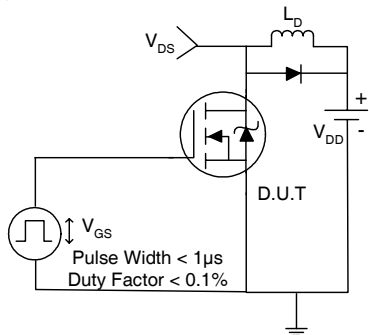


Fig 15a. Switching Time Test Circuit

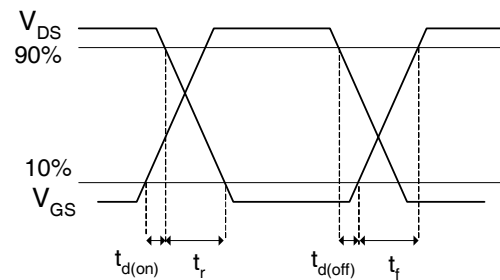


Fig 15b. Switching Time Waveforms

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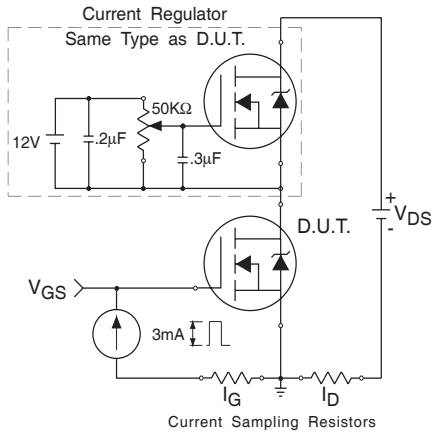


Fig 16a. Gate Charge Test Circuit

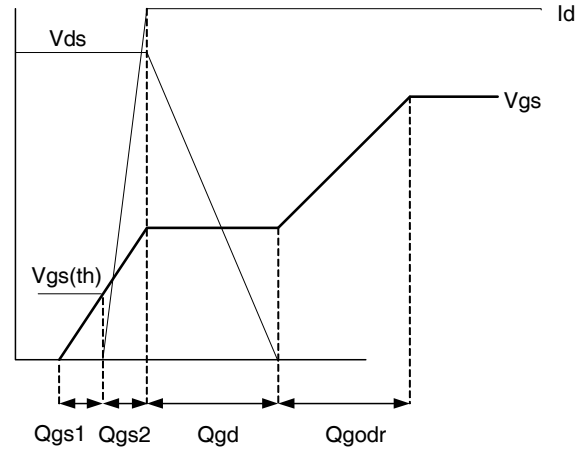
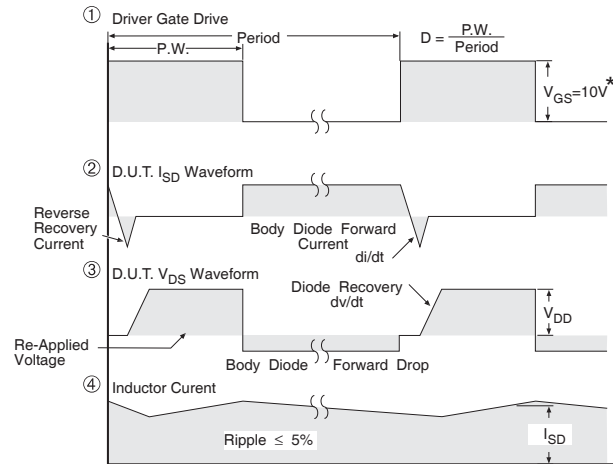
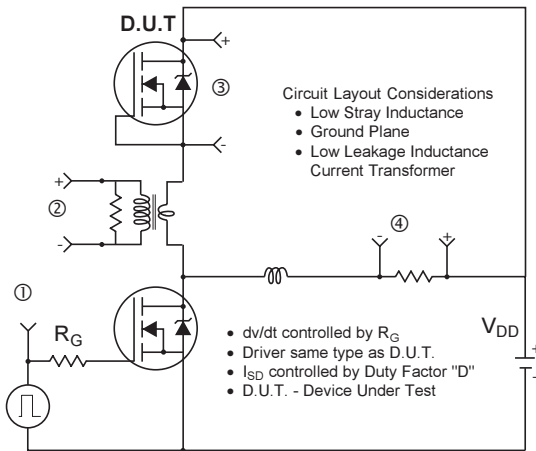


Fig 16b. Gate Charge Waveform



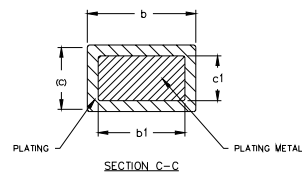
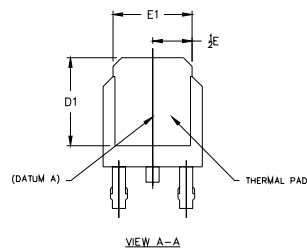
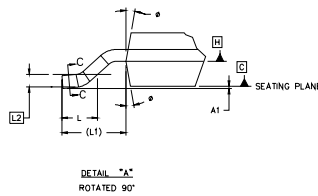
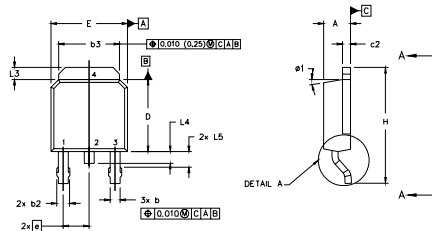
* V_{GS} = 5V for Logic Level Devices

Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel
HEXFET® Power MOSFETs

IRLR/U8713PbF

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D-Pak (TO-252AA) Package Outline



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M-1994.
 - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
 - 3.0 LEAD DIMENSION UNCONTROLLED IN L5.
 - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
 - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	
#	0" 0'	10" 0'	0" 0'	10" 0'	3
#1	0" 0'	15" 0'	0" 0'	15" 0'	

LEAD ASSIGNMENTS

HEXFET

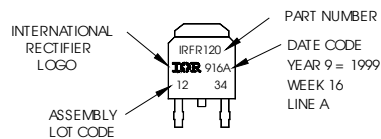
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

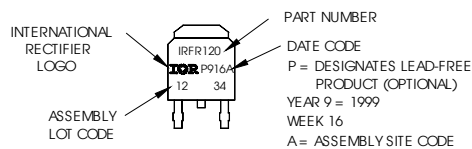
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"
Note: "P" in assembly line
position indicates "Lead-Free"



OR



Technical drawing of a three-pin connector assembly, showing front, side, and cross-sectional views with dimensions and tolerances.

Front View (Top Left): Shows the top profile of the connector. Dimensions include overall width E , pin spacing $b4$, pin diameter $\varnothing 0.010 (0.025) \text{ [C] [A] [B]}$, pin length L , and pin diameter $b2$. Surface features are labeled 1, 2, 3, and 4. Tolerances are indicated by triangles 4 and 5.

Side View (Top Right): Shows the side profile. Dimensions include overall height A , pin diameter $c2$, and a "SEATING PLANE" feature.

Front View (Bottom Left): Shows the bottom profile. Dimensions include overall width $E1$, pin spacing $b1, b3$, pin diameter $b2$, and pin length L . Surface features are labeled 1, 2, 3, and 4. Tolerances are indicated by triangles 4 and 5.

Cross-Section A-A (Bottom Right): Shows the internal structure of the connector. Dimensions include overall width $(b, b2)$, overall height (c) , and pin diameter $b1, b3$.

SECTION A-A

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED
0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST
EXTREMES OF THE PLASTIC BODY.
4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5 LEAD DIMENSION UNCONTROLLED IN L3.
6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
8 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	Ø	15'	Ø	15'	

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line
position indicates "Lead-Free"

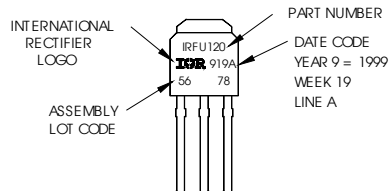


Diagram illustrating the markings on an International Rectifier (IRF) MOSFET package:

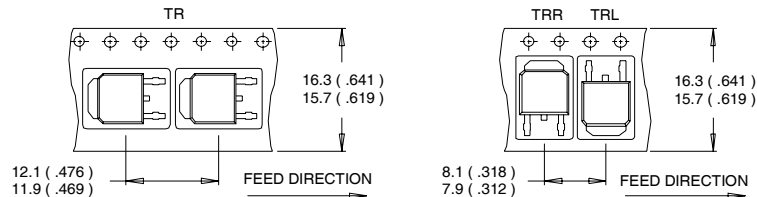
- INTERNATIONAL RECTIFIER LOGO**: Points to the IR logo on the package.
- PART NUMBER**: Points to the text **IRF-U120** on the package.
- DATE CODE**: Points to the text **P919A** on the package.
- ASSEMBLY LOT CODE**: Points to the text **56 78** on the package.
- P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)**: Points to the letter **P** in the date code **P919A**.
- YEAR 9 = 1999**: Points to the number **9** in the date code **P919A**.
- WEEK 19**: Points to the number **19** in the date code **P919A**.
- A = ASSEMBLY SITE CODE**: Points to the letter **A** in the date code **P919A**.

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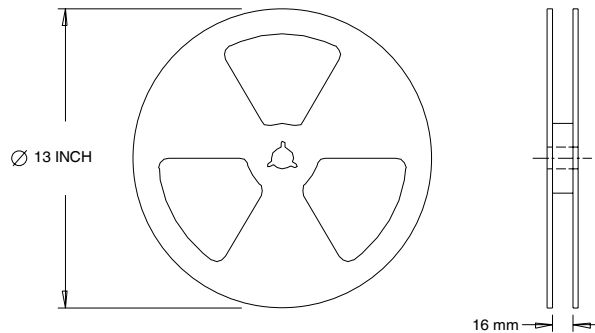
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D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.77\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 17\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ R_θ is measured at T_J approximately at 90°C

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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