



## 18Mb Pipelined DDR™II SRAM Burst of 4

**IDT71P73204**  
**IDT71P73104**  
**IDT71P73804**  
**IDT71P73604**

### Features

- ◆ 18Mb Density (2Mx8, 2Mx9, 1Mx18, 512Kx36)
- ◆ Common Read and Write Data Port
- ◆ Dual Echo Clock Output
- ◆ 4-Word Burst on all SRAM accesses
- ◆ Multiplexed Address Bus
  - One Read or One Write request per two clock cycles.
- ◆ DDR (Double Data Rate) Data Bus
  - Four word bursts data per two clock cycles
- ◆ Depth expansion through Control Logic
- ◆ HSTL (1.5V) inputs that can be scaled to receive signals from 1.4V to 1.9V.
- ◆ Scalable output drivers
  - Can drive HSTL, 1.8V TTL or any voltage level from 1.4V to 1.9V.
  - Output Impedance adjustable from 35 ohms to 70 ohms
- ◆ 1.8V Core Voltage (VDD)
- ◆ JTAG Interface
- ◆ 165-ball, 1.0mm pitch, 13mm x 15mm fBGA Package

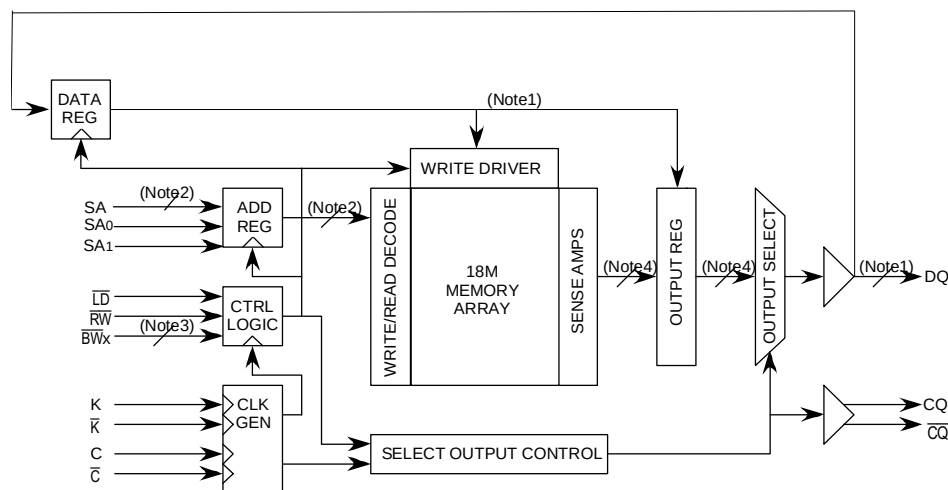
### Description

The IDT DDRII™ Burst of four SRAMs are high-speed synchronous memories with a double-data-rate (DDR), bidirectional data port. This scheme allows maximization on the bandwidth on the data bus by passing two data items per clock cycle. The address bus operates at less than single data rate speeds, allowing the user to fan out addresses and ease system design while maintaining maximum performance on data transfers.

The DDRII has scalable output impedance on its data output bus and echo clocks, allowing the user to tune the bus for low noise and high performance.

All interfaces of the DDRII SRAM are HSTL, allowing speeds beyond SRAM devices that use any form of TTL interface. The interface can be scaled to higher voltages (up to 1.9V) to interface with 1.8V systems if necessary. The device has a VDDQ and a separate Vref, allowing the user to designate the interface operational voltage, independent of the device core voltage of 1.8V VDD. The output impedance control allows the user to adjust the drive strength to adapt to a wide range of loads and transmission lines.

### Functional Block Diagram



#### Notes

- 1) Represents 8 data signal lines for x8, 9 signal lines for x9, 18 signal lines for x18, and 36 signal lines for x36
- 2) Represents 19 address signal lines for x8 and x9, 20 address signal lines for x18, and 19 address signal lines for x36.
- 3) Represents 1 signal line for x9, 2 signal lines for x18, and four signal lines for x36. On x8 parts, the  $\overline{BW}$  is a "nibble write" and there are 2 signal lines.
- 4) Represents 16 data signal lines for x8, 18 signal lines for x9, 36 signal lines for x18, and 72 signal lines for x36.

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## Clocking

The DDRII SRAM has two sets of input clocks, namely the K,  $\bar{K}$  clocks and the C,  $\bar{C}$  clocks. In addition, the QDRII has an output "echo" clock, CQ,  $\bar{CQ}$ .

The K and  $\bar{K}$  clocks are the primary device input clocks. The K clock is used to clock in the control signals ( $\bar{LD}$ ,  $R/\bar{W}$  and  $B\bar{W}x$  or  $N\bar{W}x$ ), the address, and the first and third words of the data burst during a write operation. The  $\bar{K}$  clock is used to clock in the control signals ( $B\bar{W}x$  or  $N\bar{W}x$ ), and the second and fourth words of the data burst during a write operation. The K and  $\bar{K}$  clocks are also used internally by the SRAM. In the event that the user disables the C and  $\bar{C}$  clocks, the K and  $\bar{K}$  clocks will also be used to clock the data out of the output register and generate the echo clocks.

The C and  $\bar{C}$  clocks may be used to clock the data out of the output register during read operations and to generate the echo clocks. C and  $\bar{C}$  must be presented to the SRAM within the timing tolerances. The output data from the DDRII will be closely aligned to the C and  $\bar{C}$  input, through the use of an internal DLL. When C is presented to the DDRII SRAM, the DLL will have already internally clocked the data to arrive at the device output simultaneously with the arrival of the  $\bar{C}$  clock. The C and second data item of the burst will also correspond. The third and fourth data words will follow on the next clock cycle of the  $\bar{C}$  and C, respectively.

## Single Clock Mode

The DDRII SRAM may be operated with a single clock pair. C and  $\bar{C}$  may be disabled by tying both signals high, forcing the outputs and echo clocks to be controlled instead by the K and  $\bar{K}$  clocks.

## DLL Operation

The DLL in the output structure of the DDRII SRAM can be used to closely align the incoming clocks C and  $\bar{C}$  with the output of the data, generating very tight tolerances between the two. The user may disable the DLL by holding  $\bar{Doff}$  low. With the DLL off, the C and  $\bar{C}$  (or K and  $\bar{K}$  if C and  $\bar{C}$  are not used) will directly clock the output register of the SRAM. With the DLL off, there will be a propagation delay from the time the clock enters the device until the data appears at the output.

## Echo Clock

The echo clocks, CQ and  $\bar{CQ}$ , are generated by the C and  $\bar{C}$  clocks (or K,  $\bar{K}$  if C,  $\bar{C}$  are disabled). The rising edge of C generates the rising edge of CQ, and the falling edge of  $\bar{CQ}$ . The rising edge of  $\bar{C}$  generates the rising edge of  $\bar{CQ}$  and the falling edge of CQ. This scheme improves the correlation of the rising and falling edges of the echo clock and will improve the duty cycle of the individual signals.

The echo clock is very closely aligned with the data, guaranteeing that the echo clock will remain closely correlated with the data, within the tolerances designated.

## Read and Write Operations

Read operations are initiated by holding Read/Write control input ( $R/\bar{W}$ ) high, the load control input ( $\bar{LD}$ ) low and presenting the read address to the address port during the rising edge of K, which will latch the address. The data will then be read and will appear at the device

output at the designated time in correspondence with the C and  $\bar{C}$  clocks.

Write operations are initiated by holding the Read/Write control input ( $R/\bar{W}$ ) low, the load control input ( $\bar{LD}$ ) low and presenting the write address to the address port during the rising edge of K, which will latch the address. On the following rising edge of K, the first word of the four word burst must be present on the data input bus  $DQ[x:0]$ , along with the appropriate byte write or nibble write ( $B\bar{W}x$  or  $N\bar{W}x$ ) inputs. On the following rising edge of  $\bar{K}$ , the second word of the data write burst will be accepted at the device input with the designated ( $B\bar{W}x$  or  $N\bar{W}x$ ) inputs. The subsequent K and  $\bar{K}$  rising edges will receive the last two words of the four word burst, with their  $B\bar{W}x/N\bar{W}x$  enables.

DDRII devices internally store four words of the burst as a single, wide word and will retain their order in the burst. The x8 and x9 devices do not have the ability to address to the single word level or change the burst order; however the byte and nibble write signals can be used to prevent writing any byte or individual nibbles, or combined to prevent writing one word of the burst. The x18 and x36 DDRII devices have the ability to address to the individual word level using the SA0 and SA1 address bits, but the burst will continue in a linear sequence and wraps around without incrementing the SA bits. When reading or writing x18 and x36 DDRII devices, the burst will begin at the designated address, but if the burst is started at any other position than the first word of the burst, the burst will wrap back on itself and read the first locations before completing. The x18 and x36 DDRII devices can also use the byte write signals to prevent writing any individual byte or word of the burst.

## Output Enables

The DDRII SRAM automatically enables and disables the  $DQ[x:0]$  outputs. When a valid read is in progress, and data is present at the output, the output will be enabled. If no valid data is present at the output (read not active), the output will be disabled (high impedance). The echo clocks will remain valid at all times and cannot be disabled or turned off. During power-up the DQ outputs will come up in a high impedance state.

## Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and Vss to allow the SRAM to adjust its output drive impedance. The value of RQ must be 5X the value of the intended drive impedance of the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of +/- 10% is between 175 ohms and 350 ohms, with  $V_{DDQ} = 1.5V$ . The output impedance is adjusted every 1024 clock cycles to correct for drifts in supply voltage and temperature. If the user wishes to drive the output impedance of the SRAM to its lowest value, the ZQ pin may be tied to  $V_{DDQ}$ .

## Pin Definitions

| Symbol                                                     | Pin Function             | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------------------------------------------------------------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DQ[X:0]                                                    | Input/Output Synchronous | Data I/O signals. Data inputs are sampled on the rising edge of K and $\bar{K}$ during valid write operations. Data outputs are driven during a valid read operation. The outputs are aligned with the rising edge of both C and $\bar{C}$ during normal operation. When operating in a single clock mode (C and $\bar{C}$ tied high), the outputs are aligned with the rising edge of both K and $\bar{K}$ . When a Read operation is not initiated or $\bar{LD}$ is high (deselected) during the rising edge of K, DQ[X:0] are automatically driven to high impedance after any previous read operation in progress completes.<br>2M x 8 -- DQ[7:0]<br>2M x 9 -- DQ[8:0]<br>1M x 18 -- DQ[17:0]<br>512K x 36 -- DQ[35:0]                                                       |
| $\bar{BW}_0$ , $\bar{BW}_1$<br>$\bar{BW}_2$ , $\bar{BW}_3$ | Input Synchronous        | Byte Write Select 0, 1, 2, and 3 are active LOW. Sampled on the rising edge of the K and again on the rising edge of $\bar{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. All the byte writes are sampled on the same edge as the data. Deselecting a Byte Write Select will cause the corresponding byte of data to be ignored and not written in to the device.<br>2M x 9 -- $\bar{BW}_0$ controls DQ[8:0]<br>1M x 18 -- $\bar{BW}_0$ controls DQ[8:0] and $\bar{BW}_1$ controls DQ[17:9]<br>512K x 36 -- $\bar{BW}_0$ controls DQ[8:0], $\bar{BW}_1$ controls DQ[17:9], $\bar{BW}_2$ controls DQ[26:18] and $\bar{BW}_3$ controls DQ[35:27] |
| $\bar{NW}_0$ , $\bar{NW}_1$                                | Input Synchronous        | Nibble Write Select 0 and 1 are active LOW. Available only on x8 bit parts instead of Byte Write Selects. Sampled on the rising edge of the K and $\bar{K}$ clocks during write operations. Used to select which nibble is written into the device during the current portion of the write operations. Nibbles not written remain unaltered. All the nibble writes are sampled on the same edge as the data. Deselecting a Nibble Write Select will cause the corresponding nibble of data to be ignored and not written in to the device.<br>2M x 8 -- $\bar{NW}_0$ controls D[3:0] and $\bar{NW}_1$ controls D[7:4].                                                                                                                                                           |
| SA                                                         | Input Synchronous        | Address Inputs. Addresses are sampled on the rising edge of K clock during active read or write operations.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| SA <sub>0</sub> , SA <sub>1</sub>                          | Input Synchronous        | Burst count address bits on x18 and x36 DDRII devices. These bits allow changing the burst order in read or write operations, or addressing to the individual word of a burst. See page 9 for all possible burst sequences.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| $\bar{LD}$                                                 | Input Synchronous        | Load Control Logic. Sampled on the rising edge of K. If $\bar{LD}$ is low, a four word burst read or write operation will initiate designated by the R/ $\bar{W}$ input. If $\bar{LD}$ is high during the rising edge of K, operations in progress will complete, but new operations will not be initiated.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| R/ $\bar{W}$                                               | Input Synchronous        | Read or Write Control Logic. If $\bar{LD}$ is low during the rising edge of K, the R/ $\bar{W}$ indicates whether a new operation should be a read or write. If R/ $\bar{W}$ is high, a read operation will be initiated, if R/ $\bar{W}$ is low, a write operation will be initiated. If the $\bar{LD}$ input is high during the rising edge of K, the R/ $\bar{W}$ input will be ignored.                                                                                                                                                                                                                                                                                                                                                                                      |
| C                                                          | Input Clock              | Positive Output Clock Input. C is used in conjunction with $\bar{C}$ to clock out the Read data from the device. C and $\bar{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| $\bar{C}$                                                  | Input Clock              | Negative Output Clock Input. $\bar{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\bar{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| K                                                          | Input Clock              | Positive Input Clock Input. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through DQ[X:0] when in single clock mode. All accesses are initiated on the rising edge of K.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| $\bar{K}$                                                  | Input Clock              | Negative Input Clock Input. $\bar{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through DQ[X:0] when in single clock mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| CQ, $\bar{CQ}$                                             | Output Clock             | Synchronous Echo clock outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals are free running and do not stop when the output data is three stated.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ZQ                                                         | Input                    | Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. DQ[X:0] output impedance is set to $0.2 \times R_Q$ , where $R_Q$ is a resistor connected between ZQ and ground. Alternately, this pin can be connected directly to VDDQ, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.                                                                                                                                                                                                                                                                                                                                                                           |

## Pin Definitions continued

| Symbol                   | Pin Function    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|--------------------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{\text{Doff}}$ | Input           | DLL Turn Off. When low this input will turn off the DLL inside the device. The AC timings with the DLL turned off will be different from those listed in this data sheet. There will be an increased propagation delay from the incidence of C and $\overline{\text{C}}$ to DQ, or K and $\overline{\text{K}}$ to DQ as configured. The propagation delay is not a tested parameter, but will be similar to the propagation delay of other SRAM devices in this speed grade. |
| TDO                      | Output          | TDO pin for JTAG                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| TCK                      | Input           | TCK pin for JTAG.                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| TDI                      | Input           | TDI pin for JTAG. An internal resistor will pull TDI to VDD when the pin is unconnected.                                                                                                                                                                                                                                                                                                                                                                                     |
| TMS                      | Input           | TMS pin for JTAG. An internal resistor will pull TMS to VDD when the pin is unconnected.                                                                                                                                                                                                                                                                                                                                                                                     |
| NC                       | No Connect      | No connects inside the package. Can be tied to any voltage level                                                                                                                                                                                                                                                                                                                                                                                                             |
| VREF                     | Input Reference | Reference Voltage input. Static input used to set the reference level for HSTL inputs and Outputs as well as AC measurement points.                                                                                                                                                                                                                                                                                                                                          |
| VDD                      | Power Supply    | Power supply inputs to the core of the device. Should be connected to a 1.8V power supply.                                                                                                                                                                                                                                                                                                                                                                                   |
| VSS                      | Ground          | Ground for the device. Should be connected to ground of the system.                                                                                                                                                                                                                                                                                                                                                                                                          |
| VDDQ                     | Power Supply    | Power supply for the outputs of the device. Should be connected to a 1.5V power supply for HSTL or scaled to the desired output voltage.                                                                                                                                                                                                                                                                                                                                     |

6431 tbl 02b

## Pin Configuration IDT71P73204 (2M x 8)

|   | 1                        | 2                         | 3                | 4                       | 5                        | 6                     | 7                        | 8                      | 9                | 10                        | 11              |
|---|--------------------------|---------------------------|------------------|-------------------------|--------------------------|-----------------------|--------------------------|------------------------|------------------|---------------------------|-----------------|
| A | $\overline{\text{CQ}}$   | VSS/<br>SA <sup>(2)</sup> | SA               | $\overline{\text{R/W}}$ | $\overline{\text{NW}}_1$ | $\overline{\text{K}}$ | NC                       | $\overline{\text{LD}}$ | SA               | VSS/<br>SA <sup>(1)</sup> | CQ              |
| B | NC                       | NC                        | NC               | SA                      | NC                       | K                     | $\overline{\text{NW}}_0$ | SA                     | NC               | NC                        | DQ <sub>3</sub> |
| C | NC                       | NC                        | NC               | VSS                     | SA                       | NC                    | SA                       | VSS                    | NC               | NC                        | NC              |
| D | NC                       | NC                        | NC               | VSS                     | VSS                      | VSS                   | VSS                      | VSS                    | NC               | NC                        | NC              |
| E | NC                       | NC                        | DQ <sub>4</sub>  | V <sub>DDQ</sub>        | VSS                      | VSS                   | VSS                      | V <sub>DDQ</sub>       | NC               | NC                        | DQ <sub>2</sub> |
| F | NC                       | NC                        | NC               | V <sub>DDQ</sub>        | V <sub>DD</sub>          | VSS                   | V <sub>DD</sub>          | V <sub>DDQ</sub>       | NC               | NC                        | NC              |
| G | NC                       | NC                        | DQ <sub>5</sub>  | V <sub>DDQ</sub>        | V <sub>DD</sub>          | VSS                   | V <sub>DD</sub>          | V <sub>DDQ</sub>       | NC               | NC                        | NC              |
| H | $\overline{\text{Doff}}$ | V <sub>REF</sub>          | V <sub>DDQ</sub> | V <sub>DDQ</sub>        | V <sub>DD</sub>          | VSS                   | V <sub>DD</sub>          | V <sub>DDQ</sub>       | V <sub>DDQ</sub> | V <sub>REF</sub>          | ZQ              |
| J | NC                       | NC                        | NC               | V <sub>DDQ</sub>        | V <sub>DD</sub>          | VSS                   | V <sub>DD</sub>          | V <sub>DDQ</sub>       | NC               | DQ <sub>1</sub>           | NC              |
| K | NC                       | NC                        | NC               | V <sub>DDQ</sub>        | V <sub>DD</sub>          | VSS                   | V <sub>DD</sub>          | V <sub>DDQ</sub>       | NC               | NC                        | NC              |
| L | NC                       | DQ <sub>6</sub>           | NC               | V <sub>DDQ</sub>        | VSS                      | VSS                   | VSS                      | V <sub>DDQ</sub>       | NC               | NC                        | DQ <sub>0</sub> |
| M | NC                       | NC                        | NC               | VSS                     | VSS                      | VSS                   | VSS                      | VSS                    | NC               | NC                        | NC              |
| N | NC                       | NC                        | NC               | VSS                     | SA                       | SA                    | SA                       | VSS                    | NC               | NC                        | NC              |
| P | NC                       | NC                        | DQ <sub>7</sub>  | SA                      | SA                       | C                     | SA                       | SA                     | NC               | NC                        | NC              |
| R | TDO                      | TCK                       | SA               | SA                      | SA                       | $\overline{\text{C}}$ | SA                       | SA                     | SA               | TMS                       | TDI             |

6431 tbl 12

### 165-ball FBGA Pinout TOP VIEW

#### NOTES:

1. A10 is reserved for the 36Mb expansion address.
2. A2 is reserved for the 72Mb expansion address.

## Pin Configuration IDT71P73104 (2M x 9)

|   | 1                        | 2                         | 3               | 4                       | 5   | 6                     | 7                      | 8                      | 9    | 10                        | 11              |
|---|--------------------------|---------------------------|-----------------|-------------------------|-----|-----------------------|------------------------|------------------------|------|---------------------------|-----------------|
| A | $\overline{\text{CQ}}$   | VSS/<br>SA <sup>(2)</sup> | SA              | R $\overline{\text{W}}$ | NC  | $\overline{\text{K}}$ | NC                     | $\overline{\text{LD}}$ | SA   | VSS/<br>SA <sup>(1)</sup> | CQ              |
| B | NC                       | NC                        | NC              | SA                      | NC  | K                     | $\overline{\text{BW}}$ | SA                     | NC   | NC                        | DQ <sub>3</sub> |
| C | NC                       | NC                        | NC              | VSS                     | SA  | NC                    | SA                     | VSS                    | NC   | NC                        | NC              |
| D | NC                       | NC                        | NC              | VSS                     | VSS | VSS                   | VSS                    | VSS                    | NC   | NC                        | NC              |
| E | NC                       | NC                        | DQ <sub>4</sub> | VDDQ                    | VSS | VSS                   | VSS                    | VDDQ                   | NC   | NC                        | DQ <sub>2</sub> |
| F | NC                       | NC                        | NC              | VDDQ                    | VDD | VSS                   | VDD                    | VDDQ                   | NC   | NC                        | NC              |
| G | NC                       | NC                        | DQ <sub>5</sub> | VDDQ                    | VDD | VSS                   | VDD                    | VDDQ                   | NC   | NC                        | NC              |
| H | $\overline{\text{Doff}}$ | VREF                      | VDDQ            | VDDQ                    | VDD | VSS                   | VDD                    | VDDQ                   | VDDQ | VREF                      | ZQ              |
| J | NC                       | NC                        | NC              | VDDQ                    | VDD | VSS                   | VDD                    | VDDQ                   | NC   | DQ <sub>1</sub>           | NC              |
| K | NC                       | NC                        | NC              | VDDQ                    | VDD | VSS                   | VDD                    | VDDQ                   | NC   | NC                        | NC              |
| L | NC                       | DQ <sub>6</sub>           | NC              | VDDQ                    | VSS | VSS                   | VSS                    | VDDQ                   | NC   | NC                        | DQ <sub>0</sub> |
| M | NC                       | NC                        | NC              | VSS                     | VSS | VSS                   | VSS                    | VSS                    | NC   | NC                        | NC              |
| N | NC                       | NC                        | NC              | VSS                     | SA  | SA                    | SA                     | VSS                    | NC   | NC                        | NC              |
| P | NC                       | NC                        | DQ <sub>7</sub> | SA                      | SA  | C                     | SA                     | SA                     | NC   | NC                        | DQ <sub>8</sub> |
| R | TDO                      | TCK                       | SA              | SA                      | SA  | $\overline{\text{C}}$ | SA                     | SA                     | SA   | TMS                       | TDI             |

6431 tbl 12a

## 165-ball FBGA Pinout TOP VIEW

### NOTES:

1. A10 is reserved for the 36Mb expansion address.
2. A2 is reserved for the 72Mb expansion address.

## Pin Configuration IDT71P73804 (1M x 18)

|   | 1                        | 2                                  | 3                | 4                       | 5                        | 6                     | 7                        | 8                      | 9                | 10                                 | 11              |
|---|--------------------------|------------------------------------|------------------|-------------------------|--------------------------|-----------------------|--------------------------|------------------------|------------------|------------------------------------|-----------------|
| A | $\overline{\text{CQ}}$   | V <sub>SS</sub> /SA <sup>(2)</sup> | SA               | R $\overline{\text{W}}$ | $\overline{\text{BW}}_1$ | $\overline{\text{K}}$ | NC                       | $\overline{\text{LD}}$ | SA               | V <sub>SS</sub> /SA <sup>(1)</sup> | CQ              |
| B | NC                       | DQ <sub>9</sub>                    | NC               | SA                      | NC                       | K                     | $\overline{\text{BW}}_0$ | SA                     | NC               | NC                                 | DQ <sub>8</sub> |
| C | NC                       | NC                                 | NC               | V <sub>SS</sub>         | SA                       | SA <sub>0</sub>       | SA <sub>1</sub>          | V <sub>SS</sub>        | NC               | DQ <sub>7</sub>                    | NC              |
| D | NC                       | NC                                 | DQ <sub>10</sub> | V <sub>SS</sub>         | V <sub>SS</sub>          | V <sub>SS</sub>       | V <sub>SS</sub>          | V <sub>SS</sub>        | NC               | NC                                 | NC              |
| E | NC                       | NC                                 | DQ <sub>11</sub> | V <sub>DDQ</sub>        | V <sub>SS</sub>          | V <sub>SS</sub>       | V <sub>SS</sub>          | V <sub>DDQ</sub>       | NC               | NC                                 | DQ <sub>6</sub> |
| F | NC                       | DQ <sub>12</sub>                   | NC               | V <sub>DDQ</sub>        | V <sub>DD</sub>          | V <sub>SS</sub>       | V <sub>DD</sub>          | V <sub>DDQ</sub>       | NC               | NC                                 | DQ <sub>5</sub> |
| G | NC                       | NC                                 | DQ <sub>13</sub> | V <sub>DDQ</sub>        | V <sub>DD</sub>          | V <sub>SS</sub>       | V <sub>DD</sub>          | V <sub>DDQ</sub>       | NC               | NC                                 | NC              |
| H | $\overline{\text{Doff}}$ | V <sub>REF</sub>                   | V <sub>DDQ</sub> | V <sub>DDQ</sub>        | V <sub>DD</sub>          | V <sub>SS</sub>       | V <sub>DD</sub>          | V <sub>DDQ</sub>       | V <sub>DDQ</sub> | V <sub>REF</sub>                   | ZQ              |
| J | NC                       | NC                                 | NC               | V <sub>DDQ</sub>        | V <sub>DD</sub>          | V <sub>SS</sub>       | V <sub>DD</sub>          | V <sub>DDQ</sub>       | NC               | DQ <sub>4</sub>                    | NC              |
| K | NC                       | NC                                 | DQ <sub>14</sub> | V <sub>DDQ</sub>        | V <sub>DD</sub>          | V <sub>SS</sub>       | V <sub>DD</sub>          | V <sub>DDQ</sub>       | NC               | NC                                 | DQ <sub>3</sub> |
| L | NC                       | DQ <sub>15</sub>                   | NC               | V <sub>DDQ</sub>        | V <sub>SS</sub>          | V <sub>SS</sub>       | V <sub>SS</sub>          | V <sub>DDQ</sub>       | NC               | NC                                 | DQ <sub>2</sub> |
| M | NC                       | NC                                 | NC               | V <sub>SS</sub>         | V <sub>SS</sub>          | V <sub>SS</sub>       | V <sub>SS</sub>          | V <sub>SS</sub>        | NC               | DQ <sub>1</sub>                    | NC              |
| N | NC                       | NC                                 | DQ <sub>16</sub> | V <sub>SS</sub>         | SA                       | SA                    | SA                       | V <sub>SS</sub>        | NC               | NC                                 | NC              |
| P | NC                       | NC                                 | DQ <sub>17</sub> | SA                      | SA                       | C                     | SA                       | SA                     | NC               | NC                                 | DQ <sub>0</sub> |
| R | TDO                      | TCK                                | SA               | SA                      | SA                       | $\overline{\text{C}}$ | SA                       | SA                     | SA               | TMS                                | TDI             |

### 165-ball FBGA Pinout TOP VIEW

6431 tbl 12b

#### NOTES:

1. A10 is reserved for the 36Mb expansion address. This must be tied or driven to V<sub>SS</sub> on the 1M x 18 DDRII Burst of 4 (71P73804) devices.
2. A2 is reserved for the 72Mb expansion address. This must be tied or driven to V<sub>SS</sub> on the 1M x 18 DDRII Burst of 4 (71P73804) devices.

## Pin Configuration IDT71P73604 (512K x 36)

|   | 1                        | 2                         | 3                        | 4                       | 5                        | 6                     | 7                        | 8                      | 9    | 10                        | 11               |
|---|--------------------------|---------------------------|--------------------------|-------------------------|--------------------------|-----------------------|--------------------------|------------------------|------|---------------------------|------------------|
| A | $\overline{\text{CQ}}$   | VSS/<br>SA <sup>(3)</sup> | NC/<br>SA <sup>(1)</sup> | R $\overline{\text{W}}$ | $\overline{\text{BW}}_2$ | $\overline{\text{K}}$ | $\overline{\text{BW}}_1$ | $\overline{\text{LD}}$ | SA   | VSS/<br>SA <sup>(2)</sup> | CQ               |
| B | NC                       | DQ <sub>27</sub>          | DQ <sub>18</sub>         | SA                      | $\overline{\text{BW}}_3$ | K                     | $\overline{\text{BW}}_0$ | SA                     | NC   | NC                        | DQ <sub>8</sub>  |
| C | NC                       | NC                        | DQ <sub>28</sub>         | VSS                     | SA                       | SA <sub>0</sub>       | SA <sub>1</sub>          | VSS                    | NC   | DQ <sub>17</sub>          | DQ <sub>7</sub>  |
| D | NC                       | DQ <sub>29</sub>          | DQ <sub>19</sub>         | VSS                     | VSS                      | VSS                   | VSS                      | VSS                    | NC   | NC                        | DQ <sub>16</sub> |
| E | NC                       | NC                        | DQ <sub>20</sub>         | VDDQ                    | VSS                      | VSS                   | VSS                      | VDDQ                   | NC   | DQ <sub>15</sub>          | DQ <sub>6</sub>  |
| F | NC                       | DQ <sub>30</sub>          | DQ <sub>21</sub>         | VDDQ                    | VDD                      | VSS                   | VDD                      | VDDQ                   | NC   | NC                        | DQ <sub>5</sub>  |
| G | NC                       | DQ <sub>31</sub>          | DQ <sub>22</sub>         | VDDQ                    | VDD                      | VSS                   | VDD                      | VDDQ                   | NC   | NC                        | DQ <sub>14</sub> |
| H | $\overline{\text{Doff}}$ | VREF                      | VDDQ                     | VDDQ                    | VDD                      | VSS                   | VDD                      | VDDQ                   | VDDQ | VREF                      | ZQ               |
| J | NC                       | NC                        | DQ <sub>32</sub>         | VDDQ                    | VDD                      | VSS                   | VDD                      | VDDQ                   | NC   | DQ <sub>13</sub>          | DQ <sub>4</sub>  |
| K | NC                       | NC                        | DQ <sub>23</sub>         | VDDQ                    | VDD                      | VSS                   | VDD                      | VDDQ                   | NC   | DQ <sub>12</sub>          | DQ <sub>3</sub>  |
| L | NC                       | DQ <sub>33</sub>          | DQ <sub>24</sub>         | VDDQ                    | VSS                      | VSS                   | VSS                      | VDDQ                   | NC   | NC                        | DQ <sub>2</sub>  |
| M | NC                       | NC                        | DQ <sub>34</sub>         | VSS                     | VSS                      | VSS                   | VSS                      | VSS                    | NC   | DQ <sub>11</sub>          | DQ <sub>1</sub>  |
| N | NC                       | DQ <sub>35</sub>          | DQ <sub>25</sub>         | VSS                     | SA                       | SA                    | SA                       | VSS                    | NC   | NC                        | DQ <sub>10</sub> |
| P | NC                       | NC                        | DQ <sub>26</sub>         | SA                      | SA                       | C                     | SA                       | SA                     | NC   | DQ <sub>9</sub>           | DQ <sub>0</sub>  |
| R | TDO                      | TCK                       | SA                       | SA                      | SA                       | $\overline{\text{C}}$ | SA                       | SA                     | SA   | TMS                       | TDI              |

### 165-ball FBGA Pinout TOP VIEW

6431 tbl 12c

#### NOTES:

1. A3 is reserved for the 36Mb expansion address
2. A10 is reserved for the 72Mb expansion address.
3. A2 is reserved for the 144Mb expansion address.



## Write Descriptions<sup>(1,2)</sup>

| Signal         | $\overline{BW}_0$ | $\overline{BW}_1$ | $\overline{BW}_2$ | $\overline{BW}_3$ | $\overline{NW}_0$ | $\overline{NW}_1$ |
|----------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Write Byte 0   | L                 | X                 | X                 | X                 | X                 | X                 |
| Write Byte 1   | X                 | L                 | X                 | X                 | X                 | X                 |
| Write Byte 2   | X                 | X                 | L                 | X                 | X                 | X                 |
| Write Byte 3   | X                 | X                 | X                 | L                 | X                 | X                 |
| Write Nibble 0 | X                 | X                 | X                 | X                 | L                 | X                 |
| Write Nibble 1 | X                 | X                 | X                 | X                 | X                 | L                 |

### NOTES:

6431 tbl 09

1) All byte write ( $\overline{BW}_x$ ) and nibble write ( $\overline{NW}_x$ ) signals are sampled on the rising edge of K and again on  $\overline{K}$ . The data that is present on the data bus in the designated byte/nibble will be latched into the input if the corresponding  $\overline{BW}_x$  or  $\overline{NW}_x$  is held low. The rising edge of K will sample the first and third bytes/nibbles of the four word burst and the rising edge of  $\overline{K}$  will sample the second and fourth bytes/nibbles of the four word burst.

2) The availability of the  $\overline{BW}_x$  or  $\overline{NW}_x$  on designated devices is described in the pin description table.

3) The DDRII Burst of four SRAM has data forwarding. A read request that is initiated on the cycle following a write request to the same address will produce the newly written data in response to the read request.

## Linear Burst Sequence Table <sup>(1,2)</sup>

| SA [1:0] | a  | b  | c  | d  |
|----------|----|----|----|----|
| 00       | 00 | 01 | 10 | 11 |
| 01       | 01 | 10 | 11 | 00 |
| 10       | 10 | 11 | 00 | 01 |
| 11       | 11 | 00 | 01 | 10 |

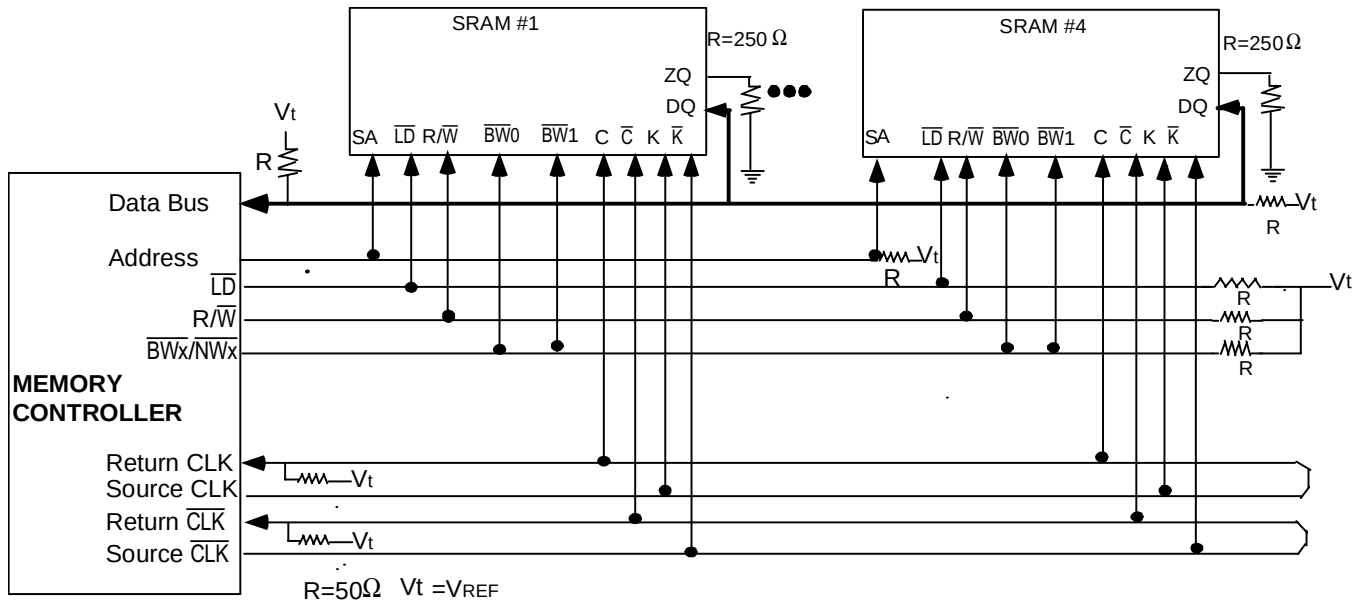
### NOTES:

6431 tbl 22

1. SA [1:0] is the address presented on pins SA1 and SA0 giving the burst sequence a,b,c,d.

2. SA0 and SA1 are only available on the x18 and x36-bit devices.

## Application Example



6431 drw 20

## Absolute Maximum Ratings<sup>(1)(2)</sup>

| Symbol            | Rating                                                         | Value                         | Unit |
|-------------------|----------------------------------------------------------------|-------------------------------|------|
| V <sub>TERM</sub> | Supply Voltage on V <sub>DD</sub> with Respect to GND          | -0.5 to +2.9                  | V    |
| V <sub>TERM</sub> | Supply Voltage on V <sub>DDQ</sub> with Respect to GND         | -0.5 to V <sub>DD</sub> +0.3  | V    |
| V <sub>TERM</sub> | Voltage on Input terminals with respect to GND                 | -0.5 to V <sub>DD</sub> +0.3  | V    |
| V <sub>TERM</sub> | Voltage on Input, Output and I/O terminals with respect to GND | -0.5 to V <sub>DDQ</sub> +0.3 | V    |
| T <sub>BIAS</sub> | Temperature Under Bias                                         | -55 to +125                   | °C   |
| T <sub>STG</sub>  | Storage Temperature                                            | -65 to +150                   | °C   |
| I <sub>OUT</sub>  | Continuous Current into Outputs                                | ± 20                          | mA   |

### NOTES:

6431 tbl 05

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>DDQ</sub> must not exceed V<sub>DD</sub> during normal operation.

## Recommended DC Operating and Temperature Conditions

| Symbol           | Parameter                          | Min. | Typ.                | Max. | Unit |
|------------------|------------------------------------|------|---------------------|------|------|
| V <sub>DD</sub>  | Power Supply Voltage               | 1.7  | 1.8                 | 1.9  | V    |
| V <sub>DDQ</sub> | I/O Supply Voltage                 | 1.4  | 1.5                 | 1.9  | V    |
| V <sub>SS</sub>  | Ground                             | 0    | 0                   | 0    | V    |
| V <sub>REF</sub> | Input Reference Voltage            | 0.68 | V <sub>DDQ</sub> /2 | 0.95 | V    |
| T <sub>A</sub>   | Ambient Temperature <sup>(1)</sup> | 0    | 25                  | 70   | °C   |

### NOTE:

6431 tbl 04

- During production testing, the case temperature equals the ambient temperature.

## Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)<sup>(1)</sup>

| Symbol           | Parameter               | Conditions                                        | Max. | Unit |
|------------------|-------------------------|---------------------------------------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance       | V <sub>DD</sub> = 1.8V<br>V <sub>DDQ</sub> = 1.5V | 5    | pF   |
| C <sub>CLK</sub> | Clock Input Capacitance |                                                   | 6    | pF   |
| C <sub>O</sub>   | Output Capacitance      |                                                   | 7    | pF   |
| C <sub>DQ</sub>  | DQ I/O Capacitance      |                                                   | 7    | pF   |

### NOTE:

6431 tbl 06

- Tested at characterization and retested after any design or process change that may affect these parameters.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD} = 1.8 \pm 100\text{mV}$ , $V_{DDQ} = 1.4\text{V to }1.9\text{V}$ )

| Parameter                      | Symbol | Test Conditions                                                                                               |        | Min         | Max         | Unit | Note |
|--------------------------------|--------|---------------------------------------------------------------------------------------------------------------|--------|-------------|-------------|------|------|
| Input Leakage Current          | IIL    | VDD = Max VIN = VSS to VDDQ                                                                                   |        | -2          | +2          |      |      |
| Output Leakage Current         | IOL    | Output Disabled                                                                                               |        | -2          | +2          |      |      |
| Operating Current (x36): DDR   | IDD    | VDD = Max,<br>IOUT = 0mA (outputs open),<br>Cycle Time ≥ tKHKH Min                                            | 250MHz | -           | 800         | mA   | 1    |
|                                |        |                                                                                                               | 200MHz | -           | 700         |      |      |
|                                |        |                                                                                                               | 167MHz | -           | 600         |      |      |
| Operating Current (x18): DDR   | IDD    | VDD = Max,<br>IOUT = 0mA (outputs open),<br>Cycle Time ≥ tKHKH Min                                            | 250MHz | -           | 650         | mA   | 1    |
|                                |        |                                                                                                               | 200MHz | -           | 550         |      |      |
|                                |        |                                                                                                               | 167MHz | -           | 475         |      |      |
| Operating Current (x9,x8): DDR | IDD    | VDD = Max,<br>IOUT = 0mA (outputs open),<br>Cycle Time ≥ tKHKH Min                                            | 250MHz | -           | 650         | mA   | 1    |
|                                |        |                                                                                                               | 200MHz | -           | 550         |      |      |
|                                |        |                                                                                                               | 167MHz | -           | 475         |      |      |
| Standby Current NOP            | ISB1   | Device Deselected (in NOP state),<br>IOUT = 0mA (outputs open),<br>f=Max,<br>All inputs ≤ 0.2V or ≥ VDD -0.2V | 250MHz | -           | 325         | mA   | 2    |
|                                |        |                                                                                                               | 200MHz | -           | 300         |      |      |
|                                |        |                                                                                                               | 167MHz | -           | 275         |      |      |
| Output High Voltage            | VOH1   | RQ = 250Ω, IOH = -15mA                                                                                        |        | VDDQ/2-0.12 | VDDQ/2+0.12 | V    | 3, 7 |
| Output Low Voltage             | VOL1   | RQ = 250Ω, IOL = 15mA                                                                                         |        | VDDQ/2-0.12 | VDDQ/2+0.12 | V    | 4, 7 |
| Output High Voltage            | VOH2   | IOH = -0.1mA                                                                                                  |        | VDDQ-0.2    | VDDQ        | V    | 5    |
| Output Low Voltage             | VOL2   | IOL = 0.1mA                                                                                                   |        | VSS         | 0.2         | V    | 6    |

6431 tbl 10C

### NOTES:

- Operating Current is measured at 100% bus utilization.
- Standby Current is only after all pending read and write burst operations are completed.
- Outputs are impedance-controlled.  $I_{OH} = -(V_{DDQ}/2)/(R_Q/5)$  and is guaranteed by device characterization for  $175\Omega \leq R_Q < 350\Omega$ . This parameter is tested at  $R_Q = 250\Omega$ , which gives a nominal  $50\Omega$  output impedance.
- Outputs are impedance-controlled.  $I_{OL} = (V_{DDQ}/2)/(R_Q/5)$  and is guaranteed by device characterization for  $175\Omega \leq R_Q < 350\Omega$ . This parameter is tested at  $R_Q = 250\Omega$ , which gives a nominal  $50\Omega$  output impedance.
- This measurement is taken to ensure that the output has the capability of pulling to the  $V_{DDQ}$  rail, and is not intended to be used as an impedance measurement point.
- This measurement is taken to ensure that the output has the capability of pulling to  $V_{SS}$ , and is not intended to be used as an impedance measurement point.
- Programmable Impedance Mode.

## Input Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD} = 1.8 \pm 100\text{mV}$ , $V_{DDQ} = 1.4\text{V}$ to $1.9\text{V}$ )

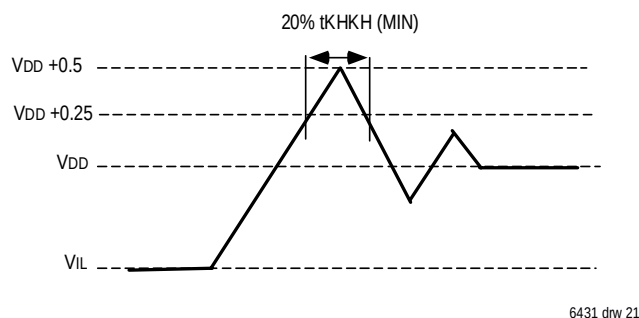
| Parameter              | Symbol        | Min             | Max             | Unit | Notes |
|------------------------|---------------|-----------------|-----------------|------|-------|
| Input High Voltage, DC | $V_{IH}$ (DC) | $V_{REF} + 0.1$ | $V_{DDQ} + 0.3$ | V    | 1,2   |
| Input Low Voltage, DC  | $V_{IL}$ (DC) | -0.3            | $V_{REF} - 0.1$ | V    | 1,3   |
| Input High Voltage, AC | $V_{IH}$ (AC) | $V_{REF} + 0.2$ | -               | V    | 4,5   |
| Input Low Voltage, AC  | $V_{IL}$ (AC) | -               | $V_{REF} - 0.2$ | V    | 4,5   |

6431 tbl 10d

### NOTES:

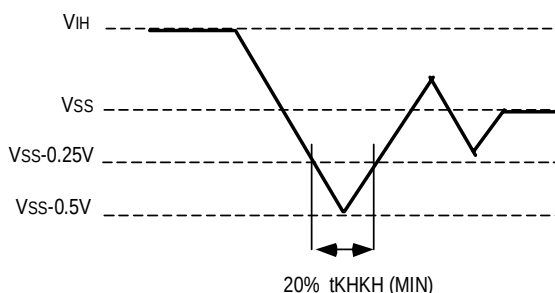
- These are DC test criteria. DC design criteria is  $V_{REF} \pm 50\text{mV}$ . The AC  $V_{IH}/V_{IL}$  levels are defined separately for measuring timing parameters.
- $V_{IH}$  (Max) DC =  $V_{DDQ} + 0.3$ ,  $V_{IH}$  (Max) AC =  $V_{DD} + 0.5\text{V}$  (pulse width  $\leq 20\%$  t<sub>KHKH</sub> (min))
- $V_{IL}$  (Min) DC =  $-0.3\text{V}$ ,  $V_{IL}$  (Min) AC =  $-0.5\text{V}$  (pulse width  $\leq 20\%$  t<sub>KHKH</sub> (min))
- This condition is for AC function test only, not for AC parameter test.
- To maintain a valid level, the transitioning edge of the input must:
  - Sustain a constant slew rate from the current AC level through the target AC level,  $V_{IL}(\text{AC})$  or  $V_{IH}(\text{AC})$
  - Reach at least the target AC level.
  - After the AC target level is reached, continue to maintain at least the target DC level,  $V_{IL}(\text{DC})$  or  $V_{IH}(\text{DC})$

## Overshoot Timing



6431 drw 21

## Undershoot Timing



6431 drw 22

## AC Test Conditions

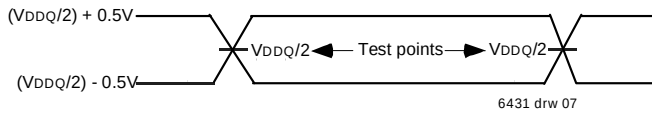
| Parameter                     | Symbol          | Value          | Unit |
|-------------------------------|-----------------|----------------|------|
| Core Power Supply Voltage     | VDD             | 1.7-1.9        | V    |
| Output Power Supply Voltage   | VDDQ            | 1.4-1.9        | V    |
| Input High Level              | V <sub>IH</sub> | (VDDQ/2) + 0.5 | V    |
| Input Low Level               | V <sub>IL</sub> | (VDDQ/2) - 0.5 | V    |
| Input Reference Level         | VREF            | VDDQ/2         | V    |
| Input Rise/Fall Time          | TR/TF           | 0.3/0.3        | ns   |
| DQ Rise/Fall Time             |                 | 0.5/0.5        |      |
| Output Timing Reference Level |                 | VDDQ/2         | V    |

### NOTE:

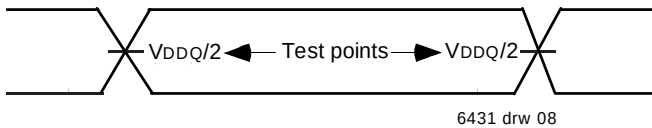
- Parameters are tested with RQ=250Ω

6431 tbl 11a

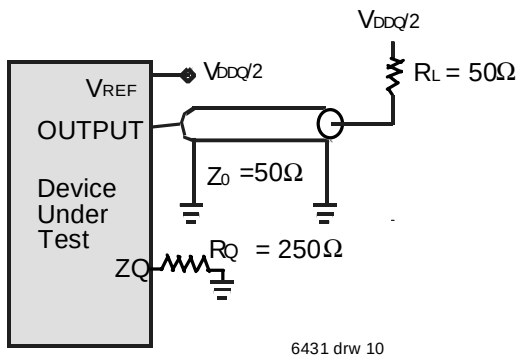
## Input Waveform



## Output Waveform



## AC Test Load



## AC Electrical Characteristics (V<sub>DD</sub> = 1.8 ± 100mV, V<sub>DDQ</sub> = 1.4V to 1.9V, T<sub>A</sub> = 0 to 70°C) <sup>(3,7)</sup>

| Symbol            | Parameter                                    | 250MHz |      | 200MHz |      | 167MHz |      | Unit   | Note  |
|-------------------|----------------------------------------------|--------|------|--------|------|--------|------|--------|-------|
|                   |                                              | Min.   | Max  | Min.   | Max  | Min.   | Max  |        |       |
| Clock Parameters  |                                              |        |      |        |      |        |      |        |       |
| tKHKH             | Average clock cycle time (K,K,C,C)           | 4.00   | 6.30 | 5.00   | 7.88 | 6.00   | 8.40 | ns     |       |
| tKC var           | Cycle to Cycle Period Jitter (K,K,C,C)       | -      | 0.20 | -      | 0.20 | -      | 0.20 | ns     | 1,5   |
| tKHKL             | Clock High Time (K,K,C,C)                    | 1.60   | -    | 2.00   | -    | 2.40   | -    | ns     | 8     |
| tKLKH             | Clock LOW Time (K,K,C,C)                     | 1.60   | -    | 2.00   | -    | 2.40   | -    | ns     | 8     |
| tKHKH             | Clock to clock (K→K, C→C)                    | 1.80   | -    | 2.20   | -    | 2.70   | -    | ns     | 9     |
| tKHKH             | Clock to clock (K→K, C→C)                    | 1.80   | -    | 2.20   | -    | 2.70   | -    | ns     | 9     |
| tKHCH             | Clock to data clock (K→C, K→C)               | 0.00   | 1.80 | 0.00   | 2.30 | 0.00   | 2.80 | ns     |       |
| tKC lock          | DLL lock time (K,C)                          | 1024   | -    | 1024   | -    | 1024   | -    | cycles | 2     |
| tKC reset         | K static to DLL reset                        | 30     | -    | 30     | -    | 30     | -    | ns     |       |
| Output Parameters |                                              |        |      |        |      |        |      |        |       |
| tCHQV             | C,C HIGH to output valid                     | -      | 0.45 | -      | 0.45 | -      | 0.50 | ns     | 3     |
| tCHQX             | C,C HIGH to output hold                      | -0.45  | -    | -0.45  | -    | -0.50  | -    | ns     | 3     |
| tCHCQV            | C,C HIGH to echo clock valid                 | -      | 0.45 | -      | 0.45 | -      | 0.50 | ns     | 3     |
| TCHCQX            | C,C HIGH to echo clock hold                  | -0.45  | -    | -0.45  | -    | -0.50  | -    | ns     | 3     |
| TCQHQV            | CQ,CQ HIGH to output valid                   | -      | 0.30 | -      | 0.35 | -      | 0.40 | ns     |       |
| TCQHQX            | CQ,CQ HIGH to output hold                    | -0.30  | -    | -0.35  | -    | -0.40  | -    | ns     |       |
| TCHQZ             | C HIGH to output HIGH-Z                      | -      | 0.45 | -      | 0.45 | -      | 0.50 | ns     | 3,4,5 |
| TCHQX1            | C HIGH to output LOW-Z                       | -0.45  | -    | -0.45  | -    | -0.50  | -    | ns     | 3,4,5 |
| Set-Up Time       |                                              |        |      |        |      |        |      |        |       |
| tAVKH             | Address valid to K,K rising edge             | 0.50   | -    | 0.6    | -    | 0.7    | -    | ns     | 6     |
| tIVKH             | R, W inputs valid to K,K rising edge         | 0.50   | -    | 0.6    | -    | 0.7    | -    | ns     |       |
| tDVKH             | Data-in and BWx/NWx valid to K,K rising edge | 0.35   | -    | 0.40   | -    | 0.50   | -    | ns     |       |
| Hold Times        |                                              |        |      |        |      |        |      |        |       |
| tKHAX             | K, K rising edge to address hold             | 0.50   | -    | 0.6    | -    | 0.7    | -    | ns     | 6     |
| tKHIX             | K, K rising edge to R, W inputs hold         | 0.50   | -    | 0.6    | -    | 0.7    | -    | ns     |       |
| tKHDX             | K, K rising edge to data-in and BWx/NWx hold | 0.35   | -    | 0.40   | -    | 0.50   | -    | ns     |       |

6431 tbl 11

### NOTES:

1. Cycle to cycle period jitter is the variance from clock rising edge to the next expected clock rising edge, as defined per JEDEC Standard No.65 (EIA/JESD65) pg.10
2. V<sub>DD</sub> slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once V<sub>DD</sub> and input clock are stable.
3. If C,C are tied High, K,K become the references for C,C timing parameters.
4. To avoid bus contention, at a given voltage and temperature t<sub>CHQX1</sub> is bigger than t<sub>CHQZ</sub>. The specs as shown do not imply bus contention because t<sub>CHQX1</sub> is a MIN parameter that is worse case at totally different test conditions (0°C, 1.9V) than t<sub>CHQZ</sub>, which is a MAX parameter (worst case at 70°C, 1.7V). It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
5. This parameter is guaranteed by device characterization, but not production tested.
6. All address inputs must meet the specified setup and hold times for all latching clock edges.
7. During production testing, the case temperature equals T<sub>A</sub>.
8. Clock High Time (t<sub>KHKL</sub>) and Clock Low Time (t<sub>KLKH</sub>) should be within 40% to 60% of the cycle time (t<sub>KHKH</sub>).
9. Clock to clock time (t<sub>KHKH</sub>) and Clock to clock time (t<sub>KHKH</sub>) should be within 45% to 55% of the cycle time (t<sub>KHKH</sub>).



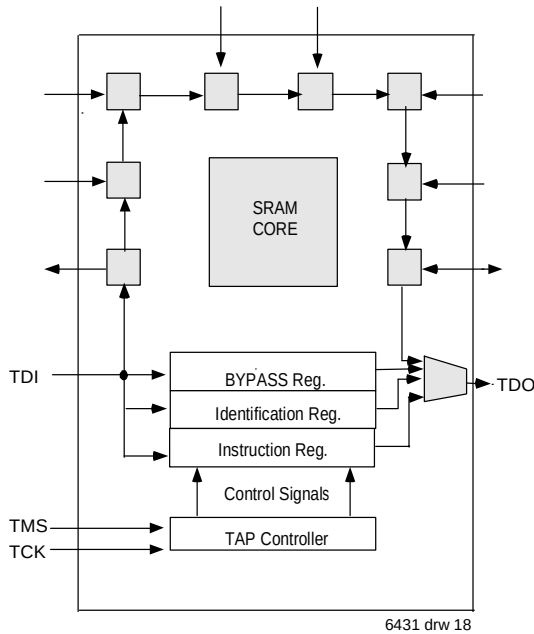


## IEEE 1149.1 Test Access Port and Boundary Scan-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up; therefore, the TRST signal is not

required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to VSS to preclude a mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected, but they may also be tied to VDD through a resistor. TDO should be left unconnected.

### JTAG Block Diagram



### JTAG Instruction Coding

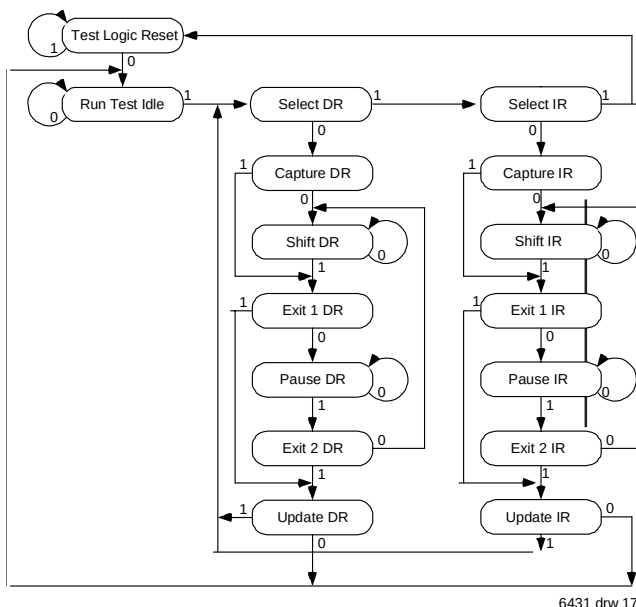
| IR2 | IR1 | IR0 | Instruction    | TDO Output              | Notes |
|-----|-----|-----|----------------|-------------------------|-------|
| 0   | 0   | 0   | EXTEST         | Boundary Scan Register  |       |
| 0   | 0   | 1   | IDCODE         | Identification register | 2     |
| 0   | 1   | 0   | SAMPLE-Z       | Boundary Scan Register  | 1     |
| 0   | 1   | 1   | RESERVED       | Do Not Use              | 5     |
| 1   | 0   | 0   | SAMPLE/PRELOAD | Boundary Scan register  | 4     |
| 1   | 0   | 1   | RESERVED       | Do Not Use              | 5     |
| 1   | 1   | 0   | RESERVED       | Do Not Use              | 5     |
| 1   | 1   | 1   | BYPASS         | Bypass Register         | 3     |

#### NOTES:

6431 tbl 13

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initialized to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when existing the Shift DR states.
4. SAMPLE instruction does not place output pins in Hi-Z.
5. This instruction is reserved for future use.

### TAP Controller State Diagram



## Scan Register Definition

| Part    | Instruction Register | Bypass Register | ID Register | Boundry Scan |
|---------|----------------------|-----------------|-------------|--------------|
| 512Kx36 | 3 bits               | 1 bit           | 32 bits     | 107 bits     |
| 1Mx18   | 3 bits               | 1 bit           | 32 bits     | 107 bits     |
| 2Mx8/x9 | 3 bits               | 1 bit           | 32 bits     | 107 bits     |

6431 tbl 14

## Identification Register Definitions

| INSTRUCTION FIELD                  | ALL DEVICES                          | DESCRIPTION                                       | PART NUMBER                                      |
|------------------------------------|--------------------------------------|---------------------------------------------------|--------------------------------------------------|
| Revision Number (31:29)            | 0x0                                  | Revision Number                                   |                                                  |
| Device ID (28:12)                  | 0x0290<br>0x0291<br>0x0292<br>0x0293 | 512Kx36 DDRII BURST OF 4<br>1Mx18<br>2Mx9<br>2Mx8 | 71P73604S<br>71P73804S<br>71P73104S<br>71P73204S |
| IDT JEDEC ID CODE (11:1)           | 0x033                                | Allows unique identification of SRAM vendor.      |                                                  |
| ID Register Presence Indicator (0) | 1                                    | Indicates the presence of an ID register.         |                                                  |

6431 tbl 15

## Boundary Scan Exit Order (2M x 8-Bit, 2Mx9-Bit, 1Mx18-Bit)

| ORDER | PIN ID |
|-------|--------|
| 1     | 6R     |
| 2     | 6P     |
| 3     | 6N     |
| 4     | 7P     |
| 5     | 7N     |
| 6     | 7R     |
| 7     | 8R     |
| 8     | 8P     |
| 9     | 9R     |
| 10    | 11P    |
| 11    | 10P    |
| 12    | 10N    |
| 13    | 9P     |
| 14    | 10M    |
| 15    | 11N    |
| 16    | 9M     |
| 17    | 9N     |
| 18    | 11L    |
| 19    | 11M    |
| 20    | 9L     |
| 21    | 10L    |
| 22    | 11K    |
| 23    | 10K    |
| 24    | 9J     |
| 25    | 9K     |
| 26    | 10J    |
| 27    | 11J    |
| 28    | 11H    |
| 29    | 10G    |
| 30    | 9G     |
| 31    | 11F    |
| 32    | 11G    |
| 33    | 9F     |
| 34    | 10F    |
| 35    | 11E    |
| 36    | 10E    |

6431 tbl 16

| ORDER | PIN ID   |
|-------|----------|
| 37    | 10D      |
| 38    | 9E       |
| 39    | 10C      |
| 40    | 11D      |
| 41    | 9C       |
| 42    | 9D       |
| 43    | 11B      |
| 44    | 11C      |
| 45    | 9B       |
| 46    | 10B      |
| 47    | 11A      |
| 48    | Internal |
| 49    | 9A       |
| 50    | 8B       |
| 51    | 7C       |
| 52    | 6C       |
| 53    | 8A       |
| 54    | 7A       |
| 55    | 7B       |
| 56    | 6B       |
| 57    | 6A       |
| 58    | 5B       |
| 59    | 5A       |
| 60    | 4A       |
| 61    | 5C       |
| 62    | 4B       |
| 63    | 3A       |
| 64    | 1H       |
| 65    | 1A       |
| 66    | 2B       |
| 67    | 3B       |
| 68    | 1C       |
| 69    | 1B       |
| 70    | 3D       |
| 71    | 3C       |
| 72    | 1D       |

6431 tbl 17

| ORDER | PIN ID |
|-------|--------|
| 73    | 2C     |
| 74    | 3E     |
| 75    | 2D     |
| 76    | 2E     |
| 77    | 1E     |
| 78    | 2F     |
| 79    | 3F     |
| 80    | 1G     |
| 81    | 1F     |
| 82    | 3G     |
| 83    | 2G     |
| 84    | 1J     |
| 85    | 2J     |
| 86    | 3K     |
| 87    | 3J     |
| 88    | 2K     |
| 89    | 1K     |
| 90    | 2L     |
| 91    | 3L     |
| 92    | 1M     |
| 93    | 1L     |
| 94    | 3N     |
| 95    | 3M     |
| 96    | 1N     |
| 97    | 2M     |
| 98    | 3P     |
| 99    | 2N     |
| 100   | 2P     |
| 101   | 1P     |
| 102   | 3R     |
| 103   | 4R     |
| 104   | 4P     |
| 105   | 5P     |
| 106   | 5N     |
| 107   | 5R     |

6431 tbl 18

## Boundary Scan Exit Order (512K x 36-Bit)

| ORDER | PIN ID |
|-------|--------|
| 1     | 6R     |
| 2     | 6P     |
| 3     | 6N     |
| 4     | 7P     |
| 5     | 7N     |
| 6     | 7R     |
| 7     | 8R     |
| 8     | 8P     |
| 9     | 9R     |
| 10    | 11P    |
| 11    | 9P     |
| 12    | 10N    |
| 13    | 10P    |
| 14    | 11M    |
| 15    | 9N     |
| 16    | 9M     |
| 17    | 11N    |
| 18    | 11L    |
| 19    | 10L    |
| 20    | 9L     |
| 21    | 10M    |
| 22    | 11K    |
| 23    | 9K     |
| 24    | 9J     |
| 25    | 10K    |
| 26    | 11J    |
| 27    | 9G     |
| 28    | 11H    |
| 29    | 10G    |
| 30    | 10J    |
| 31    | 11F    |
| 32    | 10F    |
| 33    | 9F     |
| 34    | 11G    |
| 35    | 11E    |
| 36    | 9E     |

6431 tbl 16b

| ORDER | PIN ID   |
|-------|----------|
| 37    | 10D      |
| 38    | 10E      |
| 39    | 11C      |
| 40    | 9D       |
| 41    | 9C       |
| 42    | 11D      |
| 43    | 11B      |
| 44    | 10B      |
| 45    | 9B       |
| 46    | 10C      |
| 47    | 11A      |
| 48    | Internal |
| 49    | 9A       |
| 50    | 8B       |
| 51    | 7C       |
| 52    | 6C       |
| 53    | 8A       |
| 54    | 7A       |
| 55    | 7B       |
| 56    | 6B       |
| 57    | 6A       |
| 58    | 5B       |
| 59    | 5A       |
| 60    | 4A       |
| 61    | 5C       |
| 62    | 4B       |
| 63    | 3A       |
| 64    | 1H       |
| 65    | 1A       |
| 66    | 3B       |
| 67    | 1B       |
| 68    | 1C       |
| 69    | 2B       |
| 70    | 3D       |
| 71    | 2C       |
| 72    | 1D       |

6431 tbl 17b

| ORDER | PIN ID |
|-------|--------|
| 73    | 3C     |
| 74    | 3E     |
| 75    | 1E     |
| 76    | 2E     |
| 77    | 2D     |
| 78    | 3F     |
| 79    | 1F     |
| 80    | 1G     |
| 81    | 2F     |
| 82    | 3G     |
| 83    | 2J     |
| 84    | 1J     |
| 85    | 2G     |
| 86    | 3K     |
| 87    | 1K     |
| 88    | 2K     |
| 89    | 3J     |
| 90    | 3L     |
| 91    | 1L     |
| 92    | 1M     |
| 93    | 2L     |
| 94    | 3N     |
| 95    | 2M     |
| 96    | 1N     |
| 97    | 3M     |
| 98    | 3P     |
| 99    | 1P     |
| 100   | 2P     |
| 101   | 2N     |
| 102   | 3R     |
| 103   | 4R     |
| 104   | 4P     |
| 105   | 5P     |
| 106   | 5N     |
| 107   | 5R     |

6431 tbl 18b

## JTAG DC Operating Conditions

| Parameter                                    | Symbol          | Min        | Typ | Max     | Unit | Note |
|----------------------------------------------|-----------------|------------|-----|---------|------|------|
| Output Power Supply                          | VDDQ            | 1.4        | -   | 1.9     | V    |      |
| Power Supply Voltage                         | VDD             | 1.7        | 1.8 | 1.9     | V    |      |
| Input High Level                             | V <sub>IH</sub> | 1.3        | -   | VDD+0.3 | V    |      |
| Input Low Level                              | V <sub>IL</sub> | -0.3       | -   | 0.5     | V    |      |
| TCK Input Leakage Current                    | I <sub>IL</sub> | -5         | -   | +5      | μA   |      |
| TMS, TDI Input Leakage Current               | I <sub>IL</sub> | -15        | -   | +15     | μA   |      |
| TDO Output Leakage Current                   | I <sub>OL</sub> | -5         | -   | +5      | μA   |      |
| Output High Voltage (I <sub>OH</sub> = -1mA) | V <sub>OH</sub> | VDDQ - 0.2 | -   | VDDQ    | V    | 1    |
| Output Low Voltage (I <sub>OL</sub> = 1mA)   | V <sub>OL</sub> | VSS        | -   | 0.2     | V    | 1    |

### NOTE:

6431 tbl 19

- The output impedance of TDO is set to 50 ohms (nominal process) and does not vary with the external resistor connected to ZQ.

## JTAG AC Test Conditions

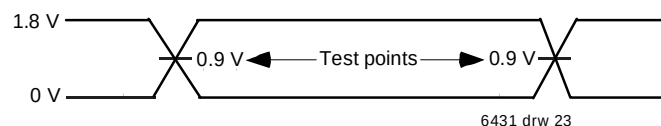
| Parameter                               | Symbol          | Min     | Unit | Note |
|-----------------------------------------|-----------------|---------|------|------|
| Input High Level                        | V <sub>IH</sub> | 1.8     | V    |      |
| Input Low Level                         | V <sub>IL</sub> | 0       | V    |      |
| Input Rise/Fall Time                    | TR/TF           | 1.0/1.0 | ns   |      |
| Input and Output Timing Reference Level |                 | 0.9     | V    | 1    |

### NOTE:

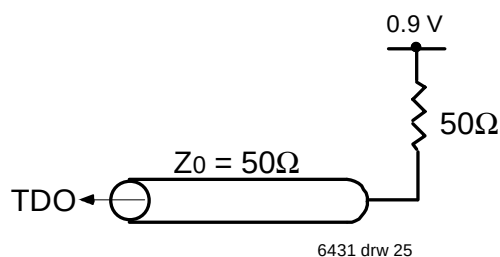
6431 tbl 20

- For SRAM outputs see AC test load on page 14.

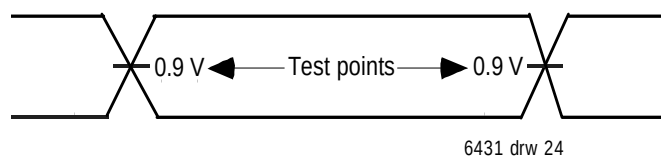
## JTAG Input Test Waveform



## JTAG AC Test Load



## JTAG Output Test Waveform

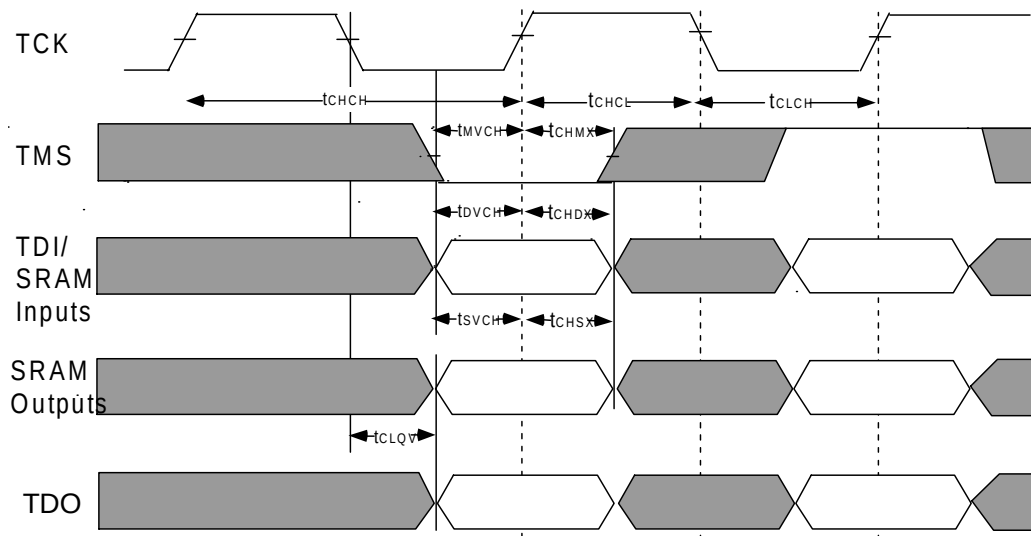


## JTAG AC Characteristics

| Parameter                 | Symbol            | Min | Max | Unit | Note |
|---------------------------|-------------------|-----|-----|------|------|
| TCK Cycle Time            | t <sub>CHCH</sub> | 50  | -   | ns   |      |
| TCK High Pulse Width      | t <sub>CHCL</sub> | 20  | -   | ns   |      |
| TCK Low Pulse Width       | t <sub>CLCH</sub> | 20  | -   | ns   |      |
| TMS Input Setup Time      | t <sub>MVCH</sub> | 5   | -   | ns   |      |
| TMS Input Hold Time       | t <sub>CHMX</sub> | 5   | -   | ns   |      |
| TDI Input Setup Time      | t <sub>DVCH</sub> | 5   | -   | ns   |      |
| TDI Input Hold Time       | t <sub>CHDX</sub> | 5   | -   | ns   |      |
| SRAM Input Setup Time     | t <sub>SVCH</sub> | 5   | -   | ns   |      |
| SRAM Input Hold Time      | t <sub>CHSX</sub> | 5   | -   | ns   |      |
| Clock Low to Output Valid | t <sub>CLQV</sub> | 0   | 10  | ns   |      |

6431 tbl.21

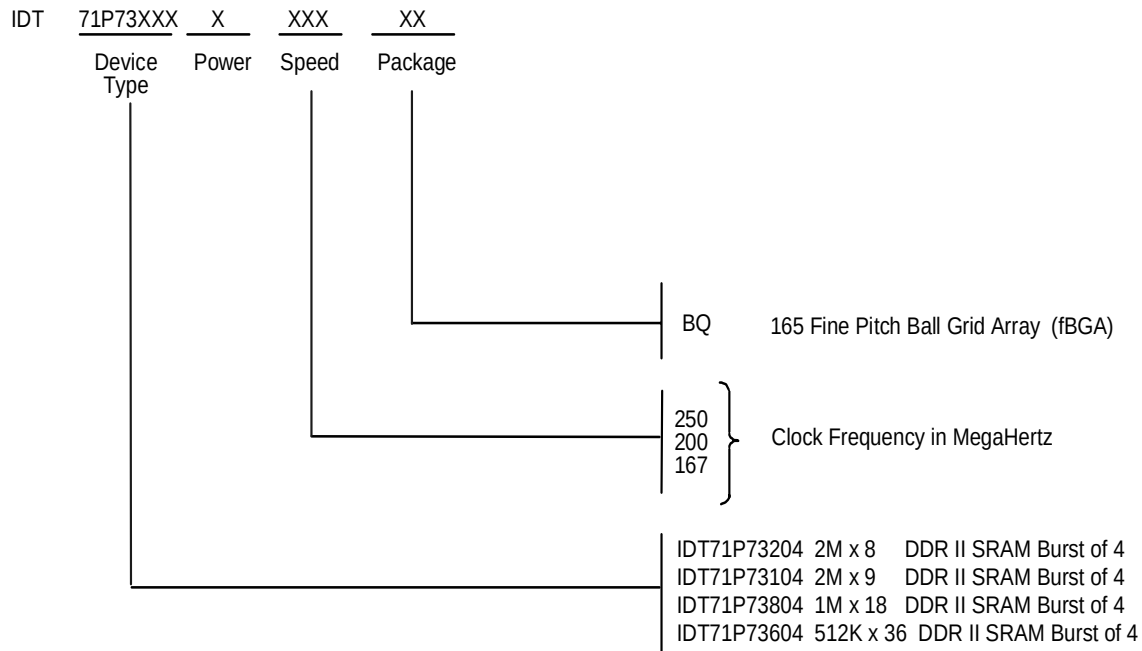
## JTAG Timing Diagram



6431 drw 19



## Ordering Information



6431 drw 15



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## Revision History

| <u>REV</u> | <u>DATE</u> | <u>PAGES</u> | <u>DESCRIPTION</u>       |
|------------|-------------|--------------|--------------------------|
| 0          | 07/29/05    | p. 1-24      | Released Final datasheet |