SN74LV139A Dual 2-Line to 4-Line Decoders/Demultiplexers

1 Features

- 2V to 5.5V V_{CC} operation
- Maximum t_{pd} of 7.5ns at 5V
- Support mixed-mode voltage operation on all ports
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporate two enable inputs to simplify cascading and/or data reception
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 250mA per JESD 17

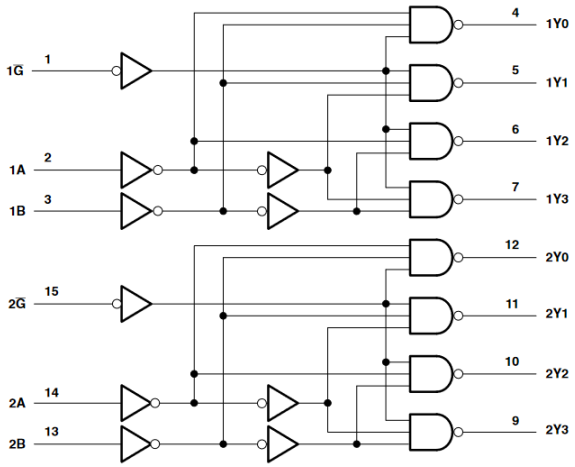
2 Description

The SN74LV139A devices are dual 2-line to 4-line decoders/demultiplexers designed for 2V to 5.5V V_{CC} operation.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LV139A	D (SOIC, 16)	9.90 mm × 6mm	9.90 mm × 3.91 mm
	DB (SSOP, 16)	6.20mm × 7.8mm	6.20 mm × 5.30 mm
	DGV (TVSOP, 16)	3.6mm × 6.4mm	3.6mm × 4.4mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00 mm × 4.40 mm
	NS (SOP, 16)	10.2mm x 7.8mm	10.20 mm x 5.30 mm
	RGY (VQFN, 16)	4.00 mm × 3.50 mm	4.00 mm × 3.50 mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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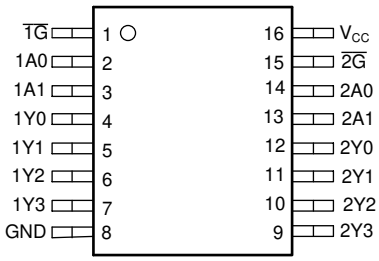
3 Pin Configuration and Functions



SN74LV139A D, DB, DGV, NS, OR PW Package; 16-Pin SOIC, SSOP, TVSOP, SOP, or TSSOP(Top View)

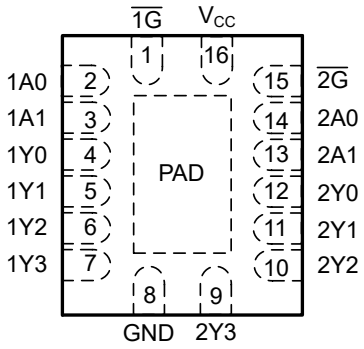


Figure 3-1. SN74LV139A RGY Package, 16-Pin VQFN

Table 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{1G}$	I	Channel 1, output enable, active low
2	$1A_0$	I	Channel 1, address select 0
3	$1A_1$	I	Channel 1, address select 1
4	$1Y_0$	O	Channel 1, output 0
5	$1Y_1$	O	Channel 1, output 1
6	$1Y_2$	O	Channel 1, output 2
7	$1Y_3$	O	Channel 1, output 3
8	GND	—	Ground
9	$2Y_3$	O	Channel 2, output 3
10	$2Y_2$	O	Channel 2, output 2
11	$2Y_1$	O	Channel 2, output 1
12	$2Y_0$	O	Channel 2, output 0
13	$2A_1$	I	Channel 2, address select 1
14	$2A_0$	I	Channel 2, address select 0
15	$\overline{2G}_0$	I	Channel 2, output enable, active low
16	V_{CC}	—	Positive supply

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I (2)	Input voltage range		–0.5	7	V
V_O (2)	Voltage range applied to any output in the high-impedance or power-off state		–0.5	7	V
V_O (2) (3)	Output voltage range		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74LV138A		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	

over operating free-air temperature range (unless otherwise noted)(1)

			SN74LV138A		UNIT
			MIN	MAX	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC(1)		SN74LV139A						UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		16 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	82	120	64	108	39	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN74LV139A			UNIT
				MIN	TYP	MAX	
V_{OH}	High-Level Output Voltage	I_{OH} = –50µA	2V to 5.5V	V_{CC} – 0.1			V
		I_{OH} = –2mA	2.3V	2			
		I_{OH} = –6mA	3V	2.48			
		I_{OH} = –12mA	4.5V	3.8			
V_{OL}	Low-Level Output Voltage	I_{OL} = 50µA	2V to 5.5V			0.1	V
		I_{OL} = 2mA	2.3V			0.4	
		I_{OL} = 6mA	3V			0.44	
		I_{OL} = 12mA	4.5V			0.55	
I_I	Input Current	V_I = 5.5V or GND	0 to 5.5V			±1	µA
I_{CC}	Supply Current	V_I = V_{CC} or GND, I_O = 0	5.5V			20	µA
I_{off}	Input/Output Power-Off Leakage Current	V_I or V_O = 0 to 5.5V	0			5	µA
C_i	Input Capacitance	V_I = V_{CC} or GND	3.3V		1.9		pF

4.6 Switching Characteristics, V_{CC} = 2.5V ± 0.2V

over recommended operating free-air temperature range, V_{CC} = 2.5V ± 0.2V (unless otherwise noted) (see Load Circuits and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	C_L = 15pF		7.7(1)	17.6(1)	1	21	ns
	$\overline{G}$				7.4(1)	15.8(1)	1	19	
t_{pd}	A or B	Y	C_L = 50pF		10.2	22.5	1	26.5	ns
	$\overline{G}$				9.9	20.2	1	24	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.7 Switching Characteristics, V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted) (see Load Circuits and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	C_L = 15pF		5.3(1)	11(1)	1	13	ns
	$\overline{G}$				5.1(1)	9.2(1)	1	11	
t_{pd}	A or B	Y	C_L = 50pF		7.3	14.5	1	16.5	ns
	$\overline{G}$				7	12.7	1	14.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.8 Switching Characteristics, V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see Load Circuits and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	C_L = 15pF		3.7(1)	7.2(1)	1	8.5	ns
	$\overline{G}$				3.5(1)	6.3(1)	1	7.5	
t_{pd}	A or B	Y	C_L = 50pF		5.2	9.2	1	10.5	ns
	$\overline{G}$				4.9	8.3	1	9.5	

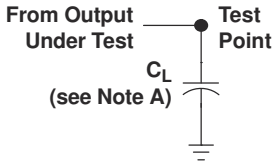
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.9 Operating Characteristics

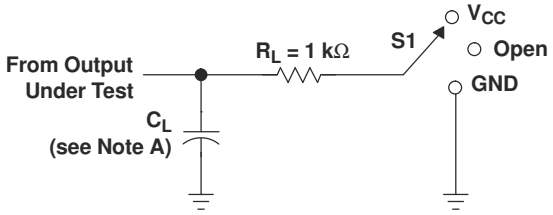
T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	17.3	pF
			5 V	18.2	

5 Parameter Measurement Information

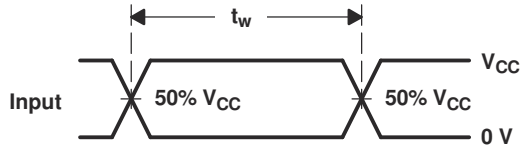


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

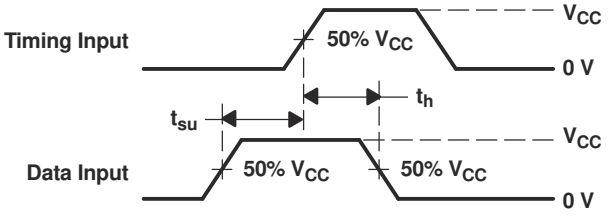


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

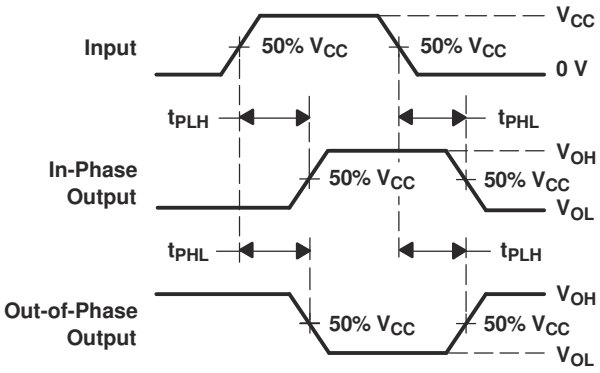
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



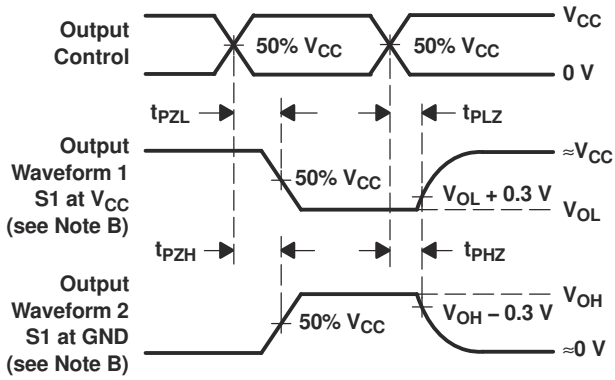
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuits and Voltage Waveforms

6 Detailed Description

6.1 Overview

The SNx4LV139A devices are 3-line to 8-line decoders/demultiplexers designed for 2 V to 5.5 V V_{CC} operation.

These devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The ’LV139A devices comprise two individual 2-line to 4-line decoders in a single package. The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

6.2 Functional Block Diagram

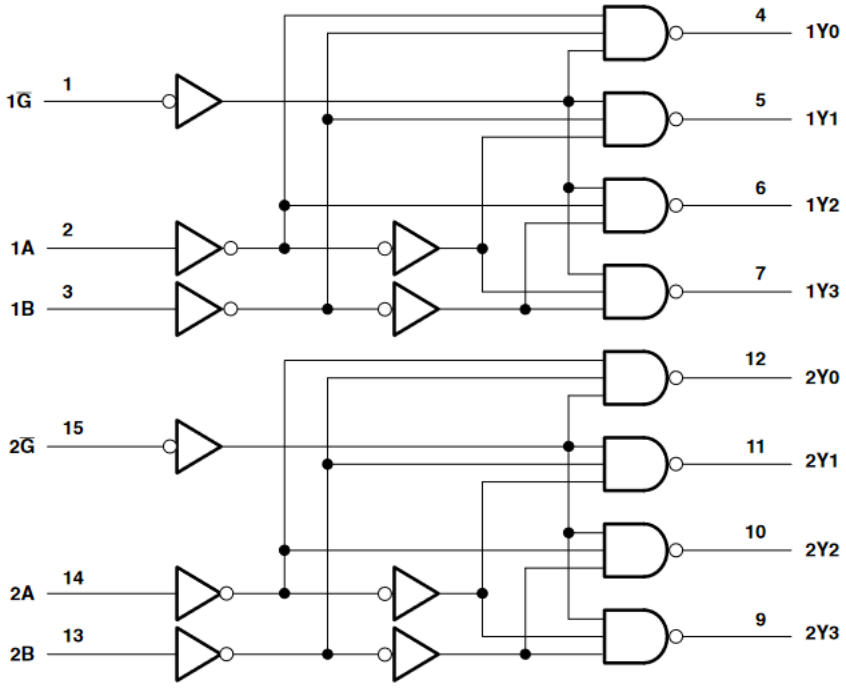


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Function Table

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H

Function Table (continued)

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
L	H	H	H	H	H	L

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

7.2.2 Layout Example

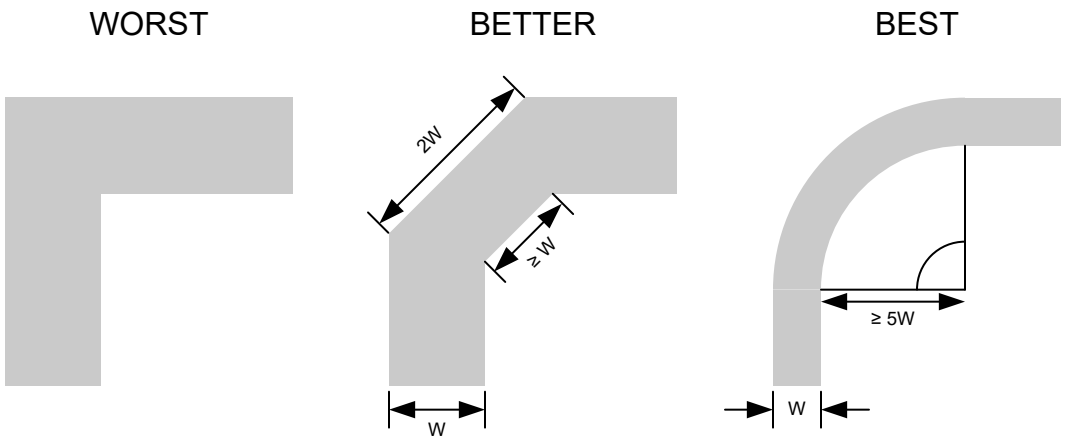


Figure 7-1. Example Trace Corners for Improved Signal Integrity

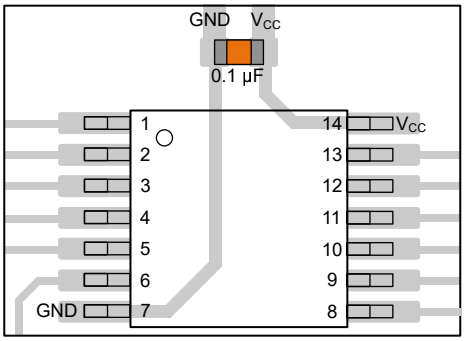


Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages

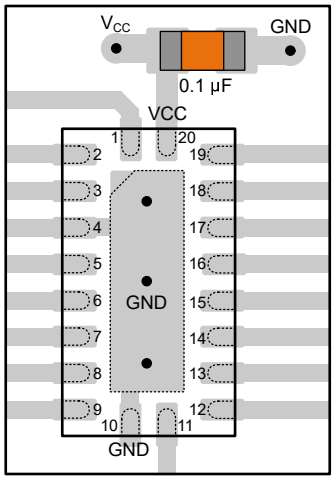


Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages

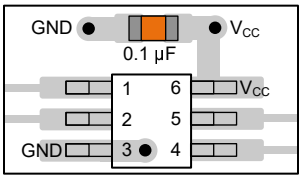


Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

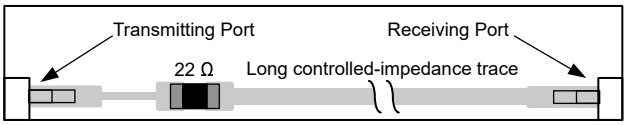


Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision I (April 2005) to Revision J (December 2024)	Page
• Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,* Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted references to machine model	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV139AD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	LV139A
SN74LV139ADBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139ADBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139ANSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV139A
SN74LV139ANSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV139A
SN74LV139ANSRE4	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV139A
SN74LV139APW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	LV139A
SN74LV139APWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139APWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139APWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139APWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139APWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139APWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A
SN74LV139ARGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV139A
SN74LV139ARGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV139A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

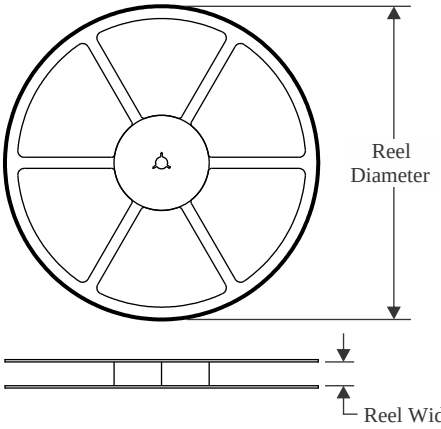
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

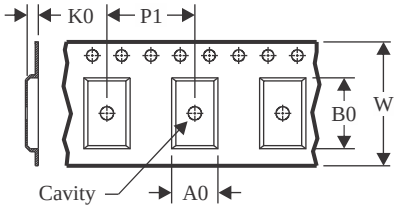
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

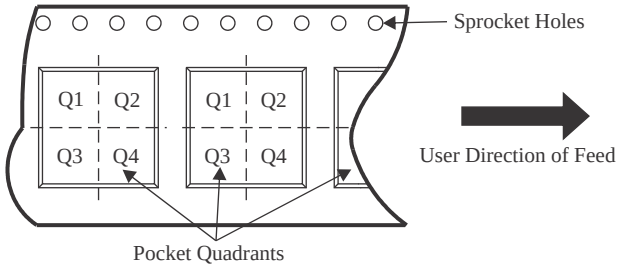


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

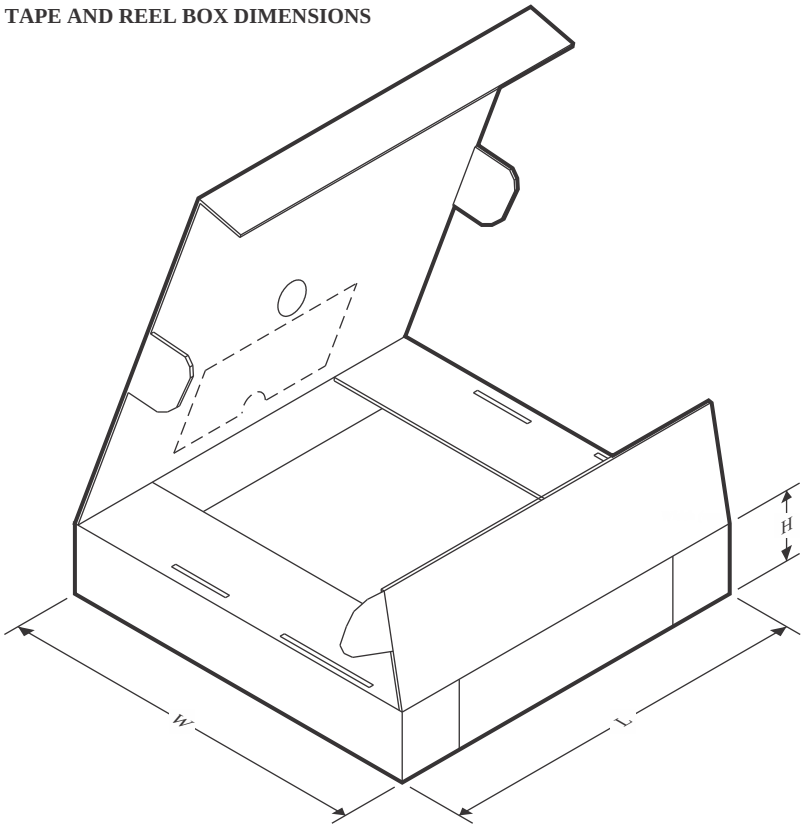
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

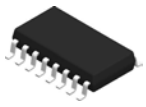
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV139ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV139ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV139ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV139APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV139APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV139ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV139ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LV139ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV139ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LV139APWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV139APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV139ARGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

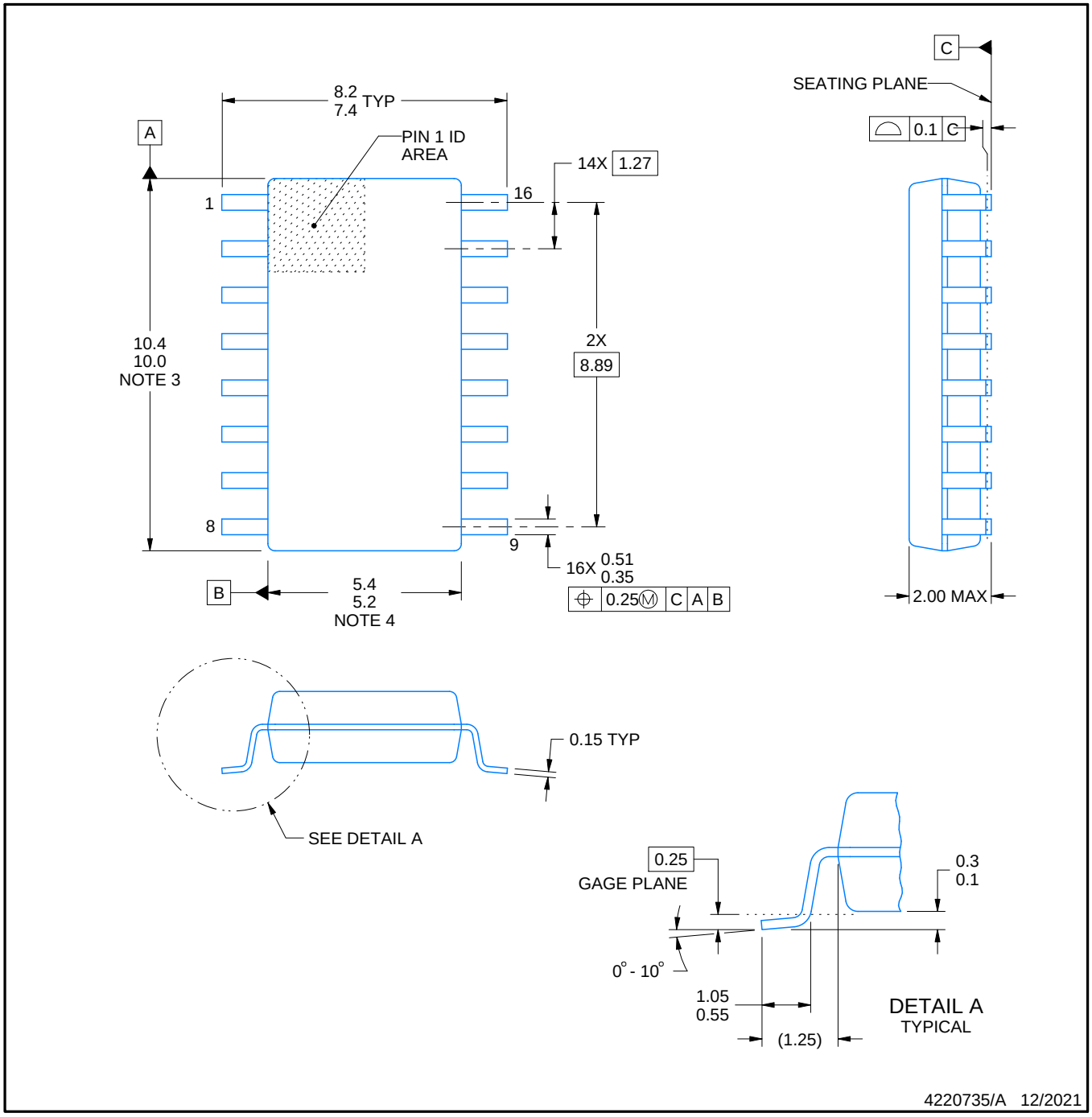


PACKAGE OUTLINE

NS0016A

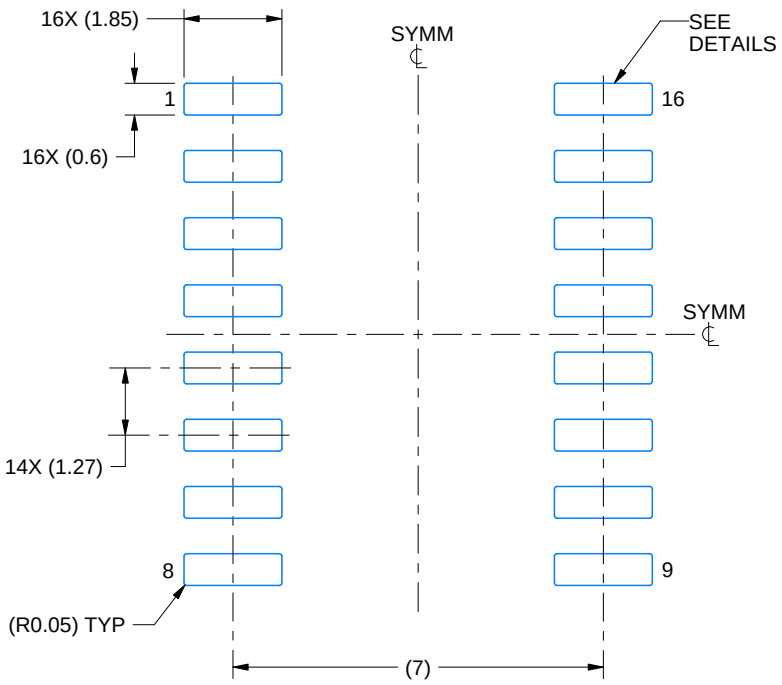
SOP - 2.00 mm max height

SOP

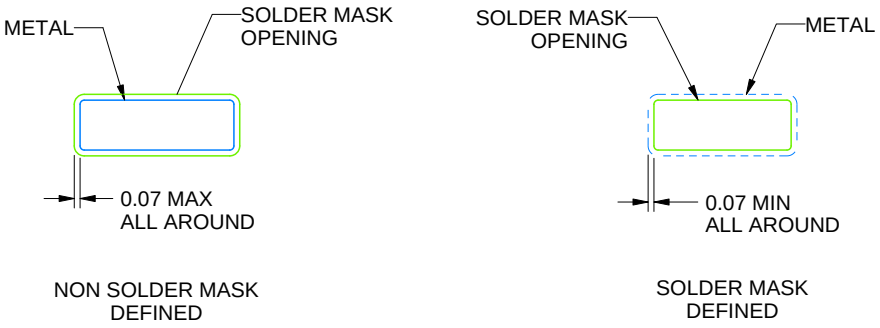


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

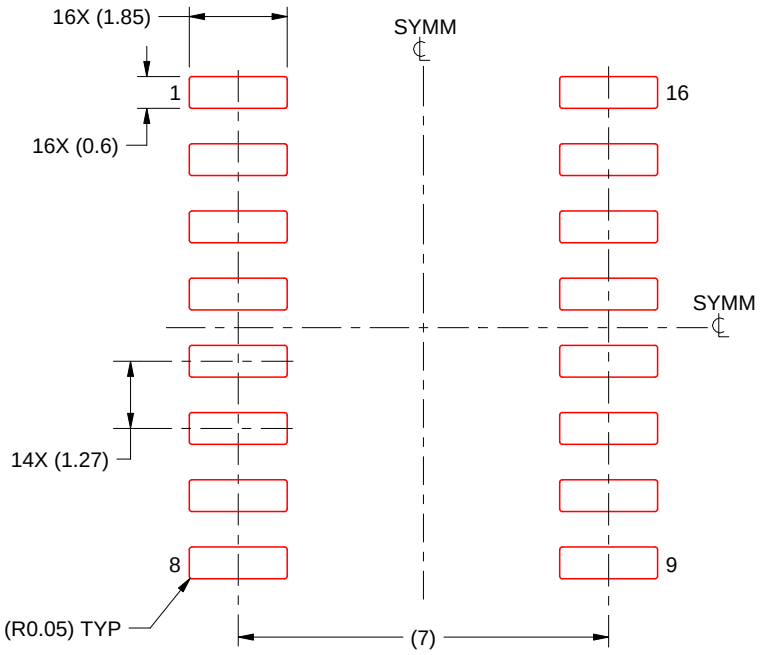
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



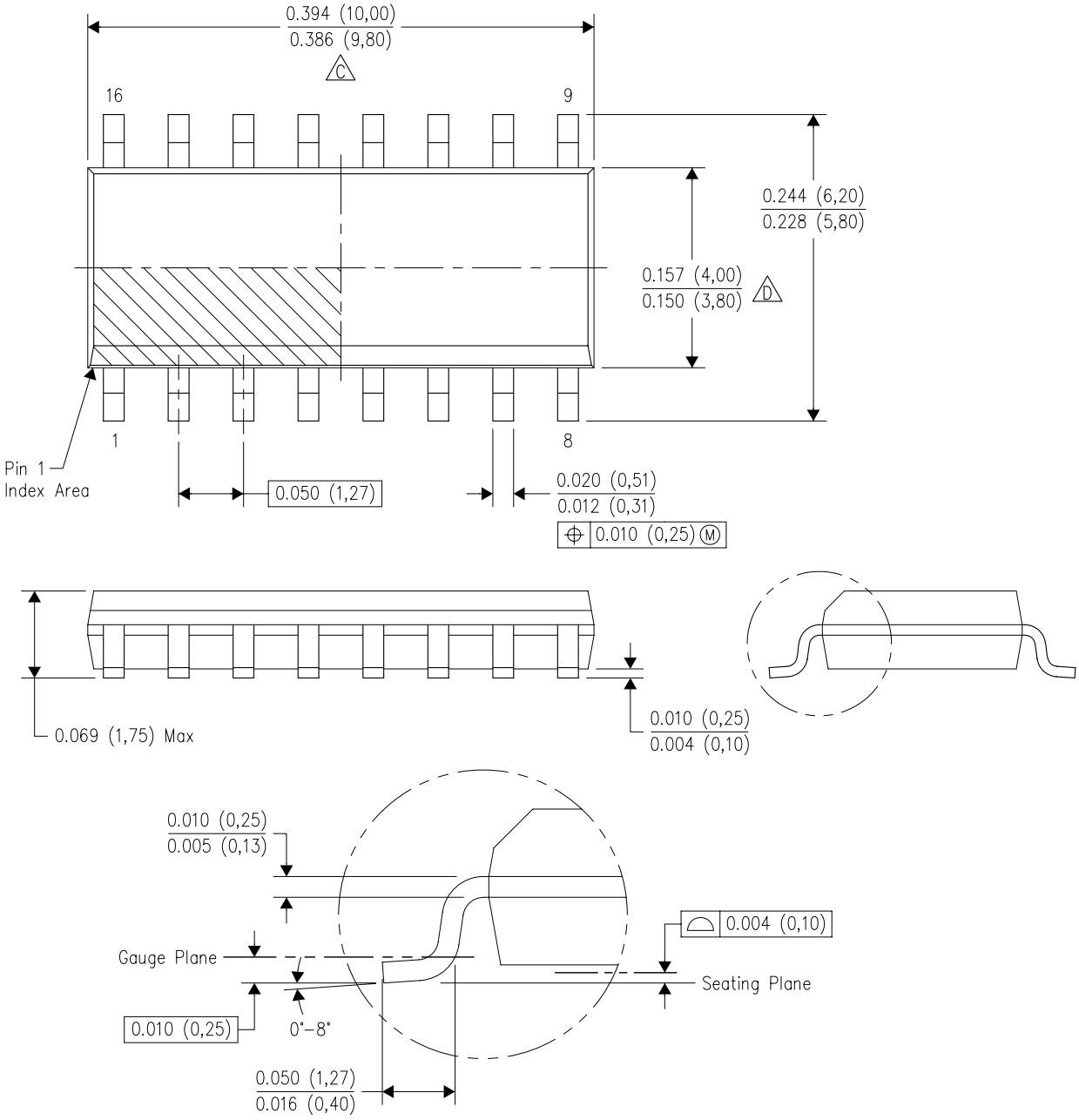
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



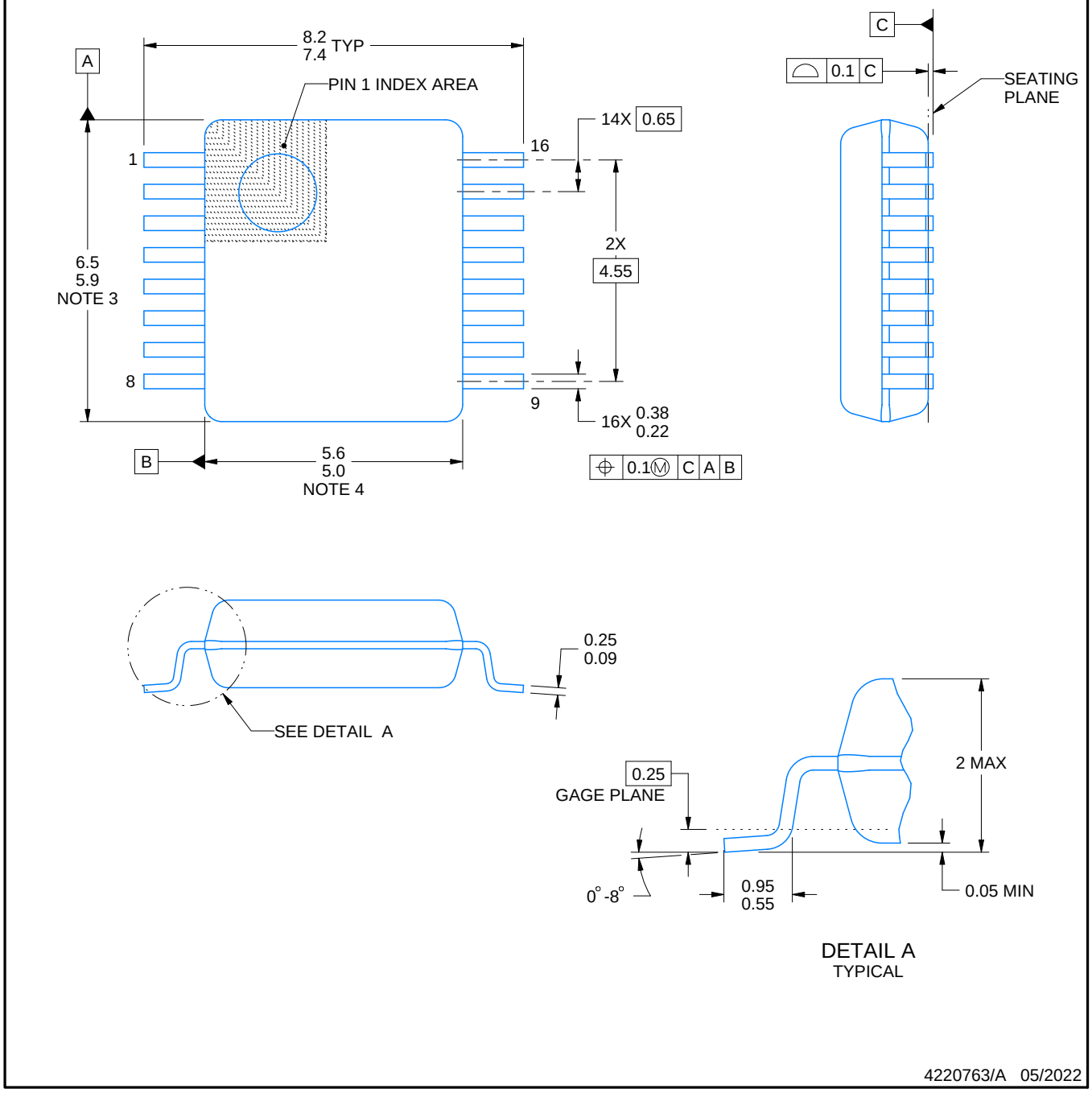
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

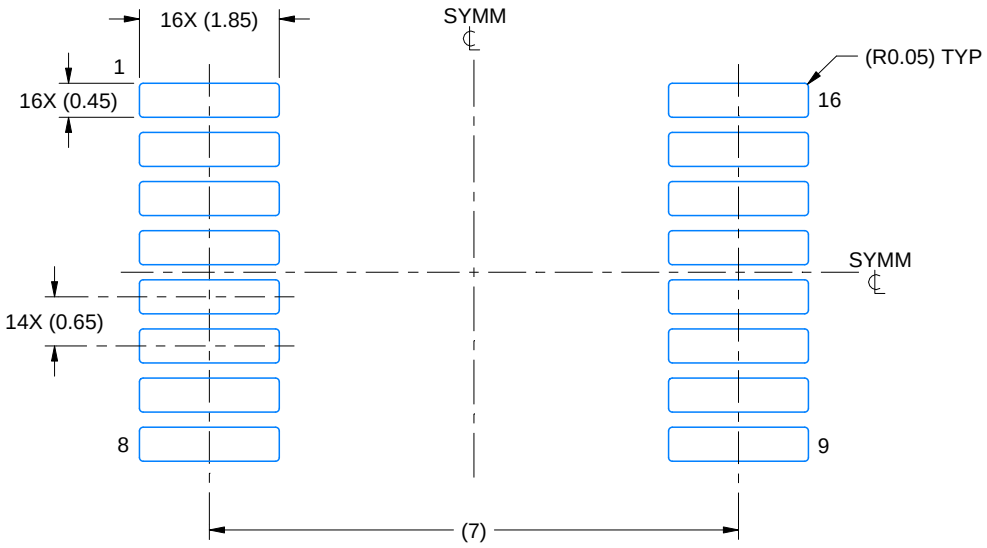
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

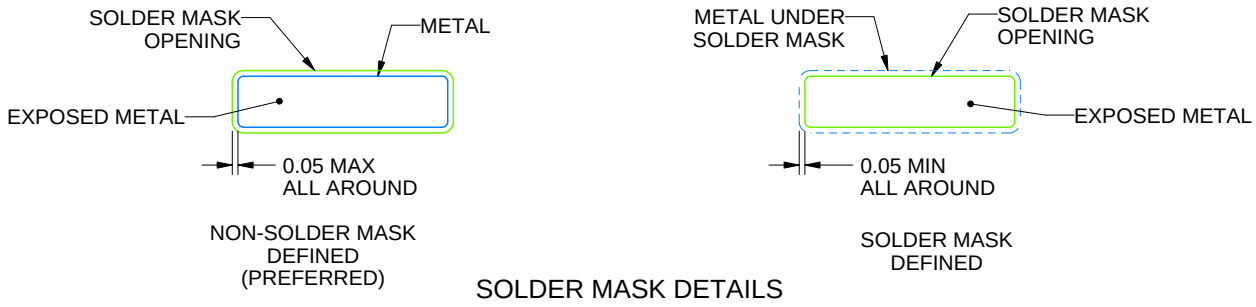


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

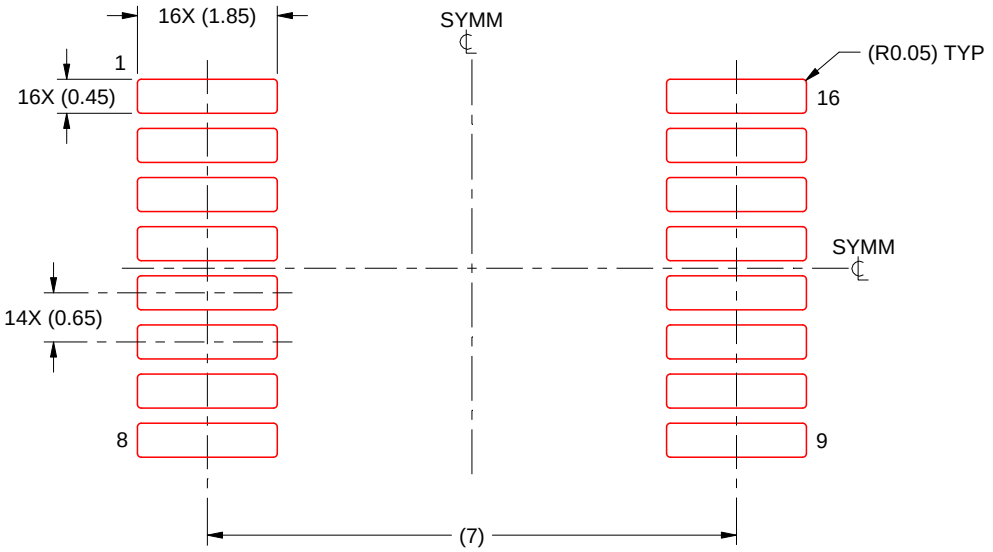


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

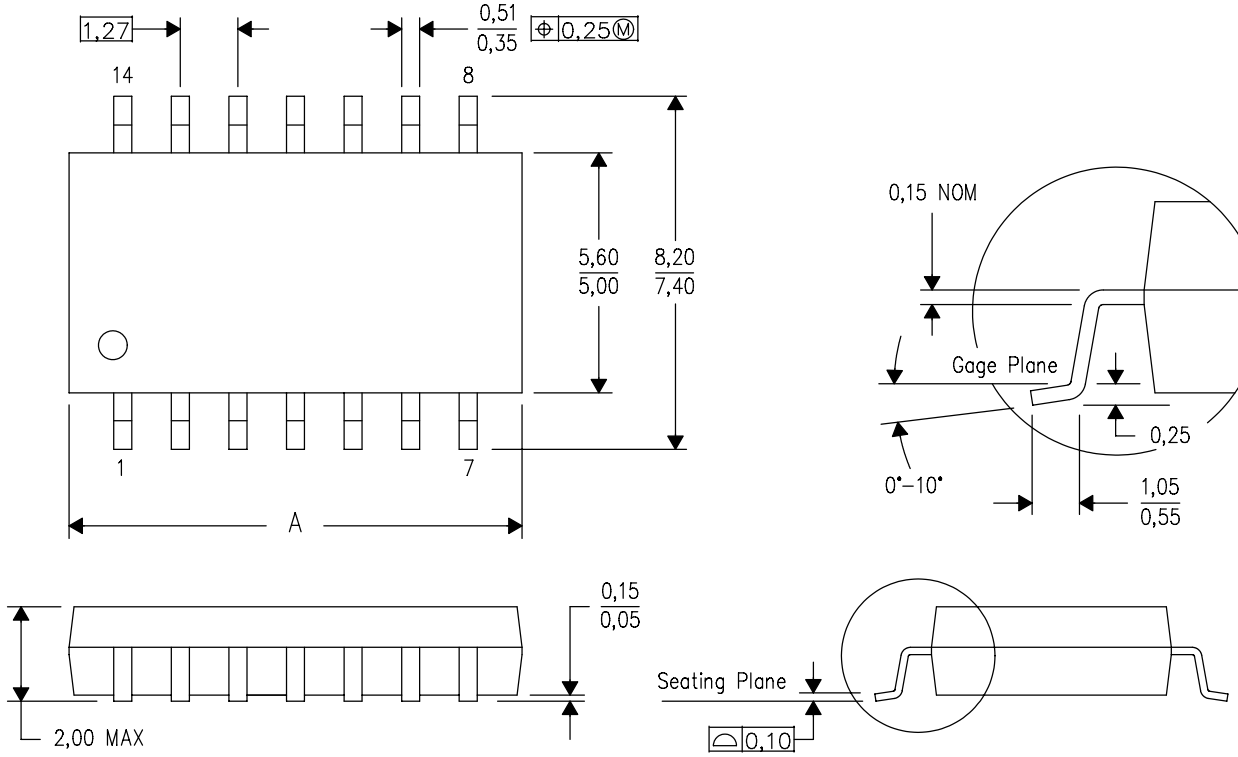
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

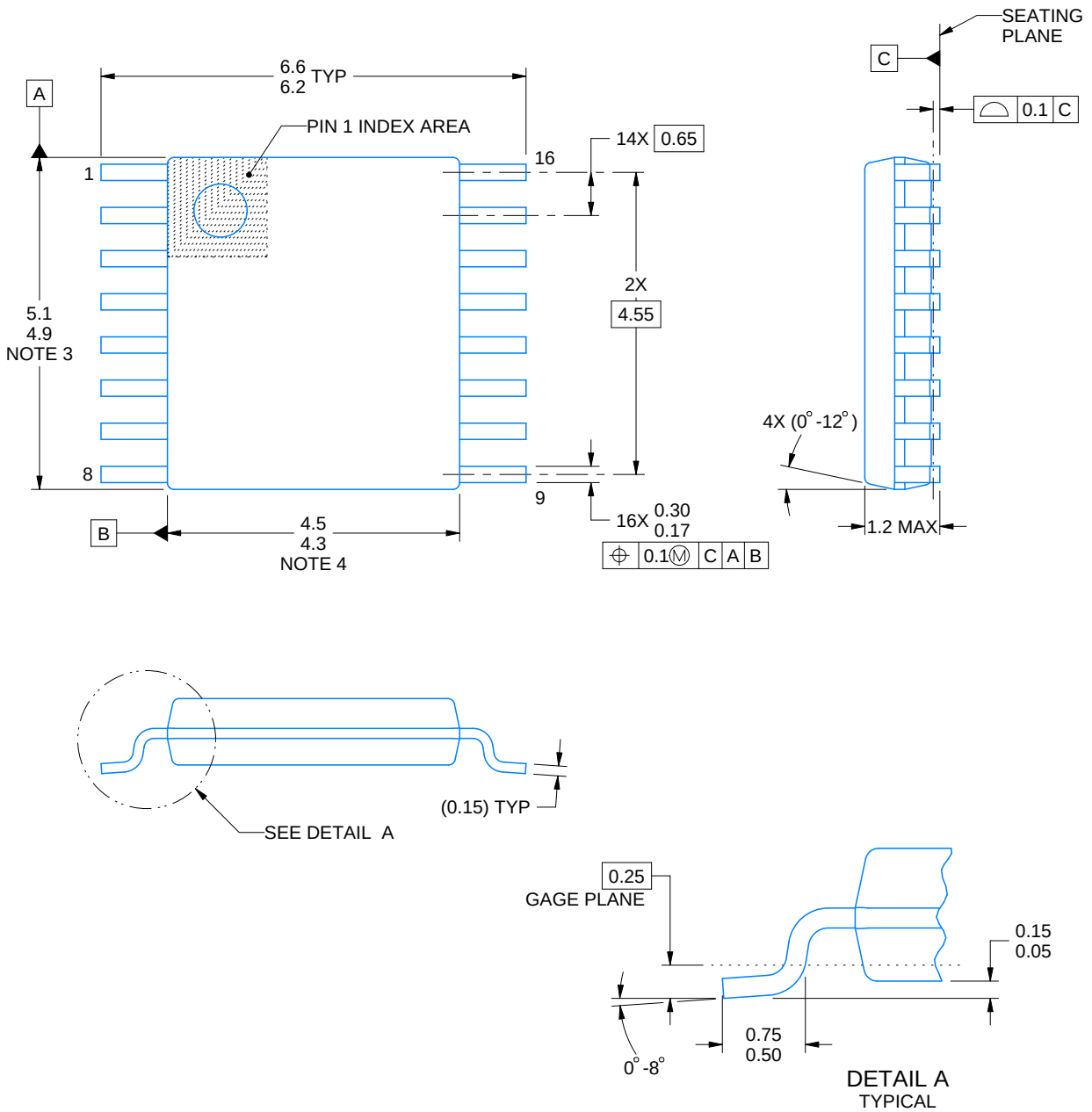
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

PW0016A

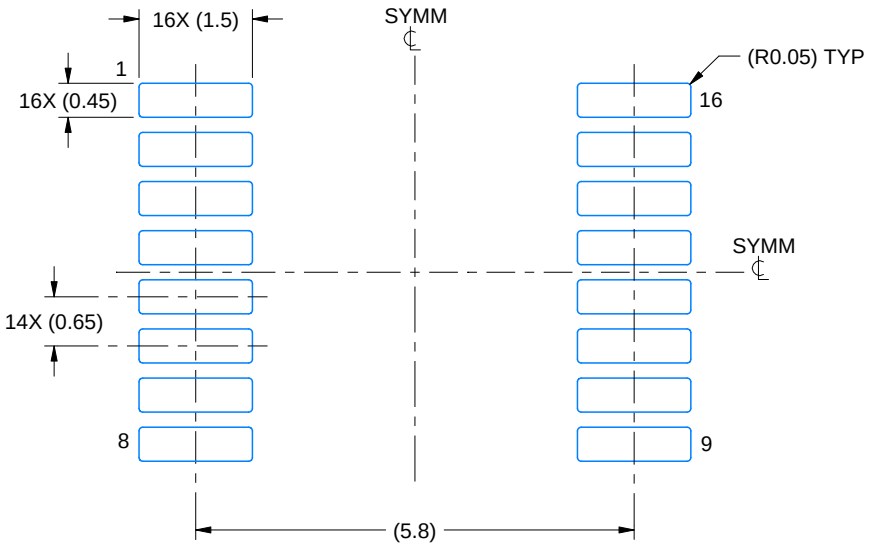
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



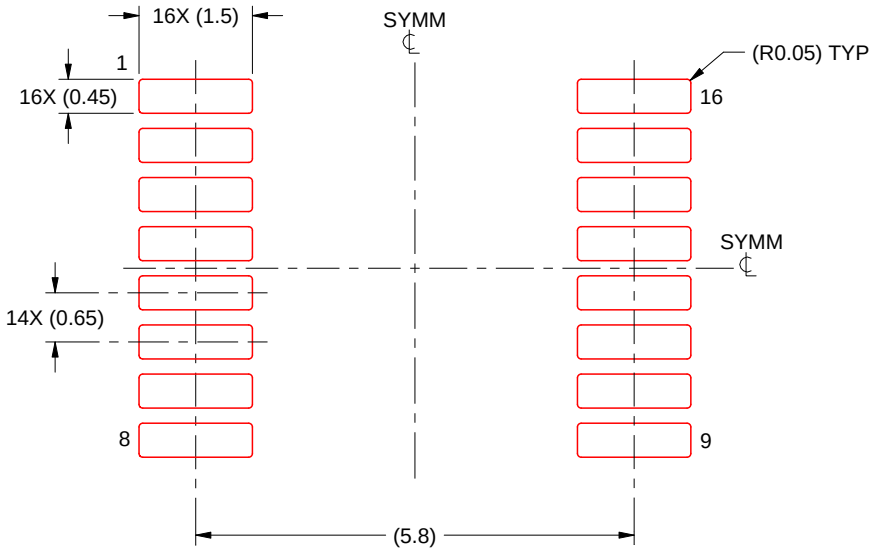
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



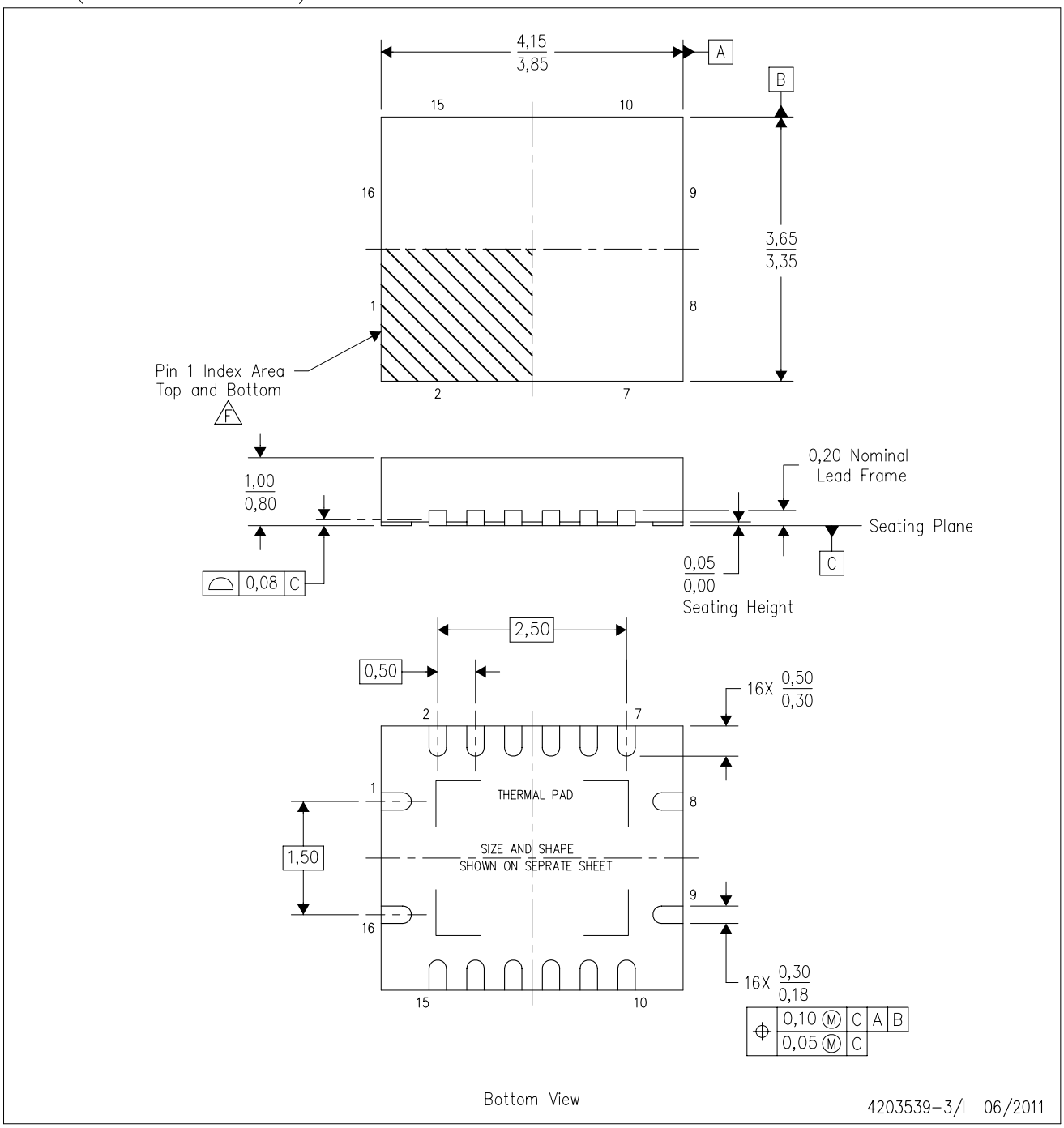
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

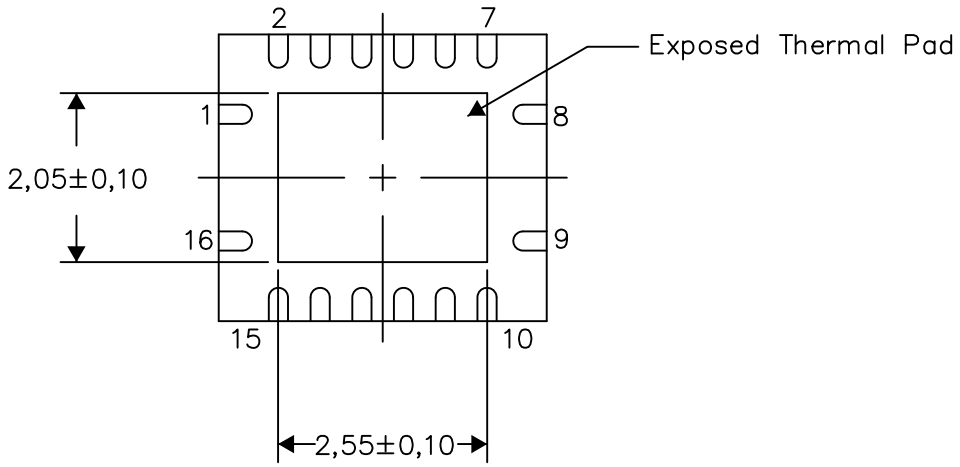
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



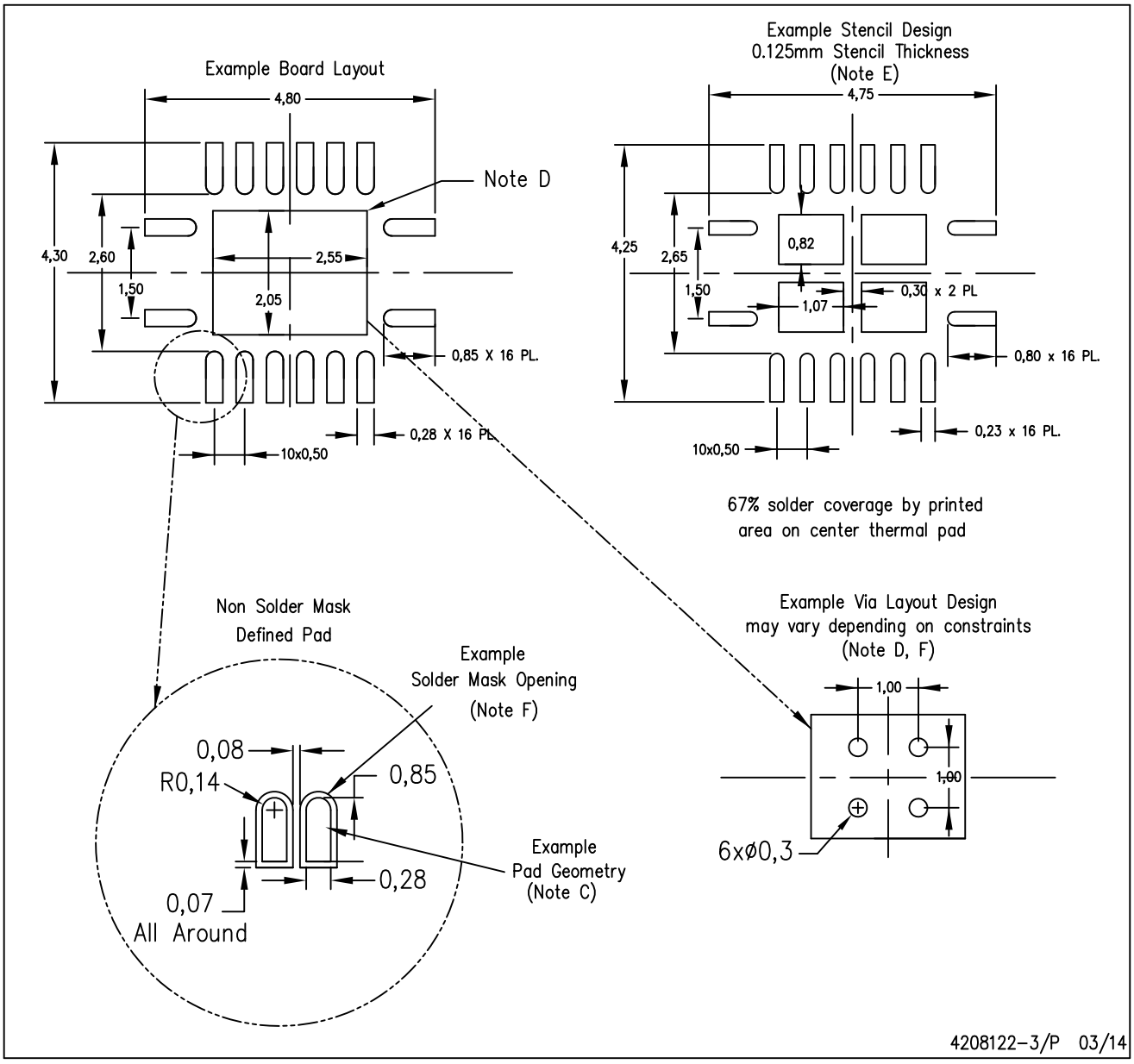
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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