LMC6001 Ultra Ultra-Low Input Current Amplifier

Check for Samples: LMC6001

FEATURES

- **(Max limit, 25°C unless otherwise noted)**
- **Input Current (100% tested): 25 fA**
- **Input Current over Temp.: 2 pA**
- **Low Power: 750 µA**
- **Low V_{OS}: 350 µV**
- **Low Noise: 22 nV/√Hz @1 kHz Typ.**

APPLICATIONS

- **Electrometer Amplifier**
- **Photodiode Preamplifier**
- **Ion Detector**
- **A.T.E. Leakage Testing**

DESCRIPTION

Featuring 100% tested input currents of 25 fA max., low operating power, and ESD protection of 2000V, the LMC6001 achieves a new industry benchmark for low input current operational amplifiers. By tightly controlling the molding compound, Texas Instruments is able to offer this ultra-low input current in a lower cost molded package.

To avoid long turn-on settling times common in other low input current opamps, the LMC6001A is tested 3 times in the first minute of operation. Even units that meet the 25 fA limit are rejected if they drift.

Because of the ultra-low input current noise of 0.13 fA/√Hz, the LMC6001 can provide almost noiseless amplification of high resistance signal sources. Adding only 1 dB at 100 kΩ, 0.1 dB at 1 MΩ and 0.01 dB or less from 10 MΩ to 2,000 MΩ, the LMC6001 is an almost noiseless amplifier.

The LMC6001 is ideally suited for electrometer applications requiring ultra-low input leakage such as sensitive photodetection transimpedance amplifiers and sensor amplifiers. Since input referred noise is only 22 nV/√Hz, the LMC6001 can achieve higher signal to noise ratio than JFET input type electrometer amplifiers. Other applications of the LMC6001 include long interval integrators, ultra-high input impedance instrumentation amplifiers, and sensitive electrical-field measurement circuits.

Connection Diagram

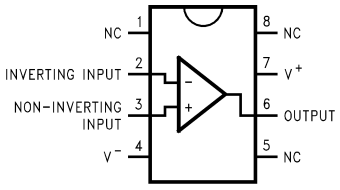

Figure 1. 8-Pin PDIP (Top View)
See P Package

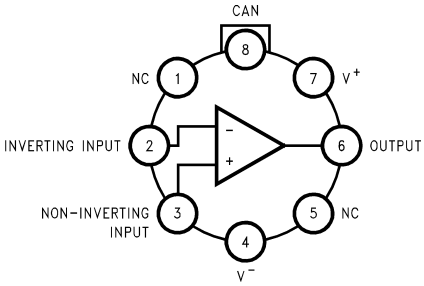

Figure 2. 8-Pin TO-99 (Top View)
See LMC Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Absolute Maximum Ratings[1][2]

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Supply Voltage $(V^+ - V^-)$	−0.3V to +16V
Output Short Circuit to V^+	See[3][4]
Output Short Circuit to V^-	See[3]
(Soldering, 10 Sec.) Lead Temperature	260°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	See[5]
ESD Tolerance[5]	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Do not connect the output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.
(5) Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings[1]

Temperature Range (LMC6001AI, LMC6001BI, LMC6001CI)		$-40°C \le T_J \le +85°C$
Supply Voltage		$4.5V \le V^+ \le 15.5V$
Thermal Resistance[2]	θ_{JA}, P Package	100°C/W
	θ_{JA}, LMC Package	145°C/W
	θ_{JC}, LMC Package	45°C/W
Power Dissipation		See[3]

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
(2) All numbers apply for packages soldered directly into a printed circuit board.
(3) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

DC Electrical Characteristics

Limits in standard typeface guaranteed for T_J = 25°C and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, and R_L > 1M.

Symbol	Parameter	Conditions	Typical(1)	Limits(2)			Units
				LMC6001AI	LMC6001BI	LMC6001CI	
I_B	Input Current	Either Input, V_{CM} = 0V, V_S = ±5V	10	25 **2000**	100 **4000**	1000 **4000**	fA
I_{OS}	Input Offset Current		5	**1000**	**2000**	**2000**	
V_{OS}	Input Offset Voltage			0.35 **1.0**	1.0 **1.7**	1.0 **2.0**	mV
		V_S = ±5V, V_{CM} = 0V		0.7 **1.35**	1.35 **2.0**	1.35	
TCV_{OS}	Input Offset Voltage Drift		2.5	10	10		µV/°C
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 7.5V V^+ = 10V	83	75 **72**	72 **68**	66 **63**	dB min
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V	83	73 **70**	66 **63**	66 **63**	
−PSRR	Negative Power Supply Rejection Ratio	0V ≥ V^- ≥ −10V	94	80 **77**	74 **71**	74 **71**	
A_V	Large Signal Voltage Gain	Sourcing, R_L = 2 kΩ(3)	1400	400 **300**	300 **200**	300 **200**	V/mV min
		Sinking, R_L = 2 kΩ(3)	350	180 **100**	90 **60**	90 **60**	
V_{CM}	Input Common-Mode Voltage	V^+ = 5V and 15V For CMRR ≥ 60 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
			V^+ − 1.9	V^+ − 2.3 **V^+ − 2.5**	V^+ − 2.3 **V^+ − 2.5**	V^+ − 2.3 **V^+ − 2.5**	V min
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.80 **4.73**	4.75 **4.67**	4.75 **4.67**	V min
			0.10	0.14 **0.17**	0.20 **0.24**	0.20 **0.24**	V max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	14.50 **14.34**	14.37 **14.25**	14.37 **14.25**	V min
			0.26	0.35 **0.45**	0.44 **0.56**	0.44 **0.56**	V max
I_O	Output Current	Sourcing, V^+ = 5V, V_O = 0V	22	16 **10**	13 **8**	13 **8**	mA min
		Sinking, V^+ = 5V, V_O = 5V	21	16 **13**	13 **10**	13 **10**	
		Sourcing, V^+ = 15V, V_O = 0V	30	28 **22**	23 **18**	23 **18**	
		Sinking, V^+ = 15V, V_O = 13V(4)	34	28 **22**	23 **18**	23 **18**	

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.
(4) Do not connect the output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

DC Electrical Characteristics (continued)

Limits in standard typeface guaranteed for T_J = 25°C and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, and R_L > 1M.

Symbol	Parameter	Conditions	Typical[1]	Limits[2]			Units
				LMC6001AI	LMC6001BI	LMC6001CI	
I_S	Supply Current	V^+ = 5V, V_O = 1.5V	450	750 **900**	750 **900**	750 **900**	µA max
		V^+ = 15V, V_O = 7.5V	550	850 **950**	850 **950**	850 **950**	

AC Electrical Characteristics

Limits in standard typeface guaranteed for T_J = 25°C and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V and R_L > 1M.

Symbol	Parameter	Conditions	Typical[1]	Limits[2]			Units
				LM6001AI	LM6001BI	LM6001CI	
SR	Slew Rate	See[3]	1.5	0.8 **0.6**	0.8 **0.6**	0.8 **0.6**	V/µs min
GBW	Gain-Bandwidth Product		1.3				MHz
φf_m	Phase Margin		50				Deg
G_M	Gain Margin		17				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.13				fA/√Hz
THD	Total Harmonic Distortion	F = 10 kHz, A_V = −10, R_L = 100 kΩ, V_O = 8 V_{PP}	0.01				%

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) V^+ = 15V. Connected as Voltage Follower with 10V step input. Limit specified is the lower of the positive and negative slew rates.

Typical Performance Characteristics

V_S = ±7.5V, T_A = 25°C, unless otherwise specified

Input Current vs. Temperature

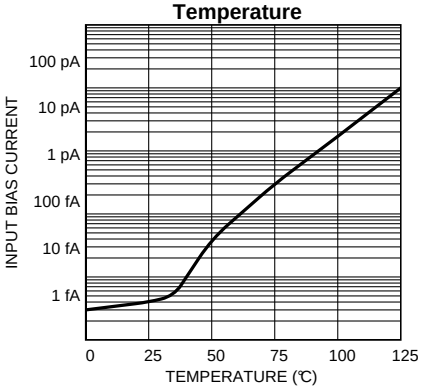


Figure 3.

Input Current vs. V_{CM} V_S = ±5V

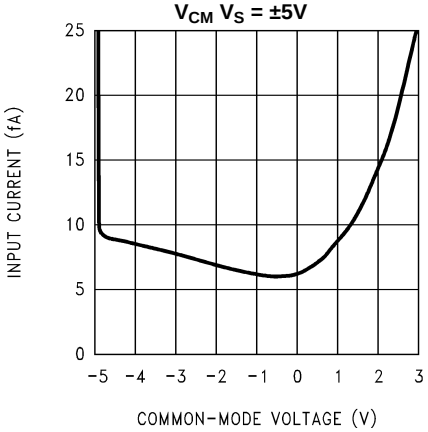


Figure 4.

Supply Current vs. Supply Voltage

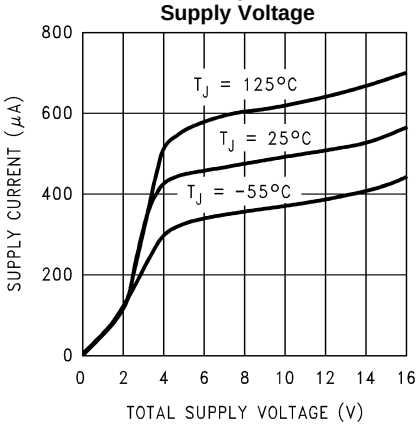


Figure 5.

Input Voltage vs.Output Voltage

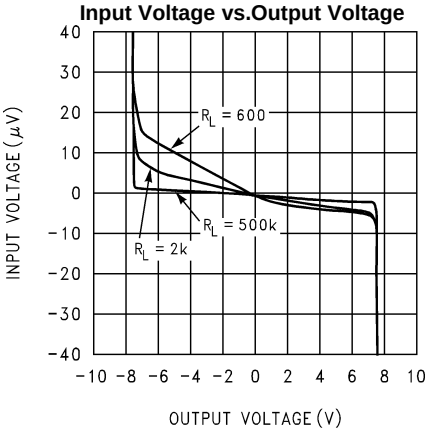


Figure 6.

Common Mode Rejection Ratio vs. Frequency

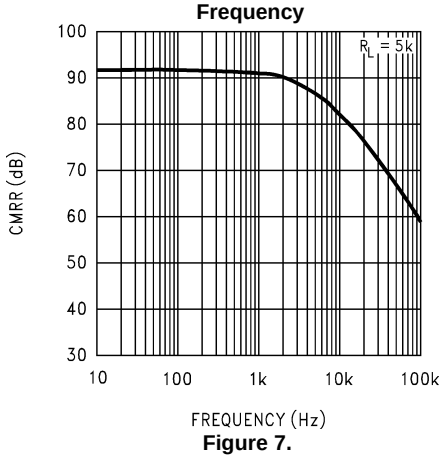


Figure 7.

Power Supply Rejection Ratio vs. Frequency

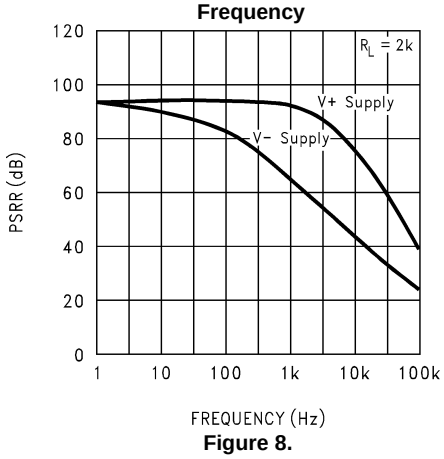


Figure 8.

Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C, unless otherwise specified

Input Voltage Noise vs. Frequency

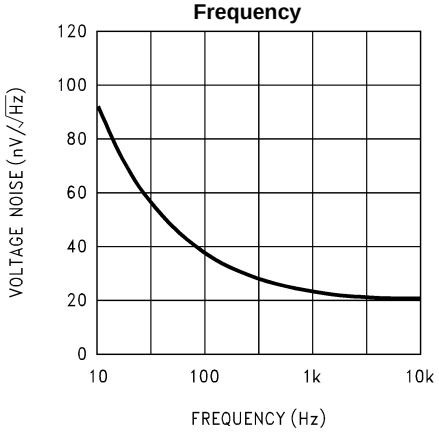


Figure 9.

Noise Figure vs. Source Resistance

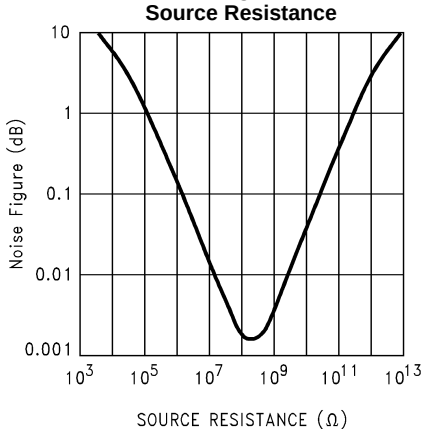


Figure 10.

Output Characteristics Sourcing Current

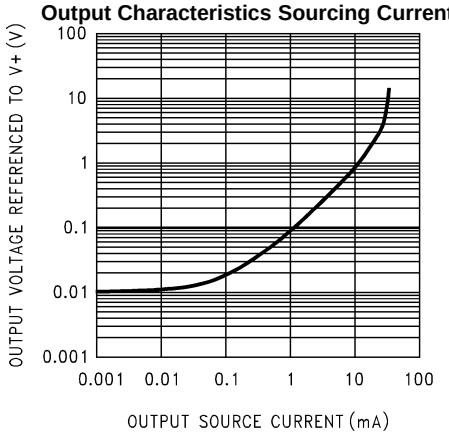


Figure 11.

Output Characteristics Sinking Current

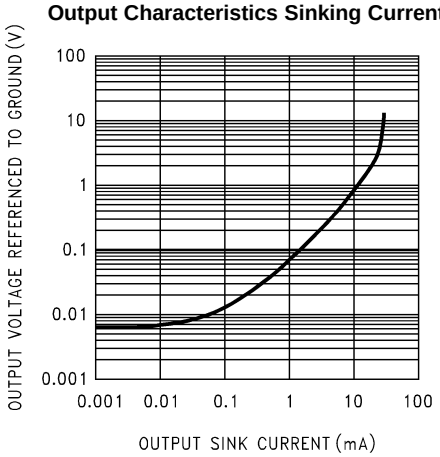


Figure 12.

Gain and Phase Response vs. Temperature (−55°C to +125°C)

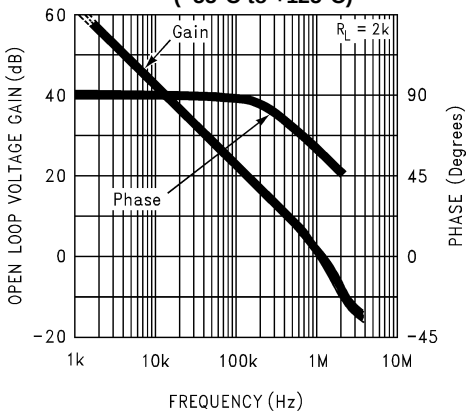


Figure 13.

Gain and Phase Response vs. Capacitive Load with R_L = 500 kΩ

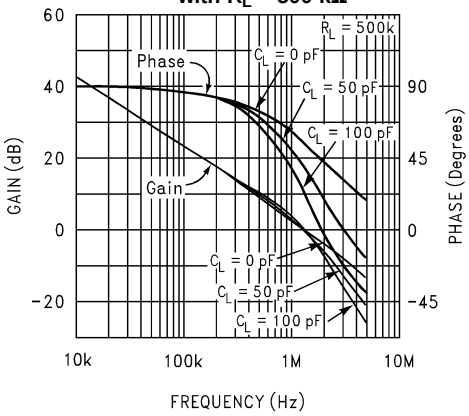


Figure 14.

Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C, unless otherwise specified

Open Loop Frequency Response

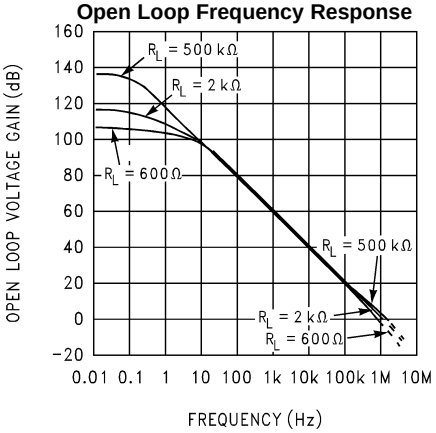


Figure 15.

Inverting Small Signal Pulse Response

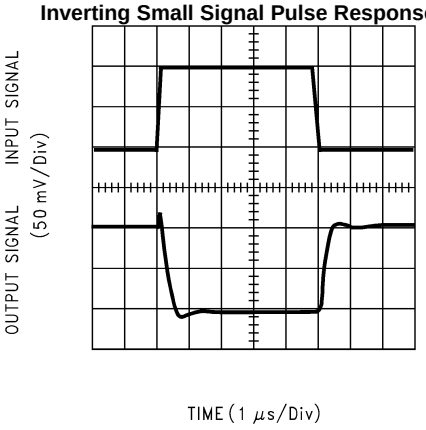


Figure 16.

Inverting Large Signal Pulse Response

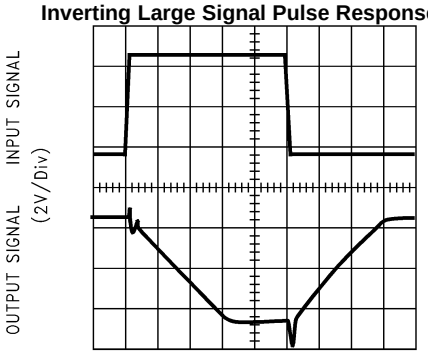


Figure 17.

Non-Inverting Small Signal Pulse Response

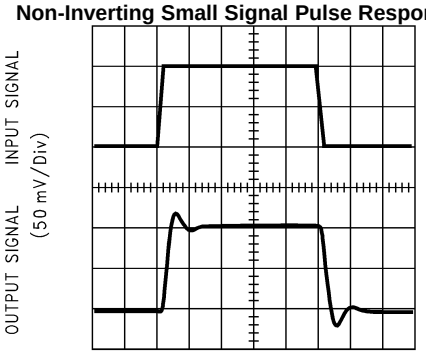


Figure 18.

Non-Inverting Large Signal Pulse Response

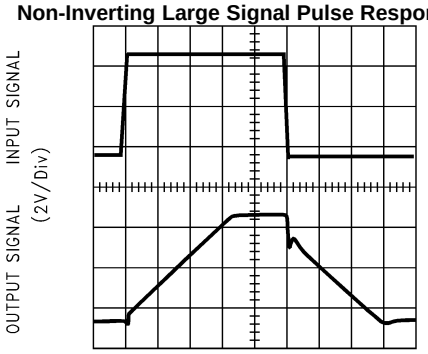


Figure 19.

Stability vs. Capacitive Load

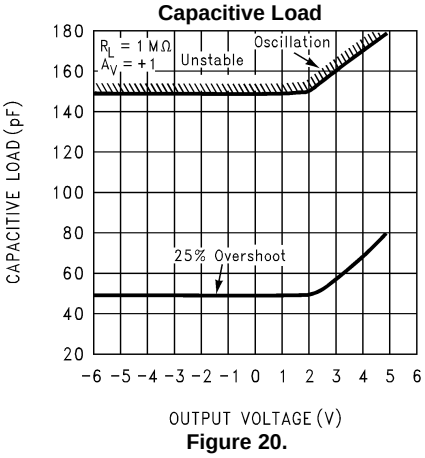


Figure 20.

APPLICATIONS HINTS

AMPLIFIER TOPOLOGY

The LMC6001 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional op-amps. These features make the LMC6001 both easier to design with, and provide higher speed than products typically found in this low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6001.

Although the LMC6001 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6001 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. See PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK.

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in Figure 21) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or

$$R_1\, C_{IN} \leq R_2\, C_f \tag{2}$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

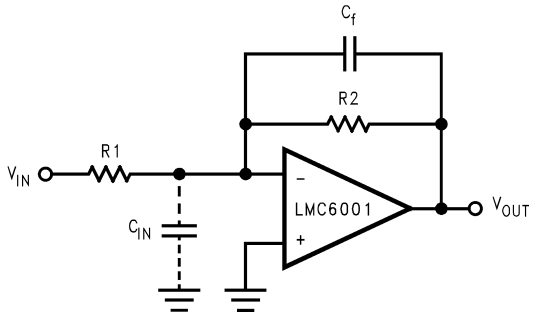


Figure 21. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load. See Typical Performance Characteristics.

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 22.

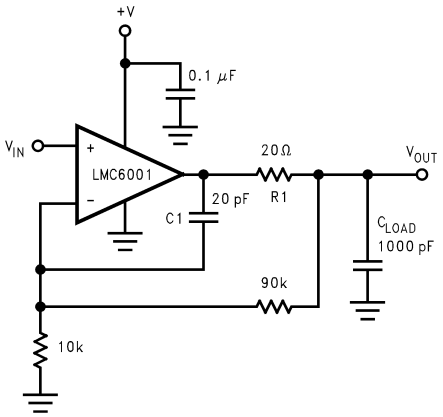


Figure 22. LMC6001 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 22, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pullup resistor to V^+ (Figure 23). Typically a pullup resistor conducting 500 µA or more will significantly improve capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pullup resistor. See DC Electrical Characteristics.

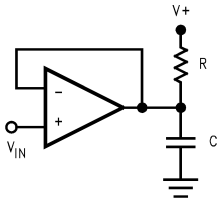


Figure 23. Compensating for Large Capacitive Loads with a Pullup Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6001, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6001's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc., connected to the op-amp's inputs, as in Figure 24. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input.

This would cause a 500 times degradation from the LMC6001's actual performance. If a guard ring is used and held within 1 mV of the inputs, then the same resistance of $10^{12}\Omega$ will only cause 10 fA of leakage current. Even this small amount of leakage will degrade the extremely low input current performance of the LMC6001. See Figure 27 for typical connections of guard rings for standard op-amp configurations.

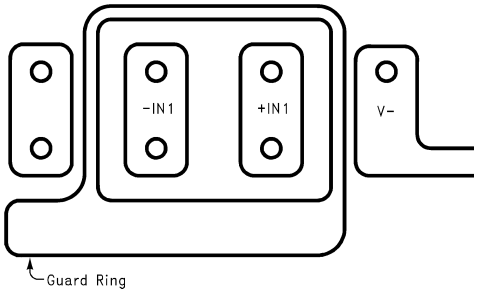


Figure 24. Examples of Guard Ring in PC Board Layout

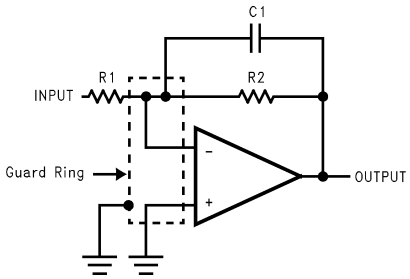


Figure 25. Inverting Amplifier

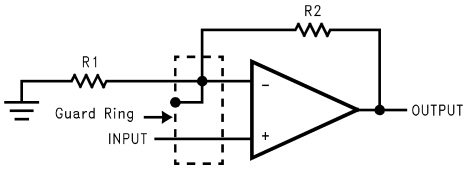


Figure 26. Non-Inverting Amplifier

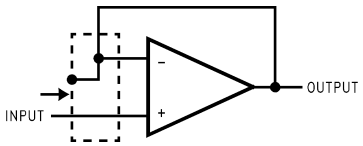
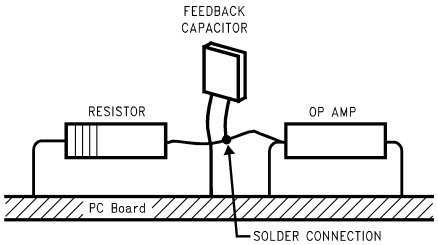


Figure 27. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 28.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

Figure 28. Air Wiring

Another potential source of leakage that might be overlooked is the device package. When the LMC6001 is manufactured, the device is always handled with conductive finger cots. This is to assure that salts and skin oils do not cause leakage paths on the surface of the package. We recommend that these same precautions be adhered to, during all phases of inspection, test and assembly.

LATCHUP

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6001 is designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Applications

The extremely high input resistance, and low power consumption, of the LMC6001 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, electrostatic field detectors and gas chromotographs.

TWO OPAMP, TEMPERATURE COMPENSATED pH PROBE AMPLIFIER

The signal from a pH probe has a typical resistance between 10 MΩ and 1000 MΩ. Because of this high value, it is very important that the amplifier input currents be as small as possible. The LMC6001 with less than 25 fA input current is an ideal choice for this application.

The theoretical output of the standard Ag/AgCl pH probe is 59.16 mV/pH at 25°C with 0V out at a pH of 7.00. This output is proportional to absolute temperature. To compensate for this, a temperature compensating resistor, R1, is placed in the feedback loop. This cancels the temperature dependence of the probe. This resistor must be mounted where it will be at the same temperature as the liquid being measured.

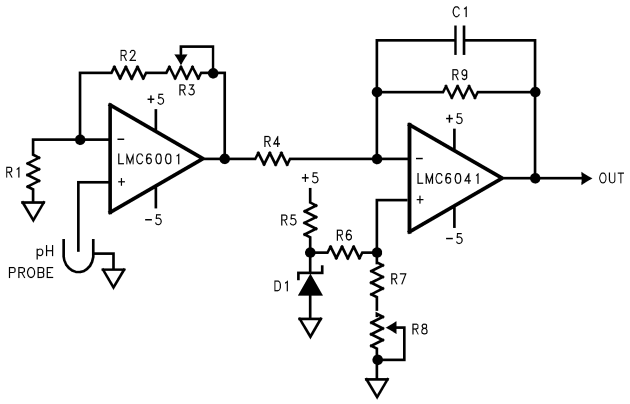
The LMC6001 amplifies the probe output providing a scaled voltage of ±100 mV/pH from a pH of 7. The second opamp, a micropower LMC6041 provides phase inversion and offset so that the output is directly proportional to pH, over the full range of the probe. The pH reading can now be directly displayed on a low cost, low power digital panel meter. Total current consumption will be about 1 mA for the whole system.

The micropower dual operational amplifier, LMC6042, would optimize power consumption but not offer these advantages:

1. The LMC6001A guarantees a 25 fA limit on input current at 25°C.
2. The input ESD protection diodes in the LMC6042 are only rated at 500V while the LMC6001 has much more robust protection that is rated at 2000V.

The setup and calibration is simple with no interactions to cause problems.

1. Disconnect the pH probe and with R3 set to about mid-range and the noninverting input of the LMC6001 grounded, adjust R8 until the output is 700 mV.
2. Apply −414.1 mV to the noninverting input of the LMC6001. Adjust R3 for and output of 1400 mV. This completes the calibration. As real pH probes may not perform exactly to theory, minor gain and offset adjustments should be made by trimming while measuring a precision buffer solution.



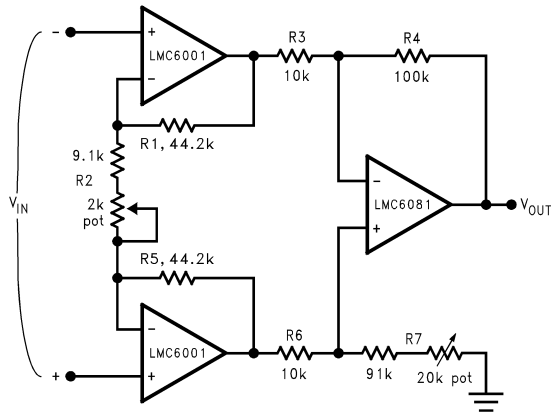
R1 100k + 3500 ppm/°C
R2 68.1k
R3, 8 5k
R4, 9 100k
R5 36.5k
R6 619k
R7 97.6k
D1 LM4040D1Z-2.5
C1 2.2 µF

(1) Micro-ohm style 137 or similar

Figure 29. pH Probe Amplifier

ULTRA-LOW INPUT CURRENT INSTRUMENTATION AMPLIFIER

Figure 30 shows an instrumentation amplifier that features high differential and common mode input resistance (>10^{14}Ω), 0.01% gain accuracy at A_V = 1000, excellent CMRR with 1 MΩ imbalance in source resistance. Input current is less than 20 fA and offset drift is less than 2.5 µV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown (R_2 = 9.85k).

Figure 30. Instrumentation Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMC6001AIN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 85	LMC6001 AIN	Samples
LMC6001AIN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC6001 AIN	Samples
LMC6001BIN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 85	LMC6001 BIN	Samples
LMC6001BIN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC6001 BIN	Samples

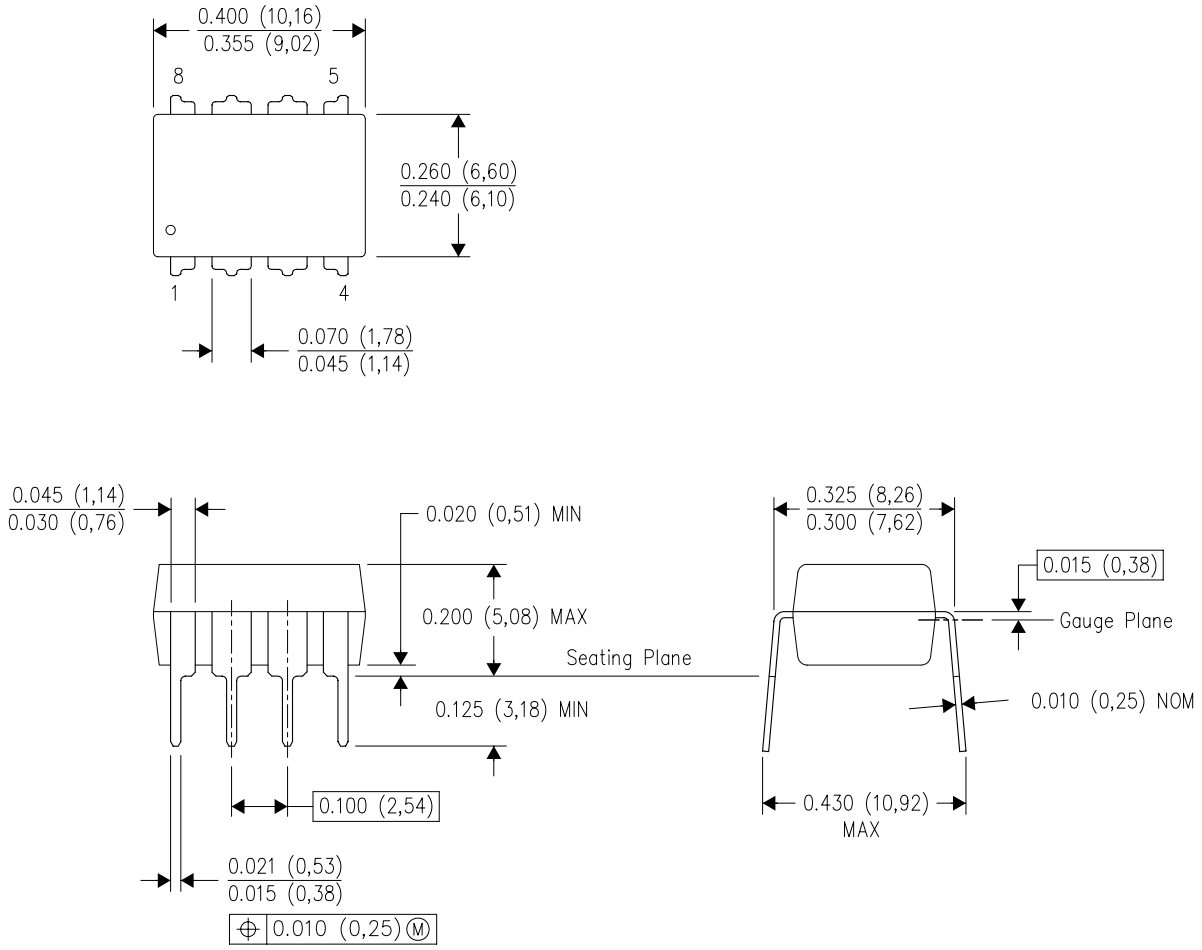
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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