160-DOTS LCD DRIVER WITH CLOCK FUNCTIONS

GENERAL DESCRIPTION

This chip is a LCD driver for a telephone dialer number display or other equipment. A maximum of 20 digits or 160 dots can be displayed, with 1/3 bias, 1/4 duty, and 40 segments.

In normal mode, there are max. 160 dots (can be programmed by μP) can be displayed on the LCD panel. In clock mode, the LCD panel can display a built-in clock that can be read out by μP.

A V_{DD1} pin is used in different voltage system application to implement voltage level shift function so the transceiver data can be guaranteed.

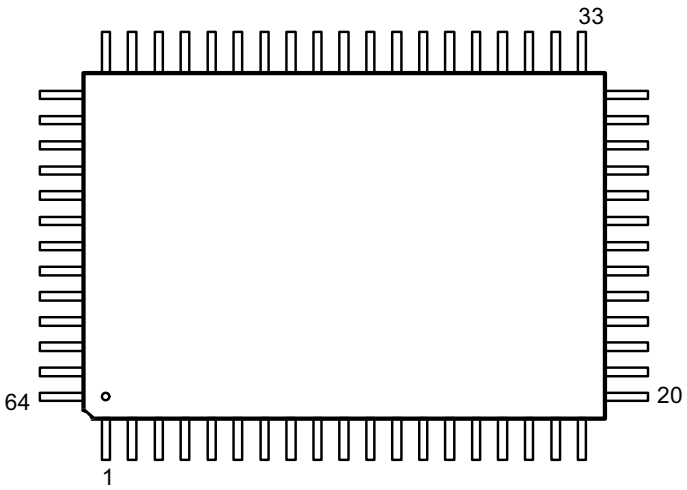
This chip is fabricated using Winbond's high performance CMOS technology.

FEATURES

- Supply voltage: 1.2V–1.7V or 2.4V–3.4V by mask option.
- Operating frequency: 32.768 KHz.
- Built-in crystal oscillator circuit.
- Voltage level shift with a μP.
- Two operating modes:
  - Normal mode (can be written by μP).
  - Clock mode (can be read out by μP).
- Max. 20 (160 dots) digits with 8 dots/digit displayed in normal mode.
- LCD (160 dots) can be programmed by μP from address 0.
- Clock display include leap-year, month, date, hour, minute, and sec.
- Clock adjustable through MODE, SET pins.
- Clock 12 or 24 format by pin select.
- 1/3 bias, 1/4 duty 40-segment LCD panel.
- Built-in V_{DD1} for different voltage system data transceiver application.
- Casecade function performed with Master/Slaver function option by mask option.

TYPE NO.	OPERATING VOLTAGE	OSCILLATOR
W33D0161	1.5V–1.7V	32.768 KHz Crystal
W33D0163	2.4V–3.4V	32.768 KHz Crystal
W33D0165	1.2V–1.7V	Slaver
W33D0166	2.4V–3.4V	Slaver

PIN CONFIGURATION



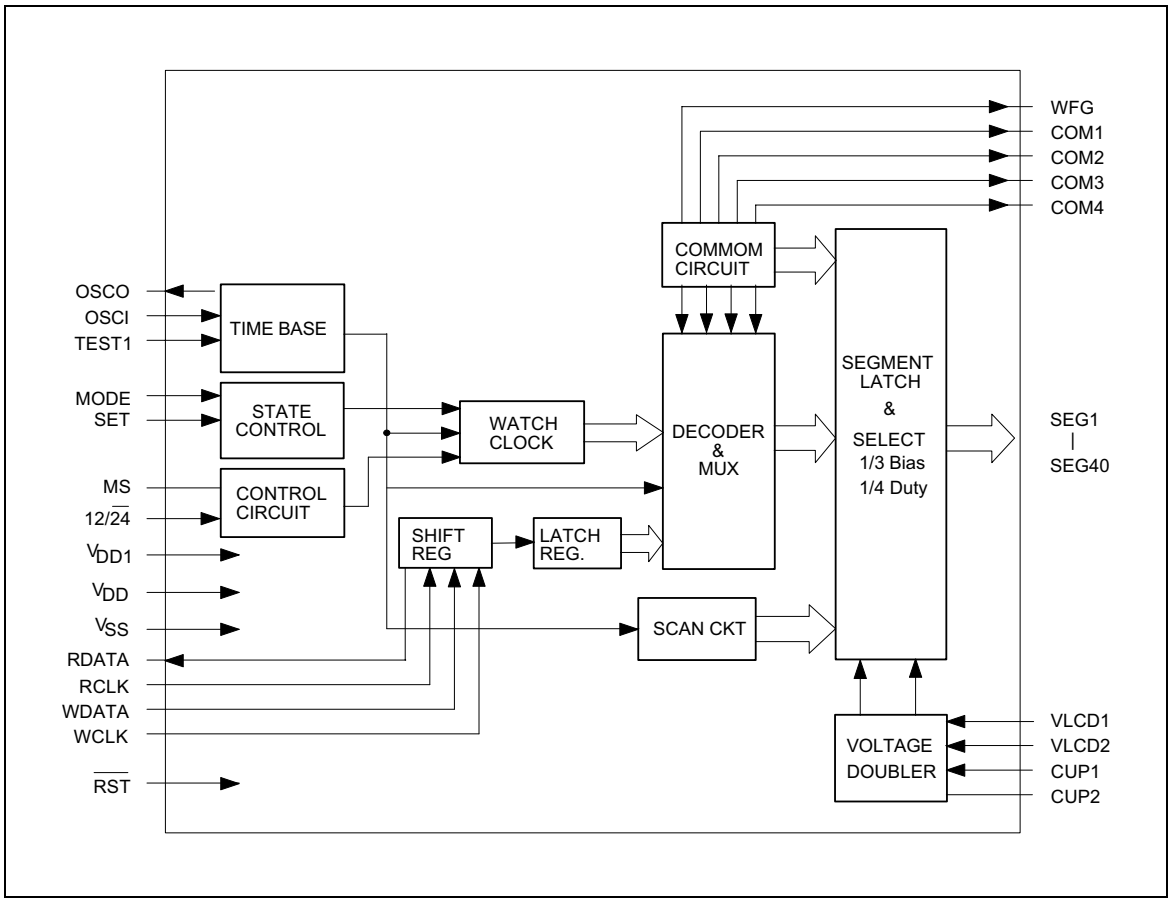
PIN DESCRIPTION

SYMBOL	PIN	I/O	FUNCTION
OSCI	38	I	Oscillator input pin. Connect to 32.768 KHz crystal. External capacitor is needed.
OSCO	37	O	Oscillator output pin with internal capacitor.
V_{DD}	35	I	Positive power supply.
V_{DD1}	45	I	For voltage level shift during data transceiver.
V_{SS}	39	I	Negative power supply.
V_{LCD1} V_{LCD2}	49, 48	I	LCD voltage pins.
CP, CN	50, 51	I	Connect a capacitor to both pins, used for the LCD double voltage capacitor.
TEST1	36	I	Test pin with pull-low resistor. Not use.
$\overline{RST}$	34	I	Chip reset input pin. Active low with internal pull-high resistor.
COM1-COM4	52–55	O	LCD panel common pins. (1/3 bias, 1/4 duty)

Pin Description, continued

SYMBOL	PIN	I/O	FUNCTION
SEG1- SEG40	56–64, 1–31	O	LCD panel segment pins. (1/3 bias, 1/4 duty)
RDATA	43	O	CMOS type serial data output pin. Power source: V_{DD1}
RCLK	41	I	Synchronous read clock input pin. Power source: V_{DD1}
WDATA	44	I	Serial data input pin. Power source: V_{DD1}
WCLK	40	I	Synchronous write clock input pin. Power source: V_{DD1}
MS	42	I	Mode select input pin with floating status. Normal mode is active high or low by mask option. In this SPEC description MS pin high active for the normal mode display. Power source: V_{DD1} (Refer to functional description for more detail)
12 / $\overline{24}$	46	I	12-hour (high) or 24-hour (low) clock select pin with floating status. Power source: V_{DD1}
WFG	47	O	Waveform generator output pin. When $\overline{RST}$ = 0, 1 Hz square-wave will output from this pin. When $\overline{RST}$ = 1, 1 Hz square-wave will output from this pin. Power source: V_{DD1}
MODE	32	I	Clock mode-adjust pin with internal pull-low resistor.
SET	33	I	Clock digit-adjust pin with internal pull-low resistor.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1. Operating Mode

The W33D0160 series LCD driver provides two operating modes: Normal mode, and Clock mode.

The Normal mode data can be written by μP only, but the Clock mode data can be read out by μP and can be adjusted by the manual method through the MODE and SET pins.

According Figure 1 the address 0–159 range works as the LCD data range and the address 160–167 work as the LCD control range. User must program the data over 168 clks to update all the data in the memory at one time, and the last 168 data will be the final data that can remain in the LCD data memory. In this case the last-in data that over 168 data will be the data of the address 167.

All the data in the location 0–167 can only be written by the WCLK and WDATA pins, and can not be read out. In this chip only the Real-Time-Clock data can be read out by the RCLK and RDATA pins.

The following table are the LCD data memory address mapping that can be written through the WCLK and WDATA pins, and the Real-Time-Clock data memory address mapping that can be read out through the RCLK and RDATA pins.

1.1.1 The write function address mapping definition (Normal mode)

(LCD data memory addressing mapping)

ADDRESS	FUNCTION
0–159	160 dots LCD panel display location, the first clk will define the address 0 data in the memory, but when the clk over 168 clks the first address will shift out, and keep the last 168 data in the memory.
160	Normal mode LCD panel ON/OFF control bit. (This bit will not affect the normal data in the chip, it just light on/off the LCD panel in the Normal data but not the Real-Time-clock data) 0: LCD panel light on.(Default value) 1: LCD panel light off.
161	Clock bit (This bit can disable or enable the Clock mode) 0: Clock mode can be shown on the LCD panel. (Default value) 1: Clock mode can not shown on the LCD panel.
162–167	Reserved.

1.1.2 The read function address mapping definition (Clock mode)

(The Real-time-clock data memory addressing mapping)

ADDRESS	FUNCTION
0–7	Month data memory range
8–15	Day data memory range
16–23	Hour data memory range
24–31	Minute data memory range
32–39	Second data memory range
40–47	Leap year data memory range

1.2 The transceiver function controlled by a μP:

The W33D0160 series LCD can display the data on LCD panel which is input by a serial transmission function from an external device such as a microprocessor. In Normal mode, the data can be written by a μP with transmission function at the rising edge of WCLK pin. In the Clock mode the Real-Time-Clock data can be read out by a μP with the receive function at the rising edge of RCLK pin. The RCLK pin and WCLK pin must be set to high state normally if there is no data reception and transmission.

1.2.1 Switch between Read and Write Function

When in write function, the first falling edge of RCLK will switch the write function to read function then μP can read data from the RCLK pin and RDATA pin, and vice versa. Refer to Figure 2. When the write function is re-active (changed from read function to write function or the power on reset), the WCLK clock input to the chip will reset the write-starting address to 0. In the same case the read function is re-active (changeed from write function to read function or the power on reset) The RCLK clock input to the chip will also reset the read-starting address to 0. Please refer to Figure 3 and Figure 4.

1.2.2 Serial Data Written by μP

A μP can send serial data and clock to through the WDATA pin and WCLK pin, respectively to control the LCD panel. When μP want to write data to the chip in Normal mode, firstly, μP must do a dummy read function or change read mode from write mode or pull MS pin from low to high to reset the write-starting addresss to 0, after this procedure the serial clock will sent by μP to set the LCD memory for the LCD display.

In this time, μP sends the serial data to the chip by the WDATA pin and WCLK pin, and W33D0160S will store the serial data from the starting address and the address is increased by one when the WCLK pin receives one clock form μP. Refer to Figure 3.

The LCD memory describe as above can not be read out from W33D0160.

1.2.3 Serial Data Read by μP

μP can only read out the Real-Time-Clock data from the RCLK and RDATA pins. Each time when the write mode change to read mode or pull the MS pin to low from high or do a dummy write function the Real-Time-Clock address will be reset to address 0, then input the clock to the RCLK pin, the Real-Time-Clock data will be sent out from RDATA pin.

The Real-Time-Clock data will output with the format as Month, Day, Hour, Minutes, Second and Leap-year. So there are only total 48 clocks can output all of the RTC memory data. The clock over the 48 will output the first memory in the RTC memory that will be the Month data.

The function of the two operating modes are described as below:

1.3 Normal mode:

MS pin pull high will make the LCD to show the normal data in the LCD panel, but no matter MS is high or low the rising edge on WCLK will write the the normal data to the LCD memory and the rising edge on RCLK will read out the Real-Time-Clock data memory.

The rising edge of the MS pin will also reset the address in the LCD memory to address 0, so in this case we can ommit the dummy read in the write procedure.

Because the LCD memory locate on the range of 0 to 159 and the LCD control memory locate on the range of 160 to 167, the first digit is shown in the most left place on the LCD panel. When μP write data to W33D0160S in normal mode, firstly, μP must reset the starting address to 0 , then μP can write one bit to W33D0160S while the WCLK pin receives one clock from μP and the address is increased by one after each one write clock input, as the address increase to 167, the next address is reset to 0, then the address increase continuously if WCLK pin keeps on receiving clock from μP.

When μP write data to W33D0160S more than 168 clocks with 160 dots at a time, the 169th clock will input the data to the first dot, and the rest can be done in the same manner. Refer to Figure 1.

Which operating mode is selected by MS pin, and Clock bit, where the Clock bit can be programmed by μP, the Clock bit locates on the address of 161.The default value of all the LCD control bits are "0".

Table 1 indicates the relation between operating mode and MS pin, and Clock bit.

1.4 Clock mode:

When the MS pin is pulled to low (by mask option), the Real-Time-Clock data will be shown on the LCD panel. As Table 2 the clock mode can display the leap-year, month, date, hour, minute and second. The RTC data will be shown on the LCD panel of the digit 3, 4, 6, 7, 11, 12, 14, 15, 17, 18, and 20. The other digits will keep the data as the Normal status before switch to Clock mode. That means if you want to show the only RTC data you must clear firstly all the Normal memorys or digit 1, 2, 5, 8, 9, 10, 13, 16, and 19 also you can control the Normal mode LCD ON/OFF control bit to 1 on the address of 160. Please refer to Figure 8.

The Real-Time-Clock data can only be adjusted by the Manual adjusting method through the MODE and SET pins. The following is the Manual adjusting method description.

1.4.1 Manual adjusting method through the MODE and SET pins.

When the Clock mode is entered (MS = low) , the current time is displayed on the LCD panel. Keep the MODE pin depressed (High Active) will cause the month digits to begin flashing. The SET pin can be used to adjust the month setting; the setting will increase by one with each trigger from the SET pin. When the MODE pin is released, the month digits will continue flash. At this time, a new input on the MODE pin will cause the date digits to begin flashing, and the date can then be set.

Successive inputs on the MODE pin will cause the hour, minute, and leap-year but no second digits to flash, allowing the hour, minute, and leap-year but no second data to be adjusted. While the leap-year digits are flashing, an input on the MODE pin will return to clock mode. While the clock setting is being adjusted at any time if there is no signal on the MODE pin for more than 15 seconds, it will return to clock mode automatically.

If the SET pin is depressed and held down over 2 seconds, the clock setting will speed up at an interval of 125 mS.

When the SET pin is ever depressed during the clock adjusting mode, the clock will be restarted from the new setting time with the second data reset to 0. The clock mode will automatically return to non-flash status from flash status if the flash status flash over 15 sec and no any key be depressed.

The MODE and SET pins are both high active. Refer to Figure 7.

2. Reset function

There are two methods to initialize the chip: one is power-on reset, the other is pulling the $\overline{RST}$ pin to low (low active).

2.1. Power-On Reset

At power on reset , the power-on reset circuit will generate a pulse to reset the chip. All LCD segments will flash momentarily about 2 seconds and the built-in clock will start from < 1 1 > and < 00 00 00 > and the 160 dots will be reset to "0".

2.2. $\overline{RST}$ Pin function

Pulling $\overline{RST}$ to low will reset all of the chip's functions except the clock memory, and all LCD segments will flash momentarily about 2 seconds and the 160 dots will be reset to "0".

3. LCD FORMAT

The LCD panel is 1/3 bias, 1/4 duty. Refer to Figure 9 and Figure 10. The LCD format is shown in Figure 11.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	-20 to +70	°C
Storage temperature	-55 to +155	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

V_{DD}-V_{SS} = 1.5V, F_{OSE} = 32.768 KHz, T_A = 25° C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage1	V_{DD1}	-	1.2	1.5	1.7	V
Op. Voltage2	V_{DD2}	-	2.4	3.0	3.4	V
Op. Current1	I_{DD1}	No load, V_{DD} = 1.5V (Crystal mode)	-	5	10	µA
Op. Current2	I_{DD2}	No load, V_{DD} = 3.0V (Crystal mode)	-	5	10	µA
SEG1–SEG40 Source Current	I_{SH}	V_{OH} = 1.2V	-0.4	-	-	mA
SEG1–SEG40 Sink Current	I_{SL}	V_{OL} = 0.3V	0.4	-	-	mA
COM1–COM4 Source Current	I_{CH1}	V_{OH} = 1.2V	-4	-	-	mA
COM1–COM4 Sink Current	I_{CL1}	V_{OL} = 0.3V	4	-	-	mA
WFG Source Current	I_{CH2}	V_{OH} = 1.2V	-	500	-	µA
WFG Sink Current	I_{CL2}	V_{OL} = 0.3V	-	500	-	µA
Pull-high Resistor	R_H	$\overline{RST}$	-	1000	2000	Kohm
Pull-low Resistor	R_L	MODE, SET	-	1000	2000	Kohm
Input Low Voltage	V_{IL}	-	0	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
RDATA Drive Current	I_{RDD}	V_{DD} = 3.0V	-	0.4	-	mA

AC CHARACTERISTICS

PARAMETER	SYMBOL	VDD	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Frequency	FOSC	1.5	Crystal	-	32.768	-	KHz
LCD Frequency	FLCD	-	Mask Option	-	16	-	Hz
				-	32	-	Hz
				-	64	-	Hz
Rising Debounce Time	TRD	-	MODE, SET (Crystal Mode)	35	-	-	mS
Falling Debounce Time	TFD	-	MODE, SET (Crystal Mode)	35	-	-	mS
MODE to SET Effect Time	TMS	-	-	1	-	-	mS
Slow Adjust Effect Period	TSPD	-	-	1	-	1999	mS
Quick Set Data Time	TQD	-	-	-	125	-	mS
Quick Set-up Time	TQS	-	-	2	-	-	S
$\overline{RST}$ Active Low Width	TRWD	-	-	-	1	-	µS
Serial Transmit Data Setup Time	TDS	-	-	50	-	-	nS
Serial Transmit Data Hold Time	TDH	-	-	50	-	-	nS
Serial Receive Data Access Time	TAS	-	-	50	-	-	nS
RCLK Period, WCLK Period	TCLK	-	-	150	-	-	nS
Transmit/Receive Time	TTRN	-	-	-	3	-	mS
Oscillator Start Up Time	TSTD	-	-	2	-	-	S
WFG Duty Cycle	TDCYL	-	-	-	50	-	%

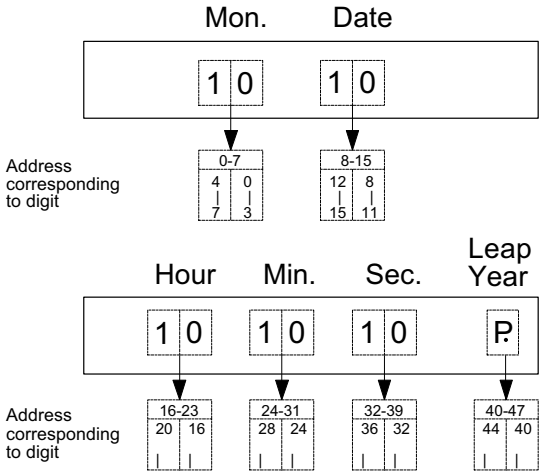
Table 1 The function table of three modes

MS	CLOCK	CLOCK MODE		NORMAL MODE	
pin	bit	Read out	Display-ed	Write	Display-ed
0	0	✓	✓	✓	✖
0	1	✓	✖	✓	✓
1	0	✓	✖	✓	✓
1	1	✓	✖	✓	✓

ps:

1. '✓' represent 'function existed'.
2. '✖' represent 'function not existed'.
3. MS pin high or low active can be select by mask option.

Table 2 The Address Mapping of Clock Mode



The address corresponding to the first displayed digit of Sec/Min./Hour/Date/Mon.

Address 4–7/ 12–15/ 20–23/ 28–31/ 36–39	Displayed Digit
0 0 0 0	None(M/D), ✻ (H/Mi/S)
0 0 0 1	1 (M/D/H/Mi/S)
0 0 1 0	2 (D/Mi/H/S)
0 0 1 1	3 (D/Mi/S)
0 1 0 0	4 (Mi./S)
0 1 0 1	5 (Mi./S)
Others	★(M/D/H/Mi/S)

40-47	H dot of 20th digit
0 0 0 0	•
0 0 0 1	None
0 0 1 0	None
0 0 1 1	None
Others	★

Ps:

1. (M/D/H/Mi/S) means "for Mon. or Date or Hour or Min. or Sec.".
2. "✻" : Displays "0" or none by mask option
3. "★" : Represent an illegal programming data
4. "•" : Represent a leap year

The address corresponding to the 2nd displayed digit of Sec/Min./Hour/Date/Mon.

Address 0–3/ 8–11/ 16–19/ 24–27/ 32–35	Displayed Digit
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
Others	★

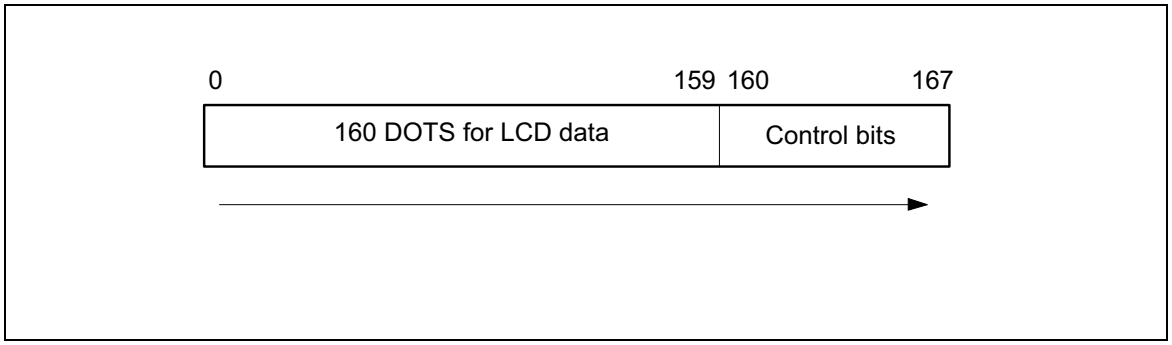


Figure 1. Address Format

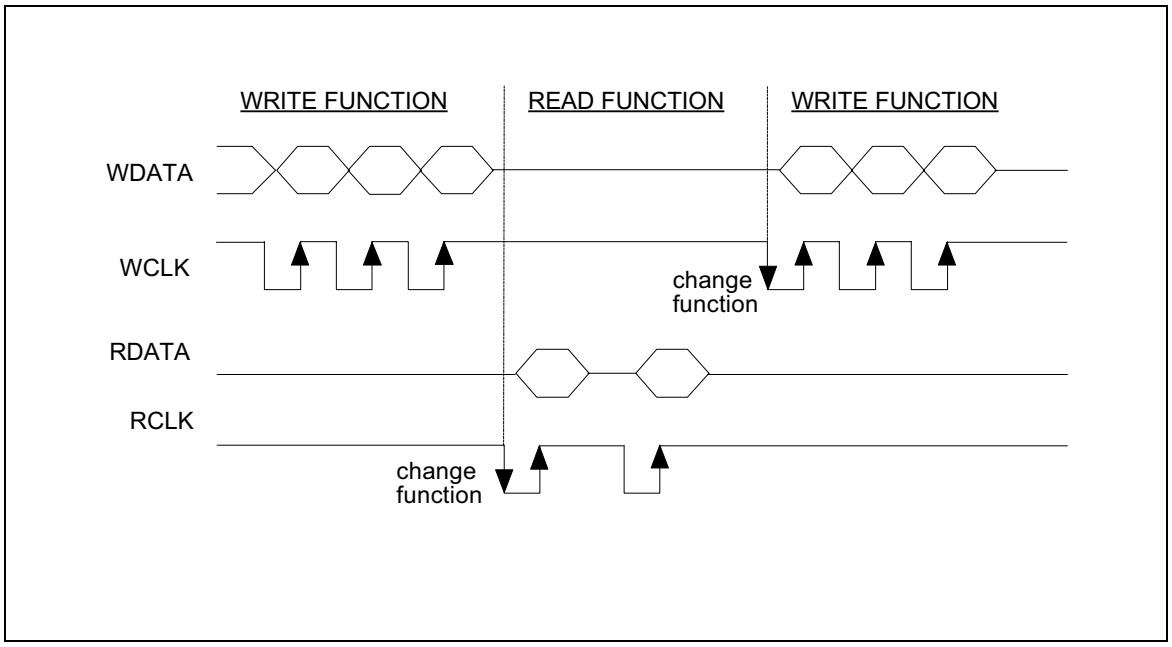


Figure 2. Read/Write Change Function

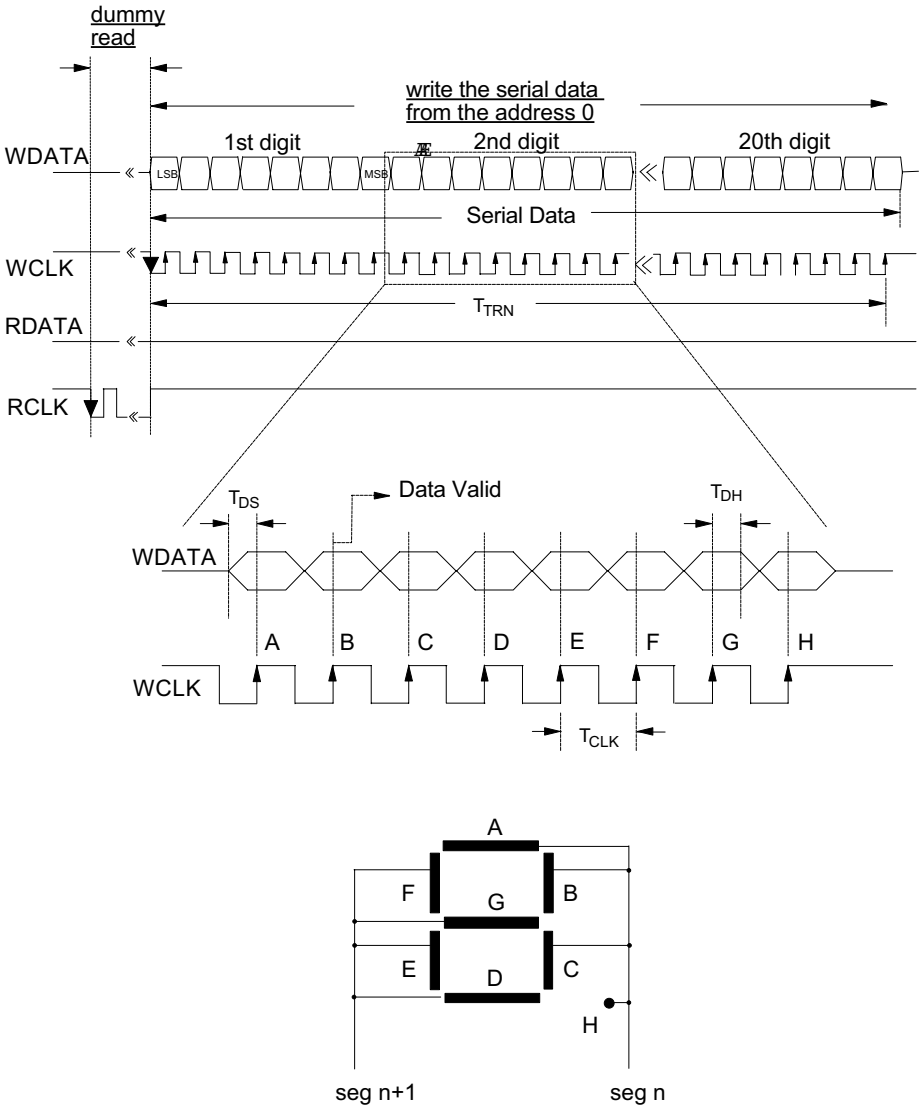


Figure 3. Write Function Controlled By μP

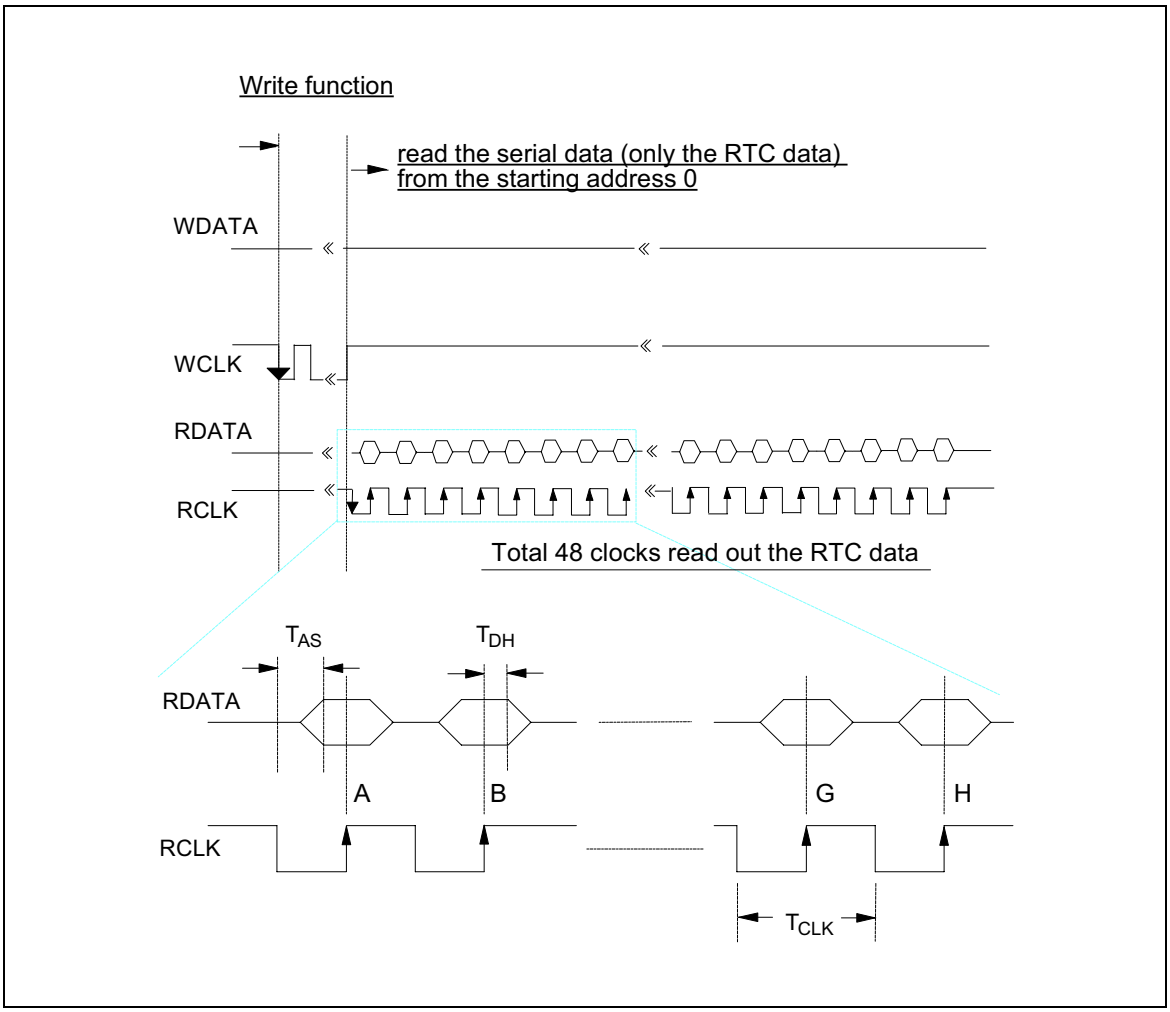


Figure 4. Read Function Controlled By µP

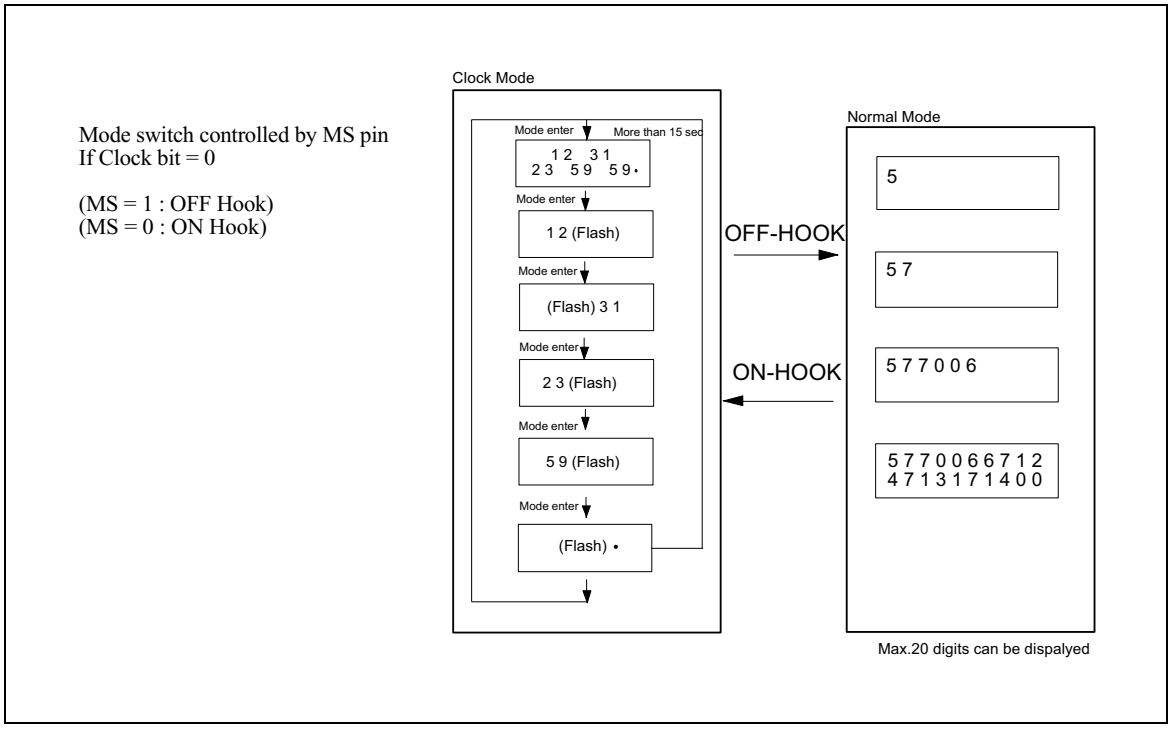


Figure 5. Mode Chart

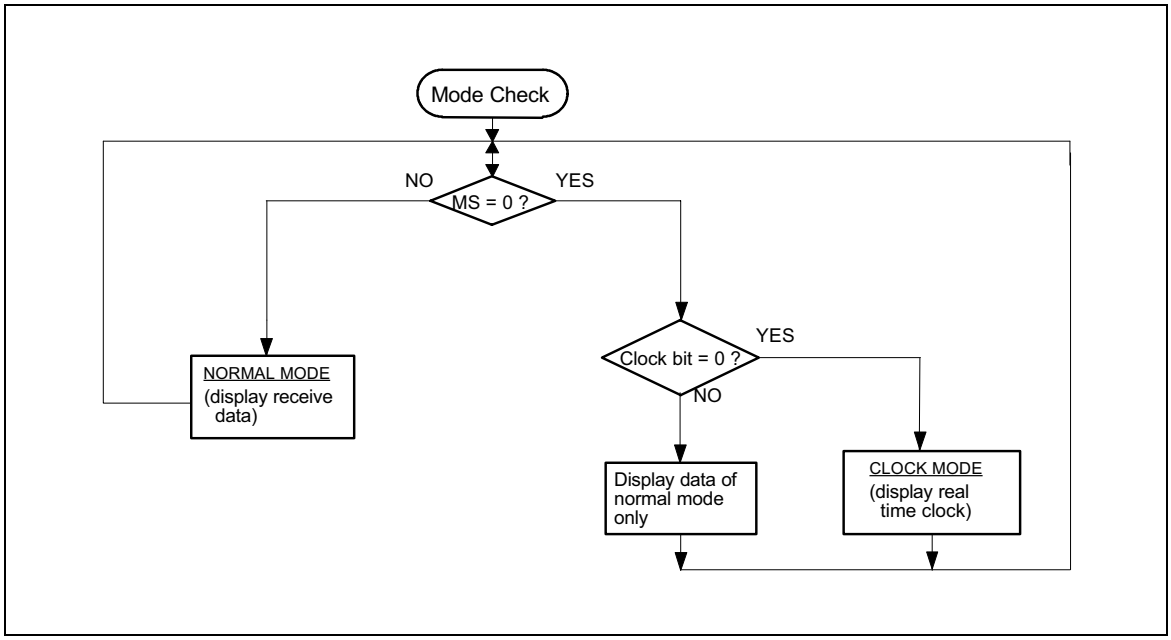


Figure 6. Flow Chart

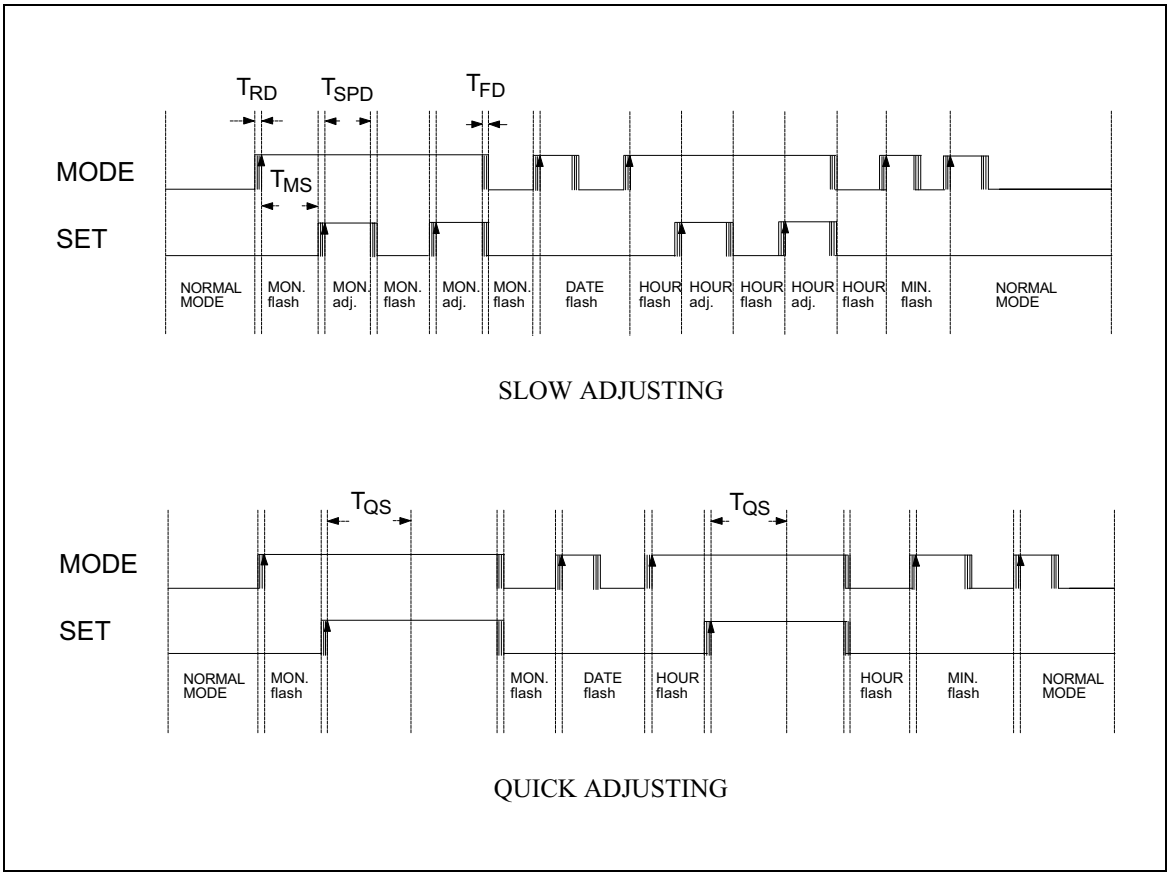
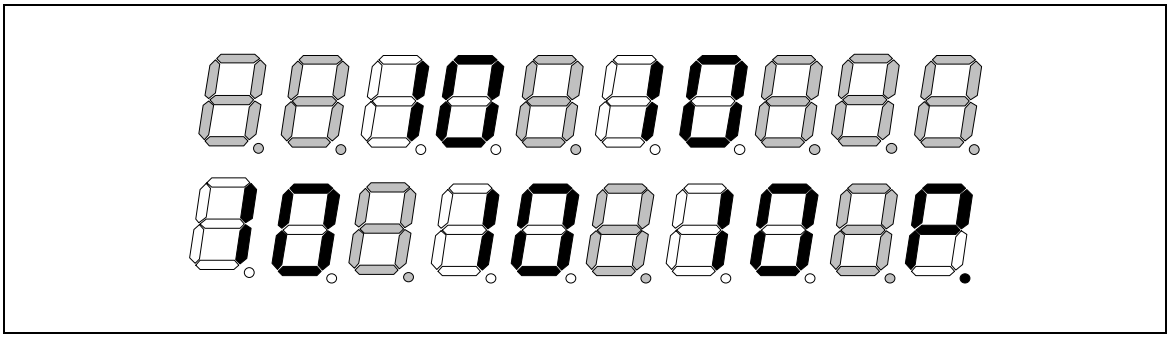


Figure 7. Clock Adjusting



The digit 1, 2, 5, 8, 9, 10, 13, 16, and 19 will not be affected and will be the same as the final status in Normal mode.

Figure 8. LCD Clock Format

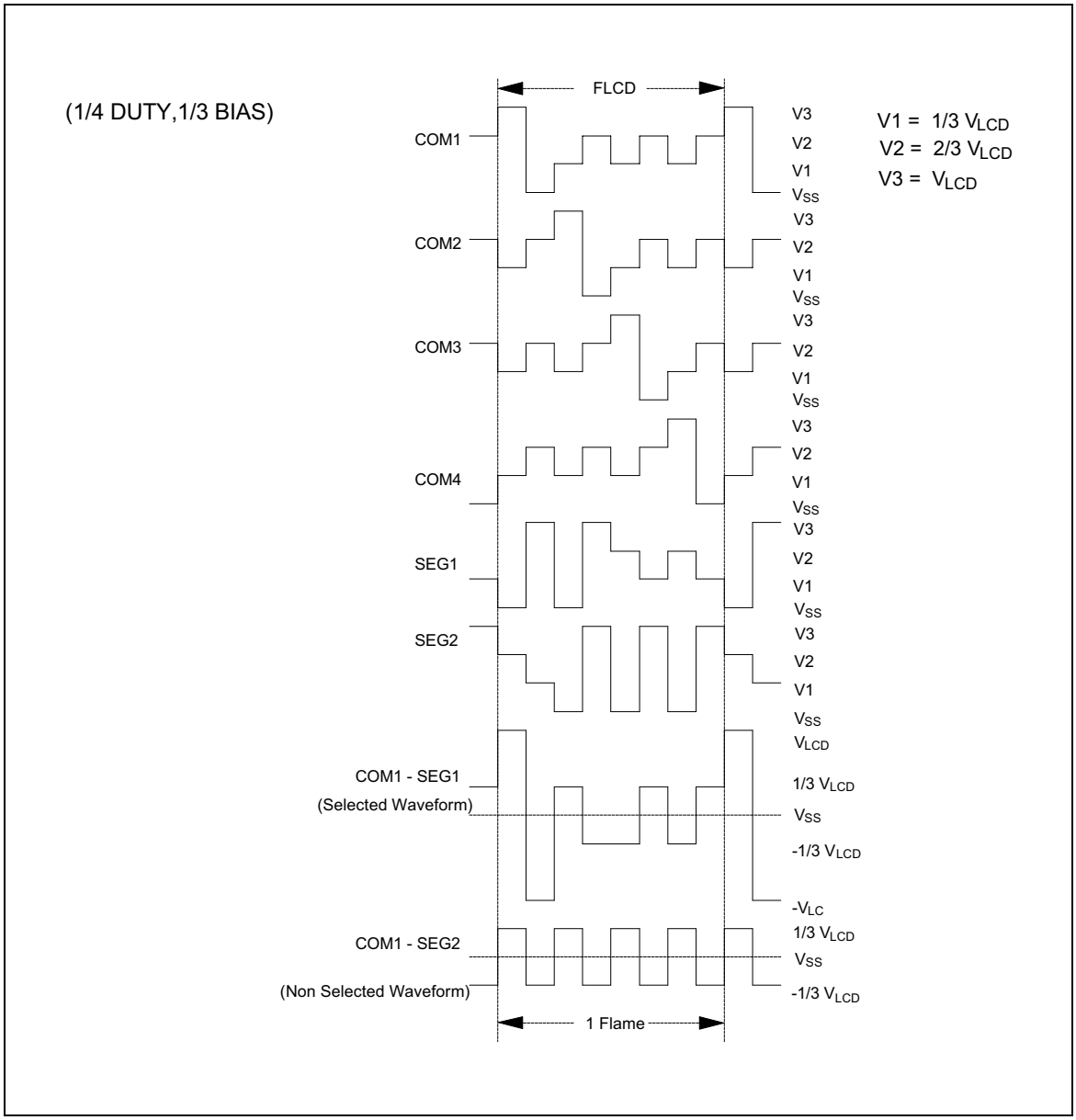


Figure 10. LCD Waveform

SEG	digit 1		digit 2		digit 3		digit 4		digit 5		digit 6		digit 7		digit 8		digit 9		digit 10	
COM	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
1	F	A	F	A	F	A	F	A	F	A	F	A	F	A	F	A	F	A	F	A
2	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
3	E	C	E	C	E	C	E	C	E	C	E	C	E	C	E	C	E	C	E	C
4	D	H	D	H	D	H	D	H	D	H	D	H	D	H	D	H	D	H	D	H

SEG	digit 11		digit 12		digit 13		digit 14		digit 15		digit 16		digit 17		digit 18		digit 19		digit 20	
COM	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	F	A	F	A	F	A	F	A	F	A	F	A	F	A	F	A	F	A	F	A
2	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
3	E	C	E	C	E	C	E	C	E	C	E	C	E	C	E	C	E	C	E	C
4	D	H	D	H	D	H	D	H	D	H	D	H	D	H	D	H	D	H	D	H

Figure 11. LCD Panel Format

The diagram of W33D0160S controlled by μP is shown in Figure 13.

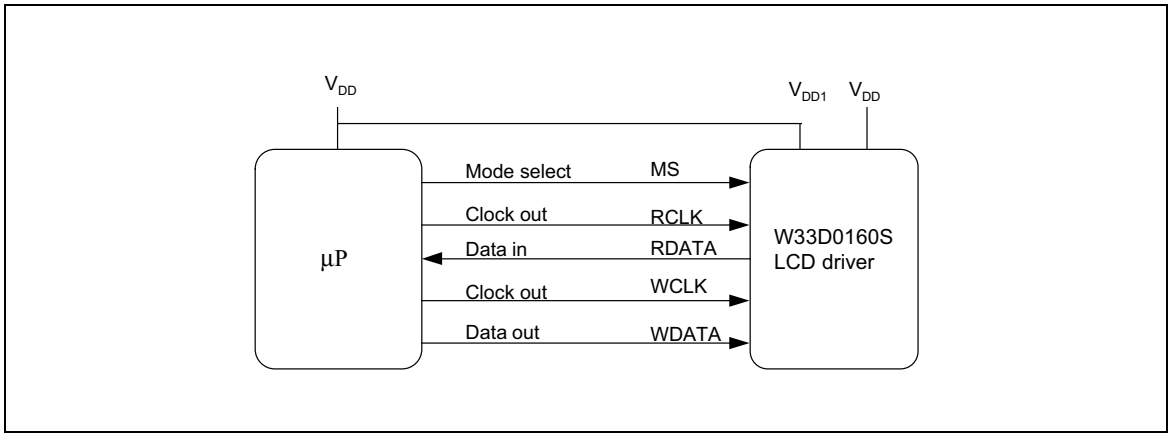


Figure 12. Application Suggestion

Noet: The condition that normal mode is enabled by setting MS pin high or low is mask option. Throughout all this spec., the normal mode is enabled when MS pin is high.

V_{DD}: W33D0160S Main power

V_{DD1}: Voltage source come from uP for level shift

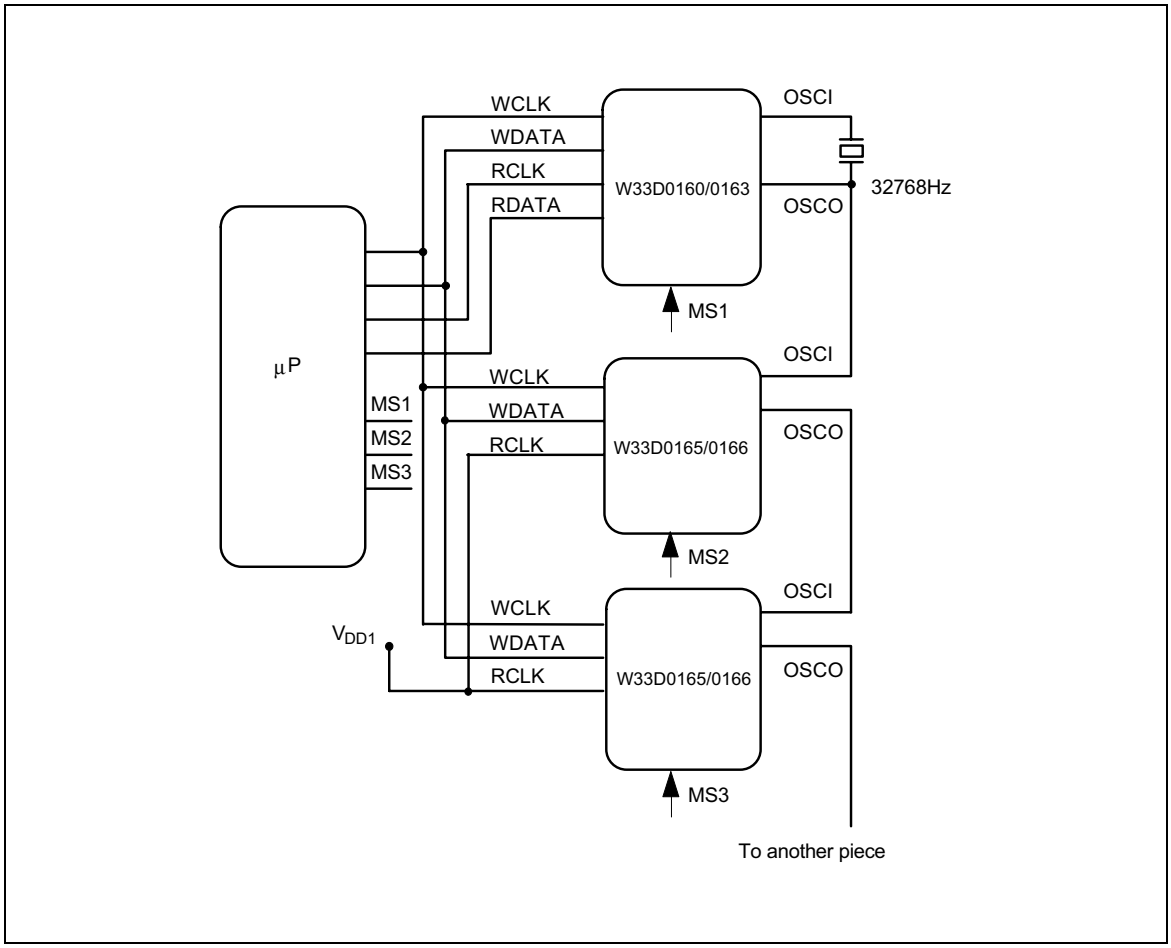
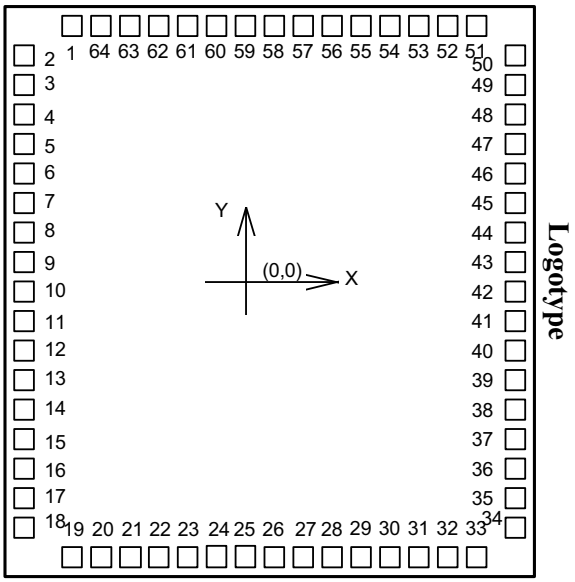


Figure 13. Normal Mode Cascade Application Circuit

BONDING PAD DIAGRAM



Notes:

1. The substrate must be connect to Vss.
2. The chip size is 2550.00 x 2720.00 μm^2.

PAD LIST

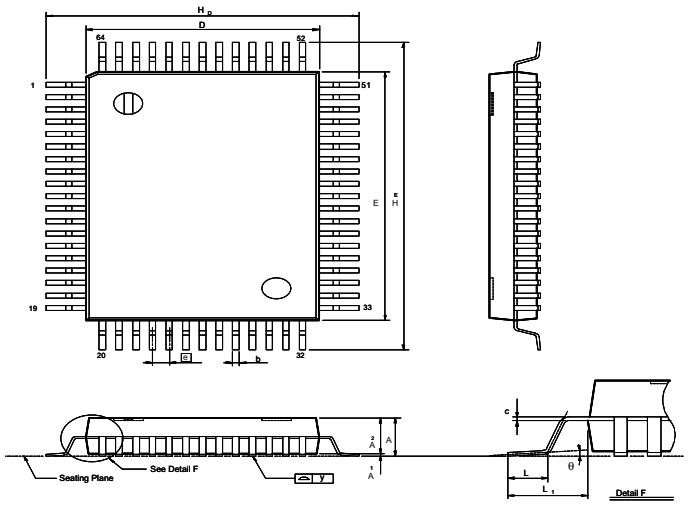
PAD NO.	PAD NAME	PIN#	X	Y	PAD NO.	PAD NAME	PIN#	X	Y
1	SEG 10	1	-963.00	1235.00	33	SET	33	945.30	-1229.90
2	SEG 11	2	-1150.00	1091.40	34	$\overline{RST}$	34	1129.50	-1089.10
3	SEG 12	3	-1150.00	955.20	35	VDD	35	1129.50	-947.30
4	SEG 13	4	-1150.00	819.20	36	TEST	36	1129.50	-816.90
5	SEG 14	5	-1150.00	683.00	37	OSCO	37	1129.50	-677.90
6	SEG 15	6	-1150.00	547.00	38	OSCI	38	1129.50	-541.90
7	SEG 16	7	-1150.00	410.80	39	Vss	39	1129.50	-402.90
8	SEG 17	8	-1150.00	274.80	40	WCLK	40	1129.50	-272.50
9	SEG 18	9	-1150.00	138.60	41	RCLK	41	1129.50	-130.70
10	SEG 19	10	-1150.00	2.60	42	MS	42	1129.50	-0.30
11	SEG 20	11	-1150.00	-133.60	43	RDATA	43	1129.50	141.50
12	SEG 21	12	-1150.00	-269.60	44	WDATA	44	1129.50	271.90
13	SEG 22	13	-1150.00	-405.80	45	VDD1	45	1129.50	413.70
14	SEG 23	14	-1150.00	-541.80	46	12 / $\overline{24}$	46	1129.50	544.10

Pad List, continued

PAD NO.	PAD NAME	PIN#	X	Y	PAD NO.	PAD NAME	PIN#	X	Y
15	SEG 24	15	-1150	-678.00	47	WFG	47	1129.50	685.90
16	SEG 25	16	-1150	-814.00	48	VLCD2	48	1129.50	819.10
17	SEG 26	17	-1150	-950.20	49	VLCD1	49	1129.50	955.30
18	SEG 27	18	-1150	-1086.20	50	CP	50	1129.50	1091.30
19	SEG 28	19	-963.00	-1229.90	51	CN	51	942.50	1235.00
20	SEG 29	20	-826.80	-1229.90	52	COM1	52	809.20	1235.00
21	SEG 30	21	-690.80	-1229.90	53	COM2	53	667.40	1235.00
22	SEG 31	22	-554.60	-1229.90	54	COM3	54	537.00	1235.00
23	SEG 32	23	-418.60	-1229.90	55	COM4	55	395.20	1235.00
24	SEG 33	24	-282.40	-1229.90	56	SEG1	56	262.00	1235.00
25	SEG 34	25	-146.40	-1229.90	57	SEG2	57	125.80	1235.00
26	SEG 35	26	-10.20	-1229.90	58	SEG3	58	-10.20	1235.00
27	SEG 36	27	125.80	-1229.90	59	SEG4	59	-146.40	1235.00
28	SEG 37	28	262.00	-1229.90	60	SEG5	60	-282.40	1235.00
29	SEG 38	29	398.00	-1229.90	61	SEG6	61	-418.60	1235.00
30	SEG 39	30	534.20	-1229.90	62	SEG7	62	-554.60	1235.00
31	SEG 40	31	670.20	-1229.90	63	SEG8	63	-690.80	1235.00
32	MODE	32	809.20	-1229.90	64	SEG9	64	-826.80	1235.00

PACKAGE DIAMENSION

64-pin QFP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.012	0.016	0.020	0.30	0.40	0.50
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.033	0.039	0.045	0.85	1.00	1.15
H_D	0.738	0.748	0.758	18.75	19.00	19.25
H_E	0.974	0.984	0.994	24.75	25.00	25.25
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	—	0.098	—	—	2.50	—
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

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