

9-CHANNEL DUAL-MODE TRANSCEIVERS

FEATURES

- 9 Channels for the Data and Control Paths of the Small Computer Systems Interface (SCSI)
- Supports Single-Ended and Low-Voltage Differential (LVD) SCSI
- CMOS Input Levels ('LVDM976) or TTL Input Levels ('LVDM977) Available
- Includes DIFFSENS Comparators on CDE0
- Single-Ended Receivers Include Noise Pulse Rejection Circuitry
- Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch
- Low Disabled Supply Current 7 mA Maximum
- Power-Up/Down Glitch Protection
- Bus is High-Impedance With $V_{CC} = 1.5$ V
- Pin-Compatible With the SN75976ADGG High-Voltage Differential Transceiver

DESCRIPTION

The SN75LVDM976 and SN75LVDM977 have nine transceivers for transmitting or receiving the signals to or from a SCSI data bus. They offer electrical compatibility to both the single-ended signaling of X3.277:1996-SCSI-3 Parallel Interface (Fast-20) and the new low-voltage differential signaling method of proposed standard 1142-D SCSI Parallel Interface – 2 (SPI-2).

The differential drivers are nonsymmetrical. The SCSI bus uses a dc bias on the line to allow terminated fail safe and wired-OR signaling. This bias can be as high as 125 mV and induces a difference in the high-to-low and low-to-high transition times of a symmetrical driver. In order to reduce pulse skew, an LVD SCSI driver's output characteristics become nonsymmetrical. In other words, there is more assertion current than negation current to or from the driver. This allows the actual differential signal voltage on the bus to be symmetrical about 0 V. Even though the driver output characteristics are nonsymmetrical, the design of the 'LVDM976 drivers maintains balanced signaling. Balanced means that the current that flows in each signal line is nearly equal but opposite in direction and is one of the keys to the low-noise performance of a differential bus.

DGG PACKAGE (TOP VIEW)			
INV/NON	1	56	CDE2
GND	2	55	CDE1
GND	3	54	CDE0
1A	4	53	9B+
1DE/RE	5	52	9B-
2A	6	51	8B+
2DE/RE	7	50	8B-
3A	8	49	7B+
3DE/RE	9	48	7B-
4A	10	47	6B+
4DE/RE	11	46	6B-
V_{CC}	12	45	V_{CC}
GND	13	44	GND
GND	14	43	GND
GND	15	42	GND
GND	16	41	GND
GND	17	40	GND
V_{CC}	18	39	V_{CC}
5A	19	38	5B+
5DE/RE	20	37	5B-
6A	21	36	4B+
6DE/RE	22	35	4B-
7A	23	34	3B+
7DE/RE	24	33	3B-
8A	25	32	2B+
8DE/RE	26	31	2B-
9A	27	30	1B+
9DE/RE	28	29	1B-

AVAILABLE OPTIONS

T_A	PACKAGE	
	TSSOP (DGG) CMOS INPUT LEVELS	TSSOP (DGG) TTL INPUTS LEVELS
0°C to 70°C	SN75LVDM976DGG SN75LVDM976DGGR ⁽¹⁾	SN75LVDM977DGG SN75LVDM977DGGR ⁽¹⁾

(1) The R suffix designates a taped and reeled package.



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DESCRIPTION (CONTINUED)

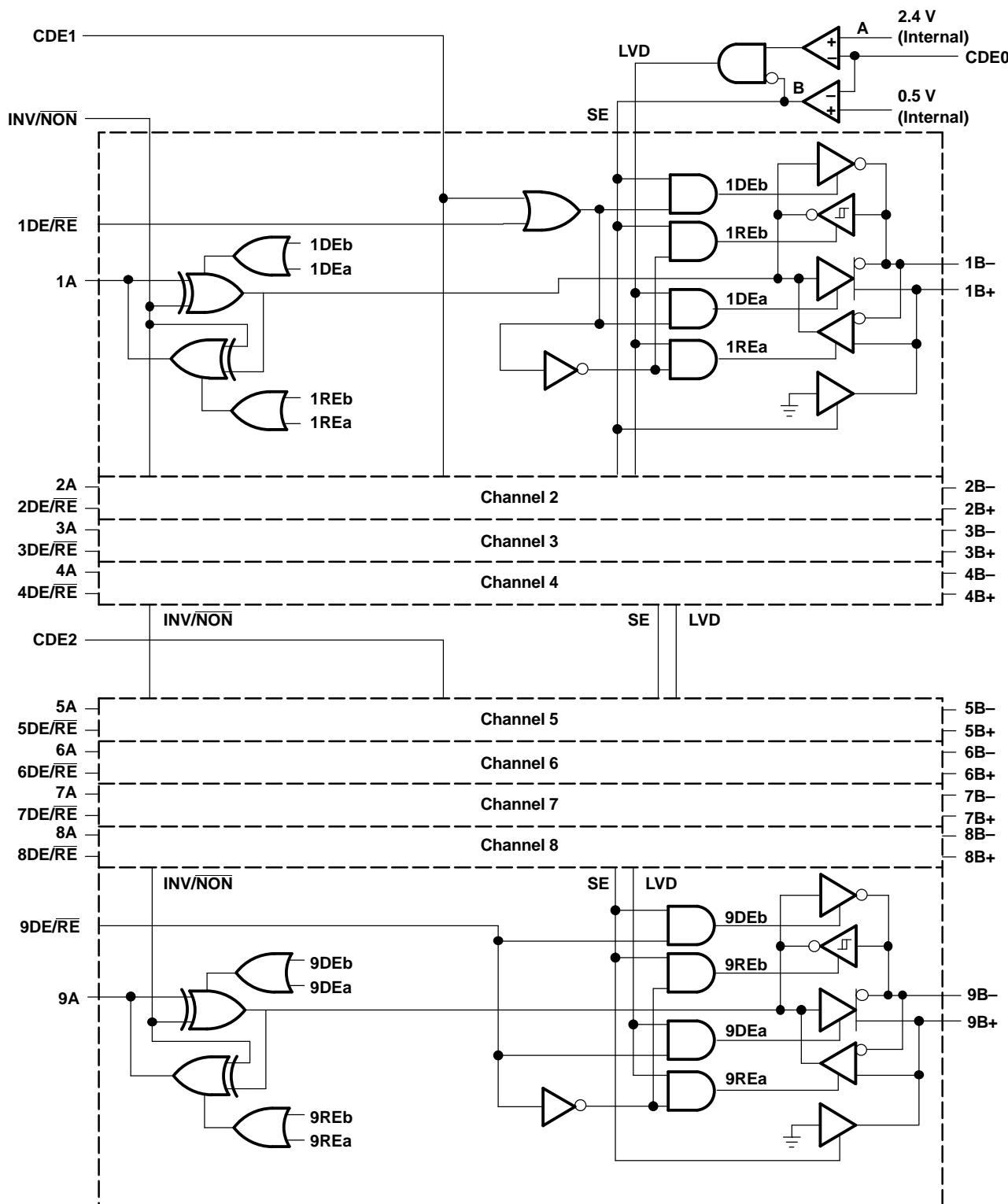
The signal symmetry requirements of the LVD-SCSI bus mean you can no longer obtain logical inversion of a signal by simply reversing the differential signal connections. This requires the ability to invert the logic convention through the INV/NON terminal. This input would be a low for SCSI controllers with active-high data and high for active-low data. In either case, the B+ signals of the transceiver must be connected to the SIGNAL+ line of the SCSI bus and the B- of the transceiver to the SIGNAL- line.

The CDE0 input incorporates a window comparator to detect the status of the DIFFSENS line of a SCSI bus. This line is below 0.5 V, if using single-ended signals, between 1.7 V and 1.9 V if low-voltage differential, and between 2.4 V and 5.5 V if high-voltage differential. The outputs assume the characteristics of single-ended or LVD accordingly or place the outputs into high-impedance, when HVD is detected. This, and the INV/NON input, are the only differences to the trade-standard function of the SN75976A HVD transceiver.

Two options are offered to minimize the signal noise margins on the interface between the communications controller and the transceiver. The SN75LVDM976 has logic input voltage thresholds of about 0.5 V_{CC}. The SN75LVDM977 has a fixed logic input voltage threshold of about 1.5 V. The input voltage threshold should be selected to be near the middle of the output voltage swing of the corresponding driver circuit.

The SN75LVDM976 and SN75LVDM977 are characterized for operation over a free-air temperature range of T_A = 0°C to 70°C.

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC DIAGRAMS AND FUNCTION TABLES

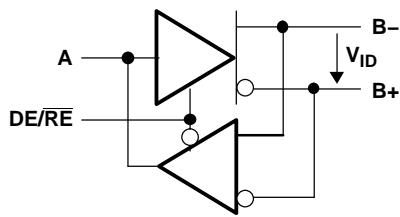


Figure 1. Inverting LVD Transceiver

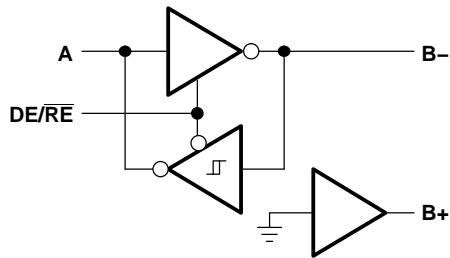


Figure 2. Inverting Single-Ended Transceiver

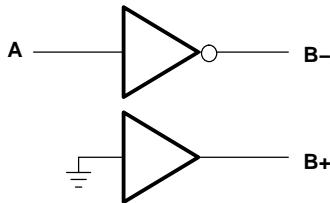


Figure 3. Inverting Single-Ended Driver

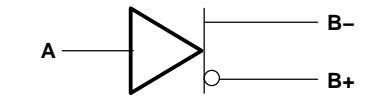


Figure 4. Inverting LVD Driver

FUNCTION TABLE

INPUTS		OUTPUTS		
$(B+ - B-)$	DE/RE	A	$B+$	$B-$
$V_{ID} \geq 30 \text{ mV}$	L	NA	Z	Z
$-30 \text{ mV} < V_{ID} < 30 \text{ mV}$	L	NA	Z	Z
$V_{ID} - 30 \text{ mV}$	L	NA	Z	Z
Open circuit	L	NA	Z	Z
NA	H	L	H	L
NA	H	H	L	H
				Z

FUNCTION TABLE

INPUTS			OUTPUTS		
$B-$	DE/RE	A	$B+$	$B-$	A
H	L	NA	L	Z	L
L	L	NA	L	Z	H
Open circuit	L	NA	L	Z	?
NA	H	L	L	H	Z
NA	H	H	L	L	Z

FUNCTION TABLE

INPUT	OUTPUTS	
A	$B+$	$B-$
L	L	H
H	L	L

FUNCTION TABLE

INPUT	OUTPUTS	
A	$B+$	$B-$
L	H	L
H	L	H

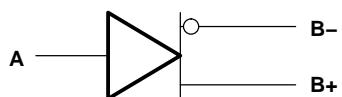


Figure 5. Noninverting LVD Driver

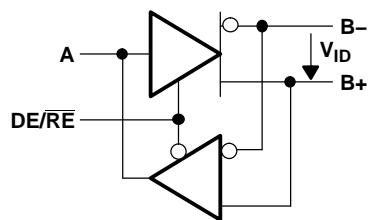


Figure 6. Noninverting LVD Transceiver

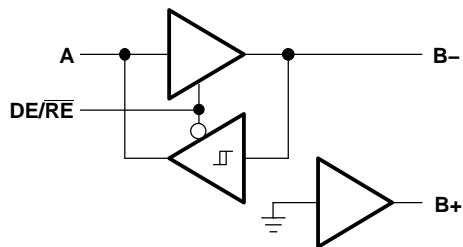


Figure 7. Noninverting Single-Ended Transceiver

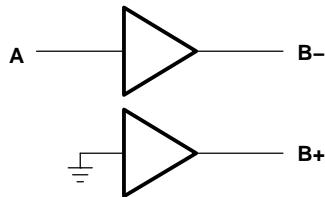


Figure 8. Noninverting Single-Ended Driver

FUNCTION TABLE

INPUT	OUTPUTS	
A	B+	B-
L	L	H
H	H	L

FUNCTION TABLE

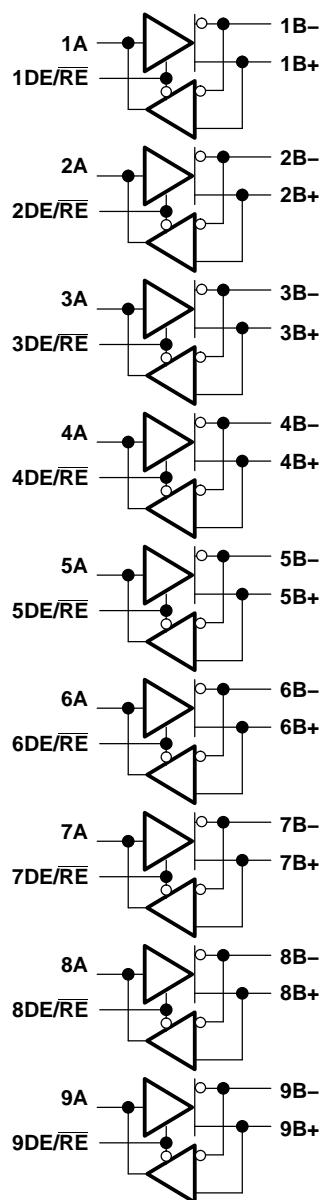
INPUTS		OUTPUTS		
(B+ - B-)	DE/RE	A	B+	B-
$V_{ID} \geq 30 \text{ mV}$	L	NA	Z	Z
$-30 \text{ mV} < V_{ID} < 30 \text{ mV}$	L	NA	Z	Z
$V_{ID} \leq -30 \text{ mV}$	L	NA	Z	Z
Open circuit	L	NA	Z	Z
NA	H	L	L	H
NA	H	H	H	L

FUNCTION TABLE

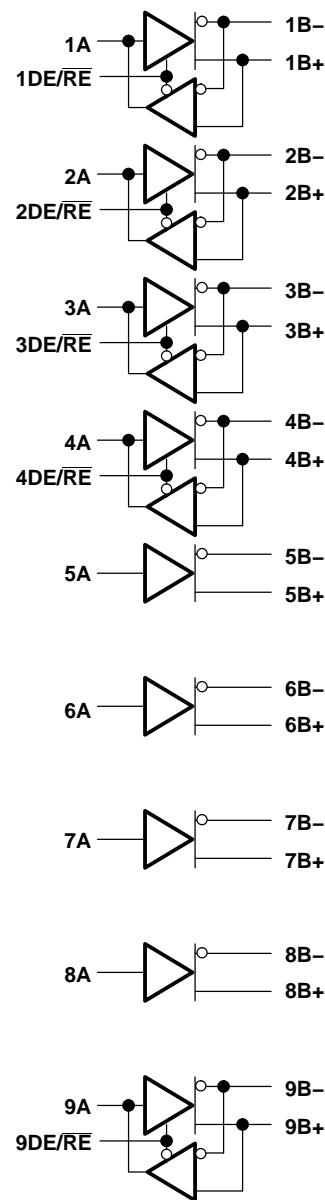
INPUTS			OUTPUTS		
B-	DE/RE	A	B+	B-	A
H	L	NA	L	Z	H
L	L	NA	L	Z	L
Open circuit	L	NA	L	Z	?
NA	H	L	L	L	Z
NA	H	H	L	H	Z

FUNCTION TABLE

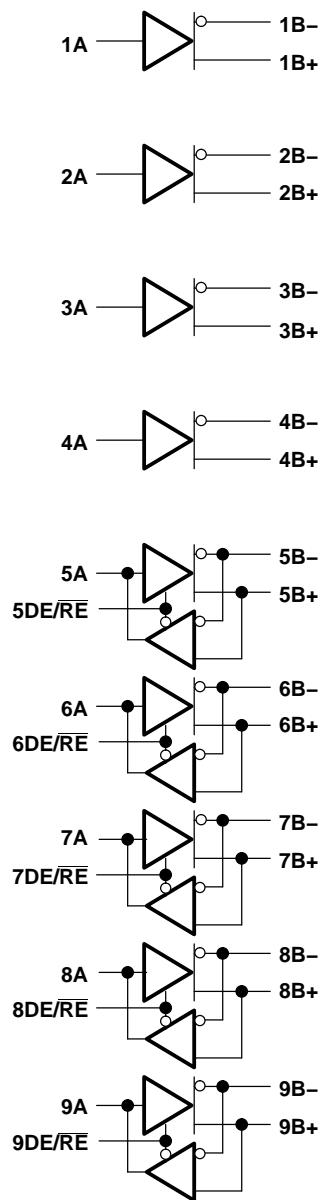
INPUT	OUTPUTS	
A	B+	B-
L	L	L
H	L	H



(a)



(b)



Control Inputs
CDE0 0.7 V < V_I < 1.9 V
INV/NON L
CDE1 L
CDE2 H

(c)

Figure 9. Logic Diagrams

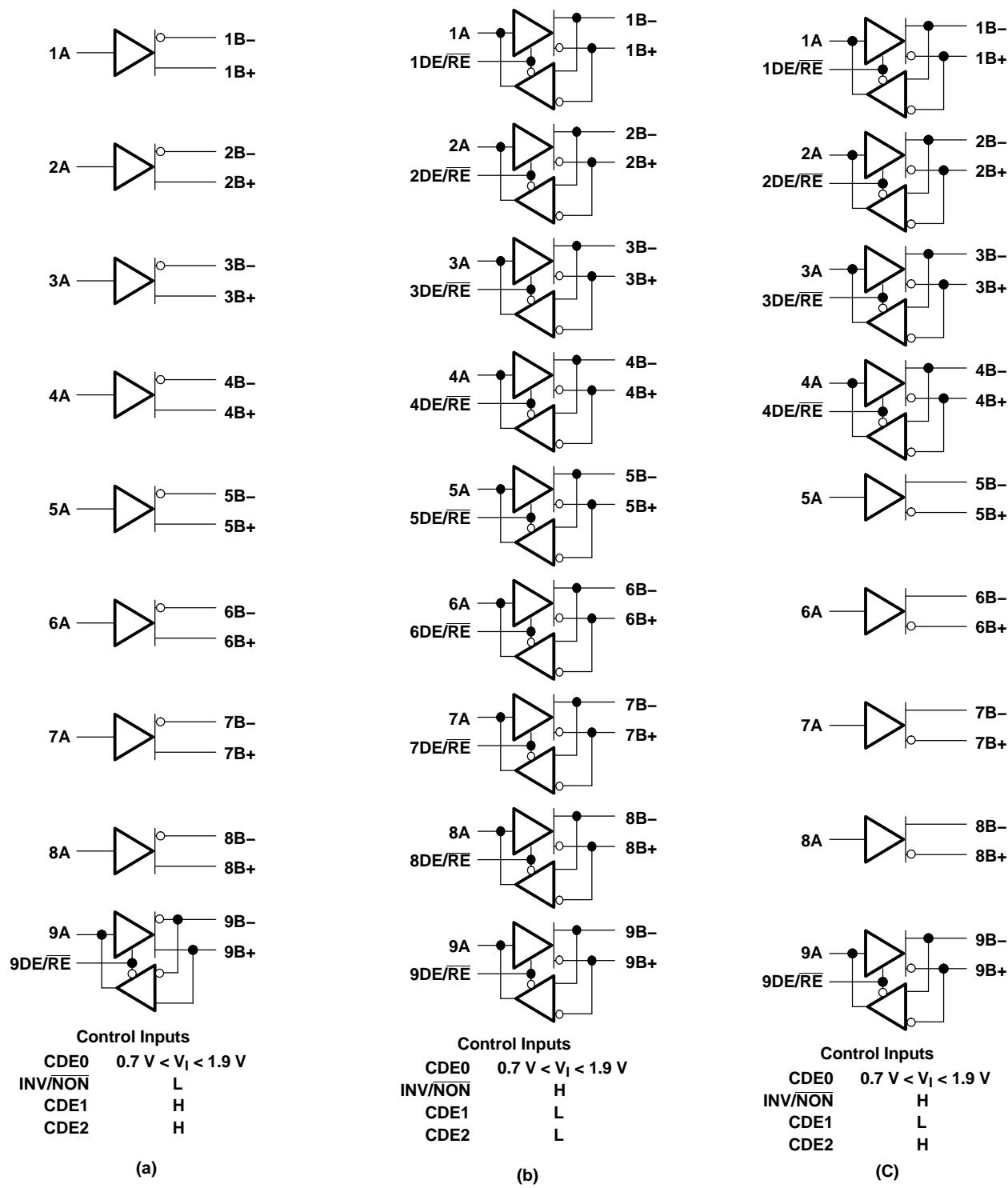


Figure 10. Logic Diagrams

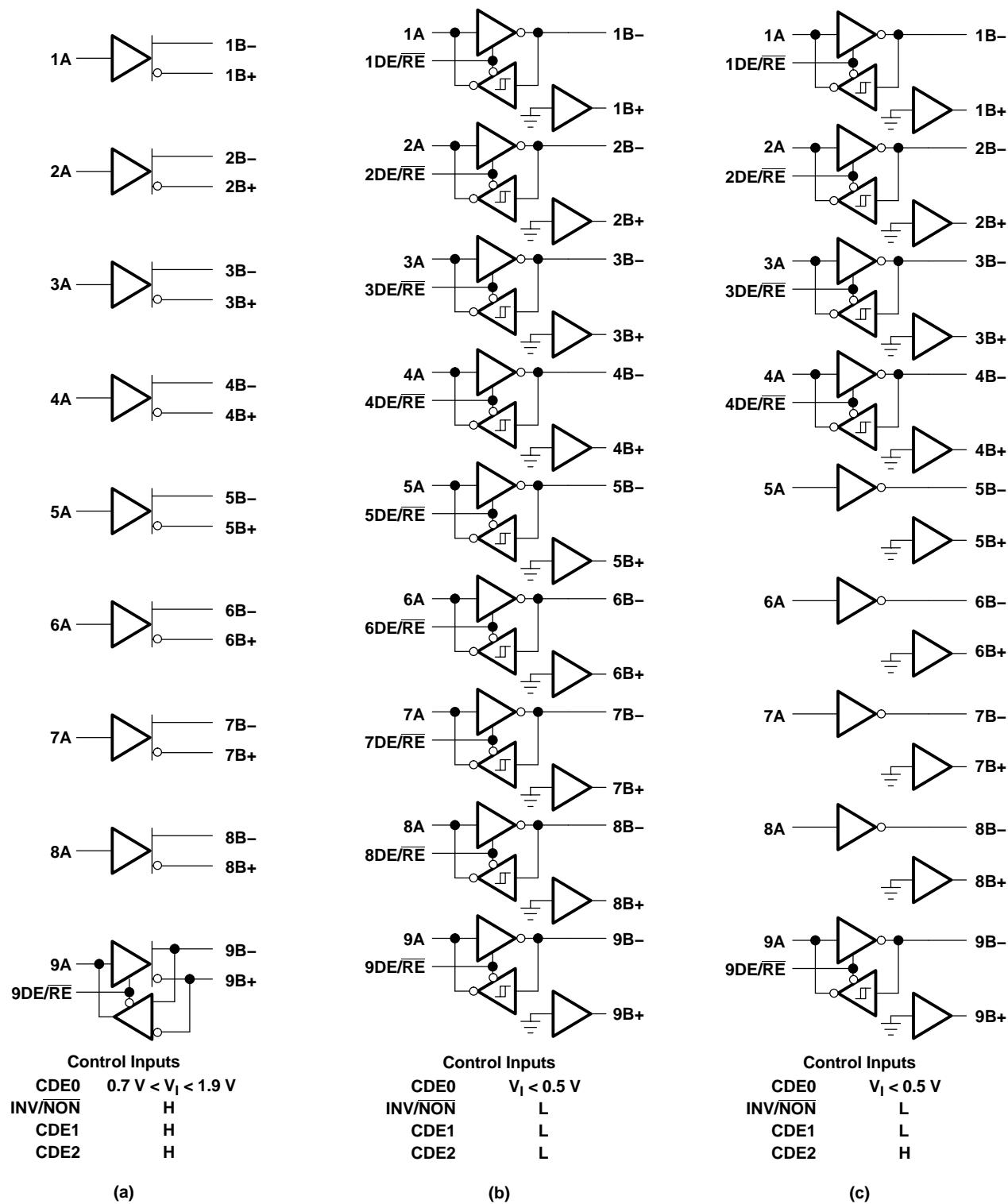


Figure 11. Logic Diagrams

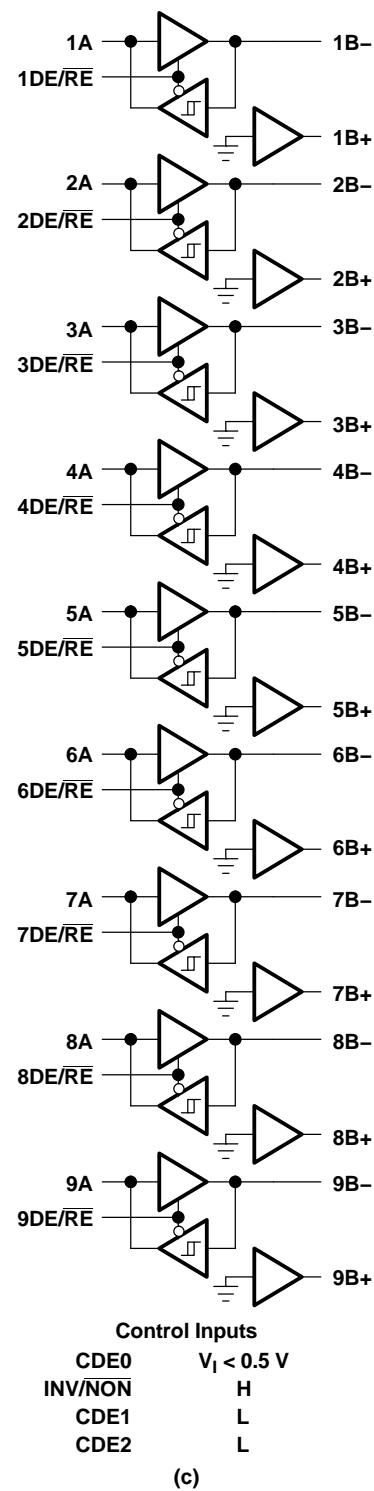
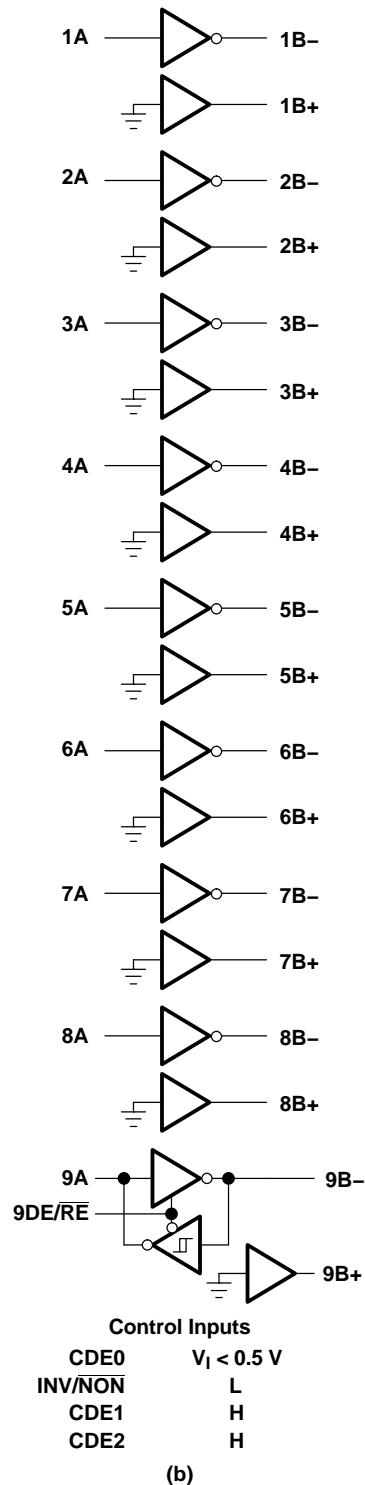
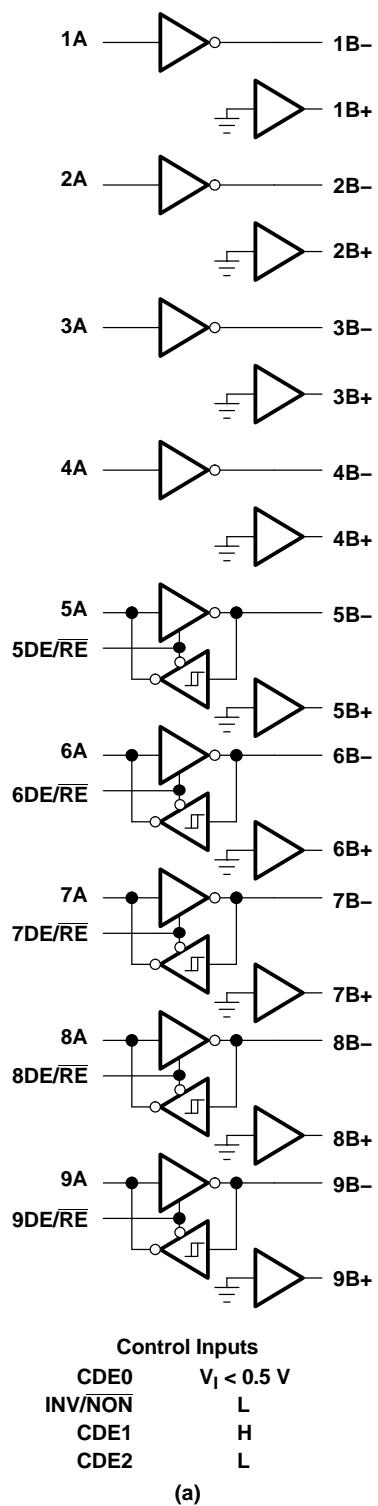
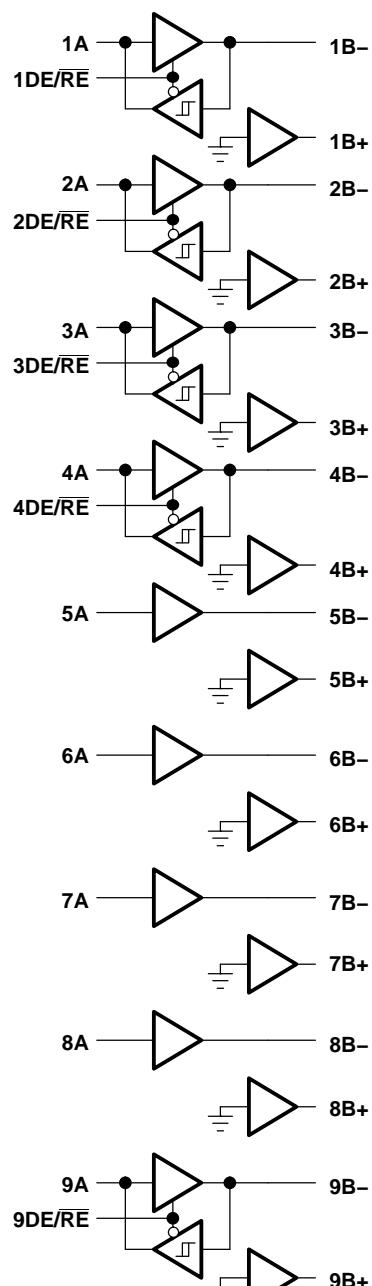
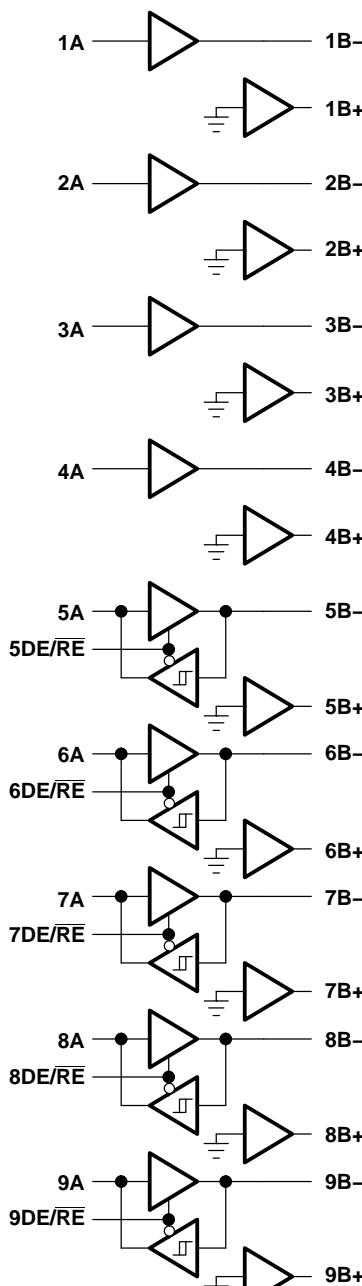


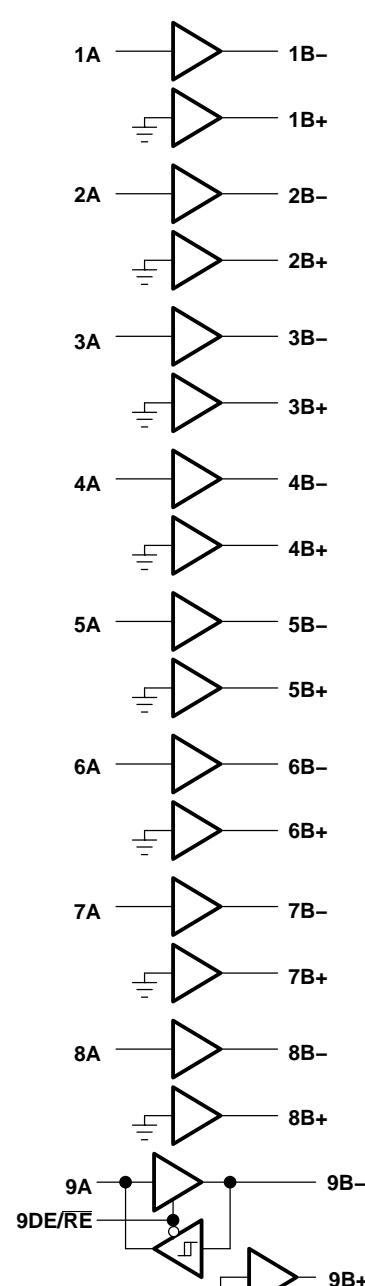
Figure 12. Logic Diagrams



(a)

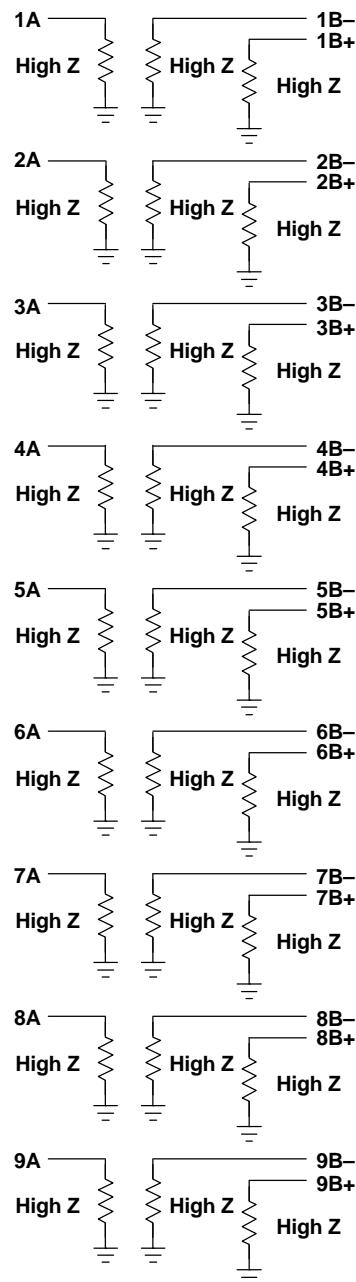


(b)



(c)

Figure 13. Logic Diagrams

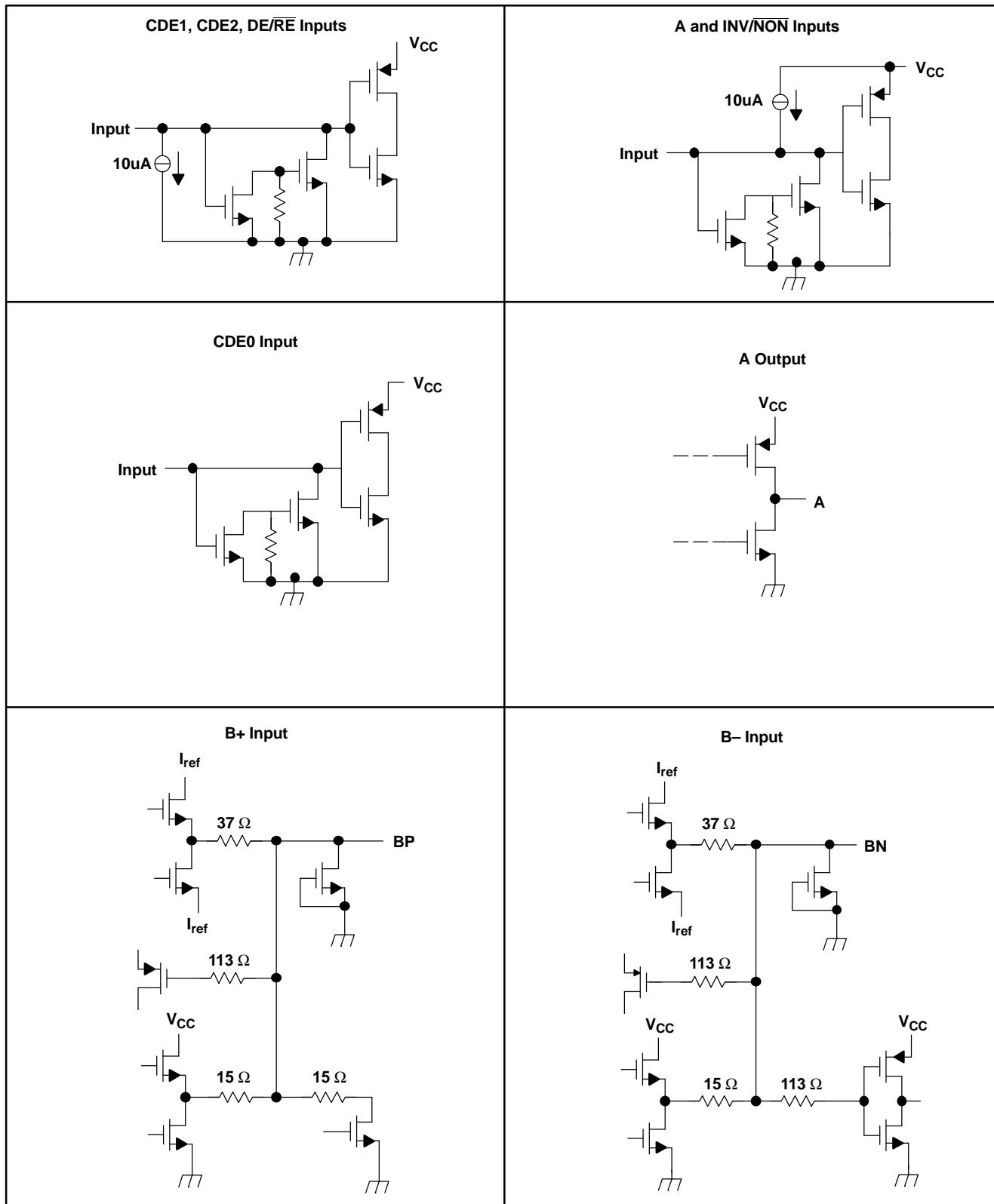


Control Inputs

CDE0	$V_I > 2.5 \text{ V}$
INV/NON	X
CDE1	X
CDE2	X

Figure 14. Logic Diagrams

INPUT AND OUTPUT EQUIVALENT SCHEMATIC DIAGRAMS



Terminal Functions

TERMINAL		'LVDM976 Logic Level	'LVDM977 Logic Level	I/O	Terminat ion	DESCRIPTION
NAME	NO.					
1A - 9A	4,6,8,10, 19,21,23, 25,27	CMOS	TTL	I/O	Pullup	1A - 9A carry data to and from the communication controller.
1B— 9B—	29,31,33, 35,37,46, 48,50,52	LVD or TTL	LVD or TTL	I/O	None	1B- to 9B- are the signals to and from the data bus. When INV/NON is low, the logic sense is the opposite that of the A input (inverted). When INV/NON is high, the logic sense is the same as the A input (noninverted).
1B+ - 9B+	30,32,34, 36,38,47, 49,51,53	LVD or GND	LVD or GND	I/O	None	When in the LVD mode, 1B+ - 9B+ are signals to or from the data bus and follow the same logic sense as the A input when INV/NON is low (noninverted). The logic sense is opposite that of the A input (inverted) when INV/NON is high. When in single-ended mode, these terminals become a ground connection through a transistor and do not switch.
CDE0	54	Trinary	Trinary	Input	None	CDE0 is the common driver enable 0. With the driver enabled and the CDE0 input less than 0.5 V, the driver output is single-ended mode. With the driver enabled and the CDE0 input between 0.7 V and 1.9 V the driver output is LVD mode. All drivers are disabled when the input is greater than 2.4 V.
CDE1	55	CMOS	TTL	Input	Pulldown	CDE1 is the common driver enable 1. When CDE1 is high, drivers 1–4 are enabled
CDE2	56	CMOS	TTL	Input	Pulldown	CDE2 is the common driver enable 2. When CDE2 is high, drivers 5 to 8 are enabled.
1DE/RE - 9DE/RE	5,7,9,11, 20,22,24, 26,28	CMOS	TTL	Input	Pulldown	1DE/RE-9DE/RE are direction controls that transmit data to the bus when it is high and CDE0 is below 2.2 V. Data is received from the bus when 1DE/RE- 9DE/RE, CDE1, and CDE2 are low.
GND	2,3,13,14, 15,16,17, 40,41,42, 43,44	NA	NA	Power	NA	GND is the circuit ground.
INV/NON	1	CMOS	CMOS	Input	Pullup	A high-level input to INV/NON inverts the logic to and from the A terminals. (i.e., the voltage at A terminal and the corresponding B-terminal are in phase.)
V _{CC}	12,18,39, 45	NA	NA	Power	NA	Supply voltage

ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
V _{CC}	Supply voltage range ⁽²⁾	-0.5 V to 7 V
V _I	(A, INV/NON)	-0.5 V to V _{CC} + 0.5 V
	(DE/RE, B+, B-, CDE0, CDE1, CDE2)	-0.5 V to 5.25 V
Continuous total power dissipation		See Dissipation Rating Table
T _{stg}	Storage temperature range,	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING
DGG	978 mW	10.8 mW/°C	492 mW

RECOMMENDED OPERATING CONDITIONS (see Figure 15)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IH}	High-level input voltage	0.7 V _{CC}			V
		2			
V _{IL}	Low-level input voltage	0.3 V _{CC}			V
		0.8			
V _{ID}	Differential input voltage	Differential receiver	0.03	3.6	V
V _{IC}	Common-mode input voltage		0.7	1.8	V
V _{OD(bias)}	Differential output voltage bias	Differential	100	125	mV
I _{OH}	High-level output current	Single-ended driver		7	mA
		Receiver		2	
I _{OL}	Low-level output current	Single-ended driver		48	mA
		Receiver		2	
Z _L	Differential load impedance		40	65	Ω
T _A	Operating free-air temperature		0	70	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{IH}	High-level input current	CDE1 and CDE2		50		μA
		INV/NON		50		
I _{IL}	Low-level input current	CDE1 and CDE2		50		μA
		INV/NON		50		
I _{CC}	Supply current	Disabled		7		mA
		LVD drivers enabled, No load		26		
		Single-ended drivers enabled, No load		10		
		LVD receivers enabled, No load		26		
		Singled-ended receivers enabled, No load		7		
C _I	Input capacitance	Bus terminal	V _I = 0.2 sin (2 π (1E06)t) + 0.5 ± 0.01 V	9.5		pF
ΔC _I	Difference in input capacitance between B+ and B-			0.2		

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

DIFFSENS (CDE0) RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT1}		0.5	0.6	0.7	
V_{IT2}		1.9	2.1	2.4	V
I_I	$0 \text{ V} \leq V_I \leq 2.7 \text{ V}$		± 1		μA
$I_{I(OFF)}$	$V_{CC} = 0, 0 \text{ V} \leq V_I \leq 2.7 \text{ V}$		± 1		μA

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

LVD DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$V_{OD(H)}$	$V_{I(1)} = 0.96 \text{ V}$, $V_{I(2)} = 0.53 \text{ V}$, See Figure 16	270	460	780	mV
		$0.69 V_{OD(L)} + 50$	$1.45 V_{OD(L)} - 65$		
$V_{OD(L)}$	$V_{I(1)} = 1.96 \text{ V}$, $V_{I(2)} = 1.53 \text{ V}$, See Figure 16	270	500	780	mV
		$0.69 V_{OD(L)} + 50$	$1.45 V_{OD(L)} - 65$		
$V_{OC(ss)}$	$V_{I(1)} = 0.96 \text{ V}$, $V_{I(2)} = 0.53 \text{ V}$, See Figure 16	260	400	640	mV
		$V_{I(1)} = 1.96 \text{ V}$, $V_{I(2)} = 1.53 \text{ V}$, See Figure 16	260	400	640
$V_{OC(ss)}$	Steady-state common-mode output voltage	1.1	1.2	1.5	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage between logic states		± 50	± 120	mV
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		80	150	mV
I_{IH}	High-level input current A	7			μA
			50		
I_{IL}	Low-level input current A		30		μA
		8			
$I_{O(OFF)}$	Power-off output current	$V_{CC} = 0, 0 \text{ V} \leq V_O \leq 2.5 \text{ V}$		± 1	μA
I_{OS}	Short-circuit output current	$0 \text{ V} \leq V_O \leq 2.5 \text{ V}$		± 24	mA
I_{OZ}	High-impedance output current	$V_O = 0 \text{ or } 2.5 \text{ V}$		± 1	μA

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

LVD DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted) (See [Figure 16](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	2.9	8.8		ns
t_{PHL}	Propagation delay time, high-to-low level output	2.9	8.8		ns
t_r	Differential output signal rise time	1	3	6	ns
t_f	Differential output signal fall time	1	3	6	ns
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)		3.7		ns
$t_{sk(lim)}$	Skew limit ⁽²⁾		5.9		ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output		50		ns
t_{en}	Enable time, receiver to driver		33		ns

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

(2) $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

SINGLE-ENDED DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage B- output	I _{OH} = -7 mA, See Figure 19	2	3.24	3.7	V
		I _{OH} = 0 mA			3.7	V
V _{OL}	Low-level output voltage B+	V _{CC} = 5 V, I _{OL} = 48 mA		0.5	0.5	V
		I _{OL} = -25 mA		-0.5	0.5	V
I _{IH}	High-level input current A DE/RE	V _{IH} = 3.3 V ('976), V _{IH} = 2 V ('977)	-7		50	μA
				-30	8	μA
I _{IL}	Low-level input current A DE/RE	V _{IL} = 1.6 V ('976), V _{IL} = 0.8 V ('977)		-30	8	μA
				50	8	μA
I _{O(OFF)}	Power-off output current	B-	V _{CC} = 0, 0 V ≤ V _O ≤ 5.25 V		±1	μA
I _{OZ}	High-impedance output current		V _O = 0 or V _{CC}		±1	μA

SINGLE-ENDED DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high level output t _{PHL} Propagation delay time, high-to-low level output t _r Differential output signal rise time t _f Differential output signal fall time t _{sk(p)} Pulse skew (t _{PHL} - t _{PLH}) t _{sk(lim)} Skew limit ⁽²⁾ t _{en} Enable time, receiver to driver	V _{CC} = 5 V, T _A = 25°C, See Figure 19	2.7	8.2	ns
t _{PLH}			2.7	8.2	ns
t _r			0.5	4	ns
t _f			0.5	4	ns
t _{sk(p)}				3.4	ns
t _{sk(lim)}				5.5	ns
t _{en}				50	ns
t _{PLZ}	Propagation delay time, low-level to high-impedance output	See Figure 20		30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) t_{sk(lim)} is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

LVD RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IT+}	Positive-going differential input voltage threshold See Figure 21		30		mV
V _{IT-}			-30		mV
V _{OH}	I _{OH} = -2 mA	3.7			V
V _{OL}	I _{OL} = 2 mA		0.5		V
I _I	I _I = 0 V to 2.5 V		±1		μA
I _{I(OFF)}	V _{CC} = 0, V _I = 0 V to 2.5 V		±1		μA
I _{IH}	V _{IH} = 3.3 V ('976), V _{IH} = 2 V ('977)		50		μA
I _{IL}	V _{IL} = 1.6 V ('976), V _{IL} = 0.8 V ('977)	8			μA
I _{OZ}	V _O = 0 or V _{CC}		±30		μA

LVD RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, See Figure 21	4.5	10	ns	
t_{PHL}		4.5	10	ns	
$t_{sk(p)}$			3	ns	
t_r			8	ns	
t_f			8	ns	
$t_{sk(lim)}$			5.5	ns	
t_{PHZ}	See Figure 18		42	ns	
t_{PLZ}			20	ns	
t_{en}			26	ns	

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

(2) $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

SINGLE-ENDED RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input voltage threshold B—		1.6	1.9	V
V_{IT-}		1	1.1		V
V_{OH}	High-level output voltage	$I_{OH} = -2 \text{ mA}$	3.7	4.6	V
V_{OL}	Low-level output voltage	$I_{OL} = 2 \text{ mA}$	0.3	0.5	V
I_I	Input current	$V_I = 0 \text{ to } V_{CC}$		± 1	μA
$I_{I(OFF)}$	Power-off Input current	$V_{CC} = 0 \text{ V}$, $V_I = 0 \text{ to } 5.25 \text{ V}$		± 1	μA
I_{IH}	High-level input current	$V_{IH} = 3.3 \text{ V}$ ('976), $V_{IH} = 2 \text{ V}$ ('977)		50	μA
I_{IL}	Low-level input current	$V_{IL} = 1.6 \text{ V}$ ('976), $V_{IL} = 0.8 \text{ V}$ ('977)	8		μA
I_{OZ}	High-impedance output current	$V_O = 0 \text{ or } V_{CC}$		-30	μA

SINGLE-ENDED RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, See Figure 22	7	12.5	ns	
t_{PHL}		7	12.5	ns	
$t_{sk(p)}$			3.5	ns	
t_r			8	ns	
t_f			8	ns	
$t_{sk(lim)}$			5.5	ns	
t_{PHZ}	See Figure 20		20	ns	
t_{PLZ}			30	ns	
t_{en}			48	ns	

(1) $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

PARAMETER MEASUREMENT INFORMATION

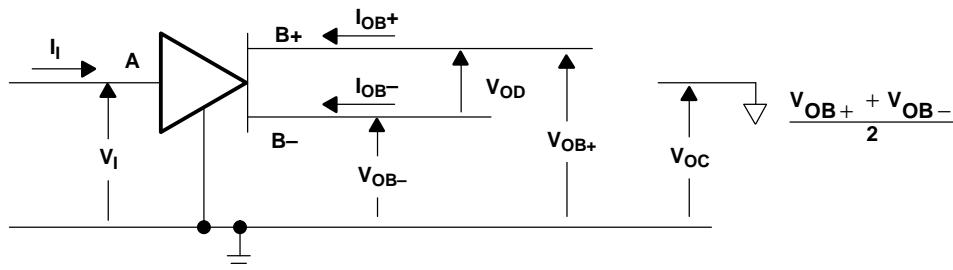
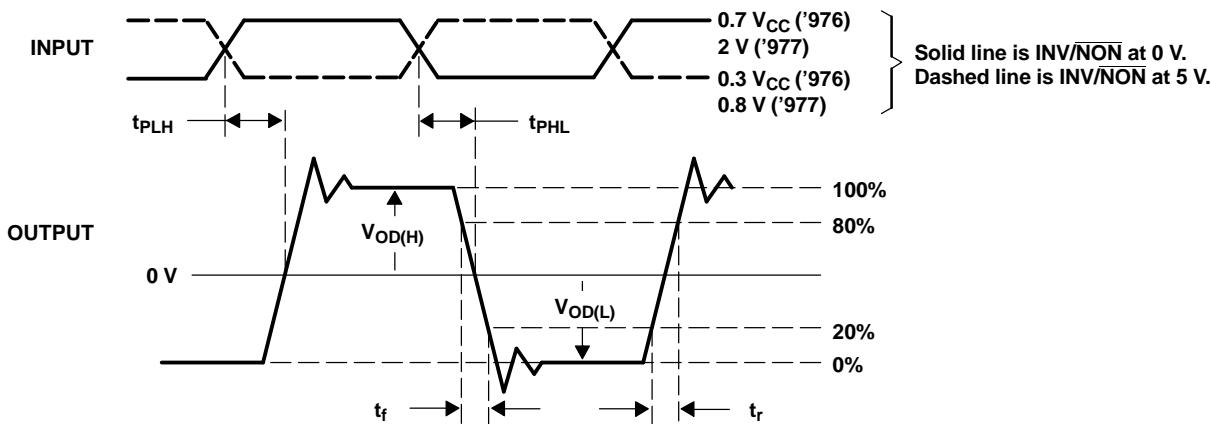
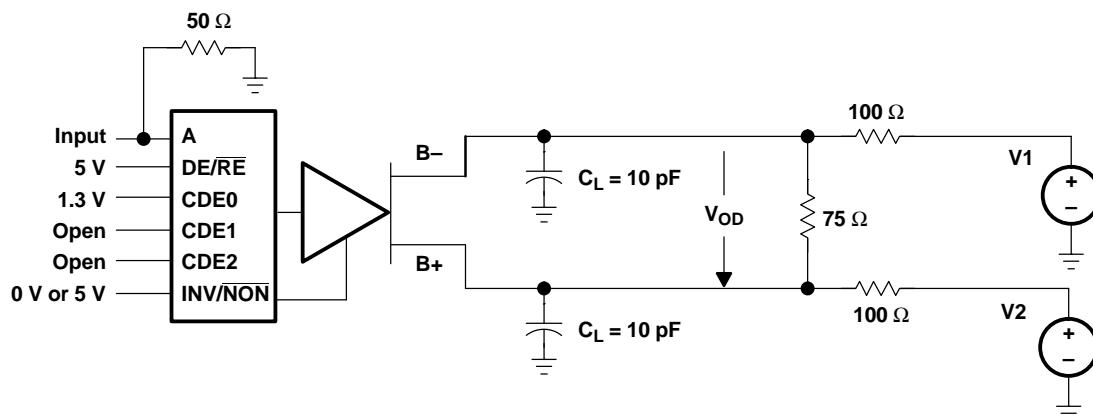


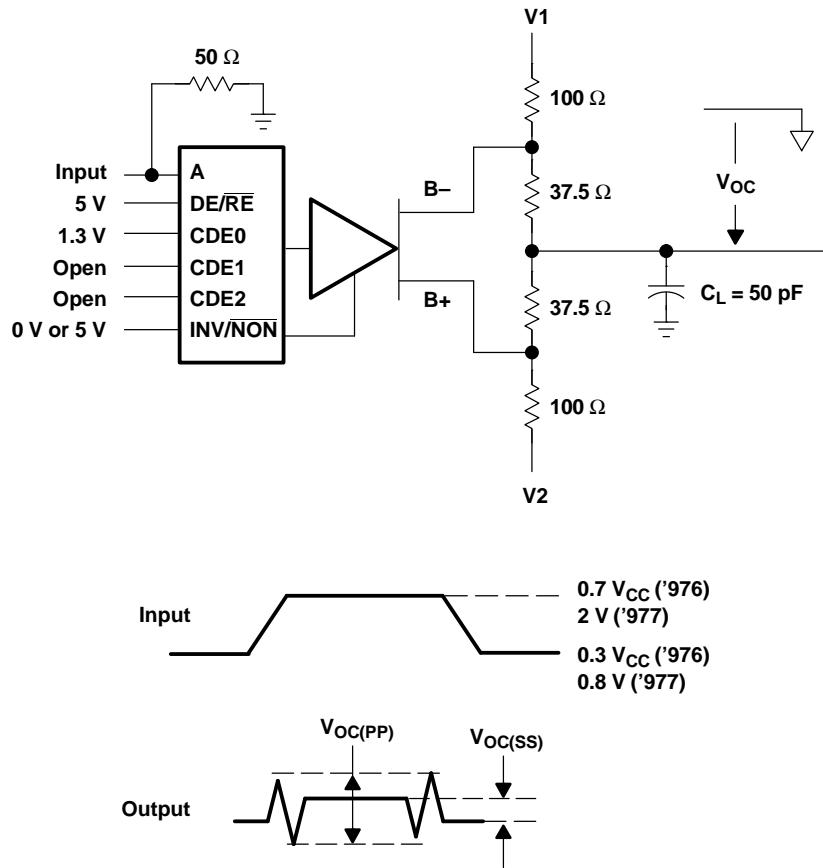
Figure 15. Voltage and Current Definitions



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f < 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ± 5 ns, $Z_o = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 16. Differential Output Signal Test Circuit, Timing, and Voltage Definitions

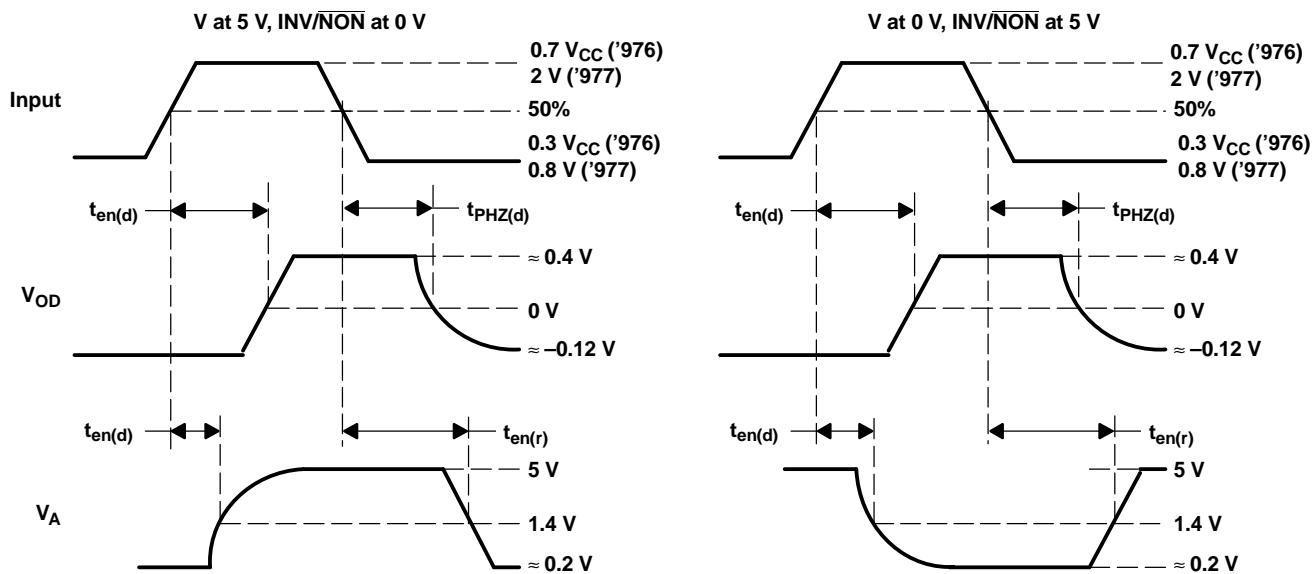
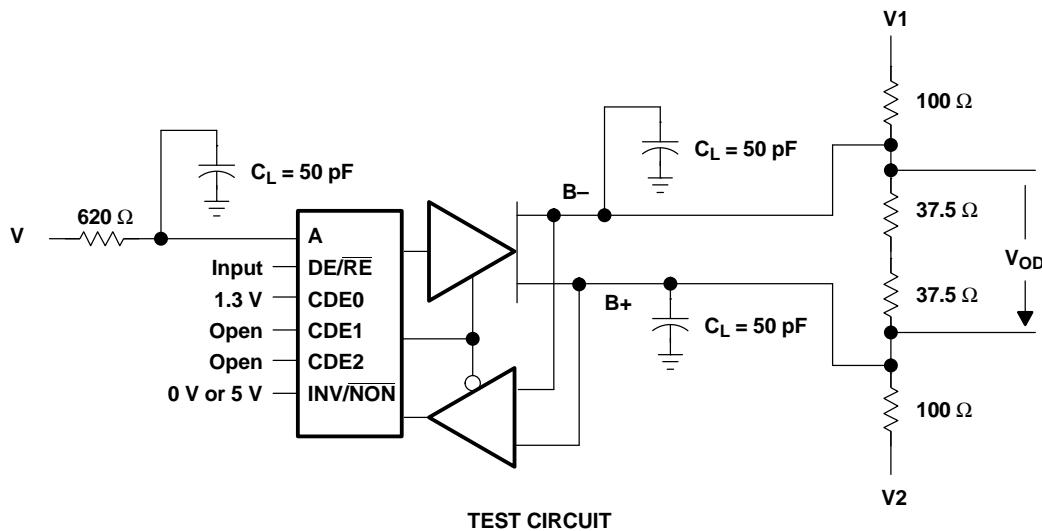
PARAMETER MEASUREMENT INFORMATION (continued)



- A. NOTES: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulselwidth = 50 ns ± 5 ns, $Z_o = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.
- C. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 17. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

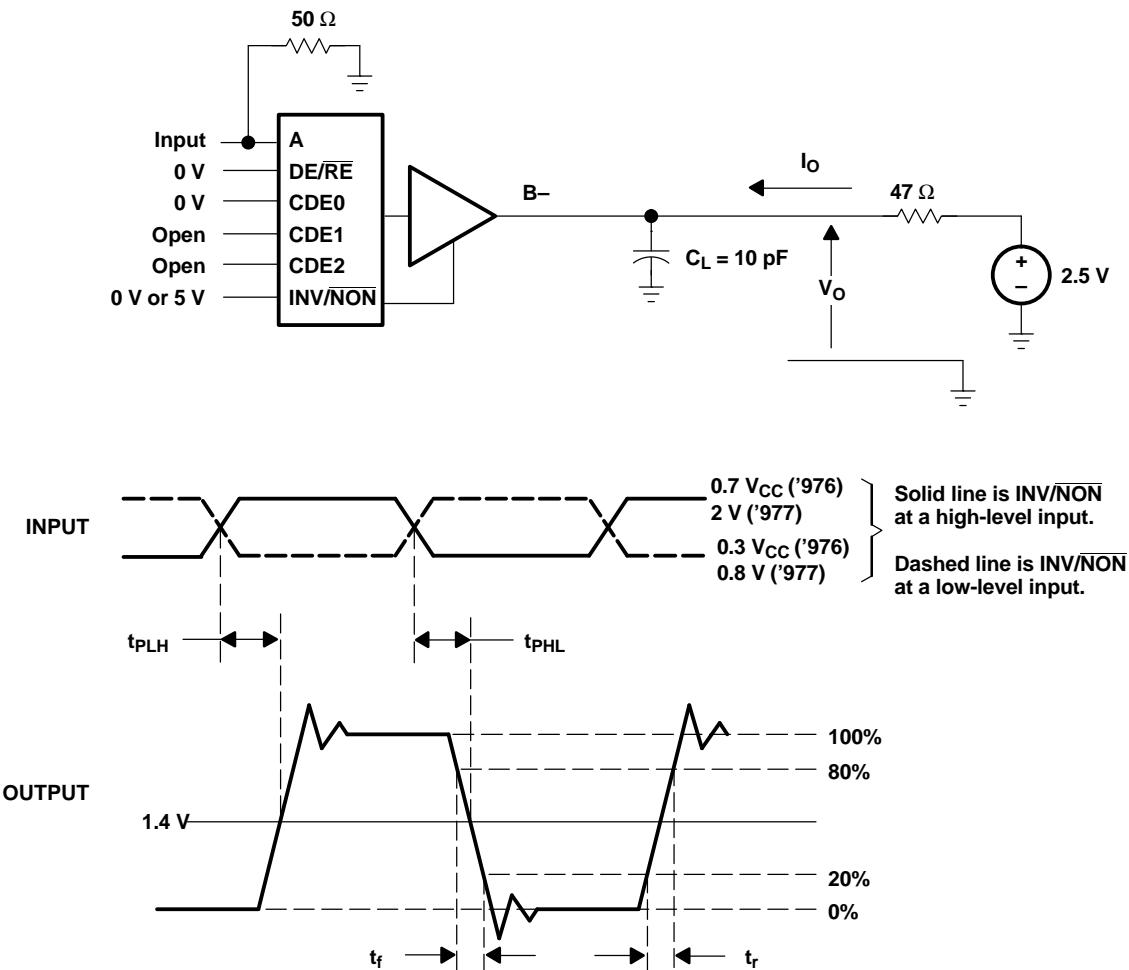
PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulselwidth = 500 ns ± 50 ns, $Z_o = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 18. LVD Transceiver Enable and Disable Time Test Circuit and Definitions

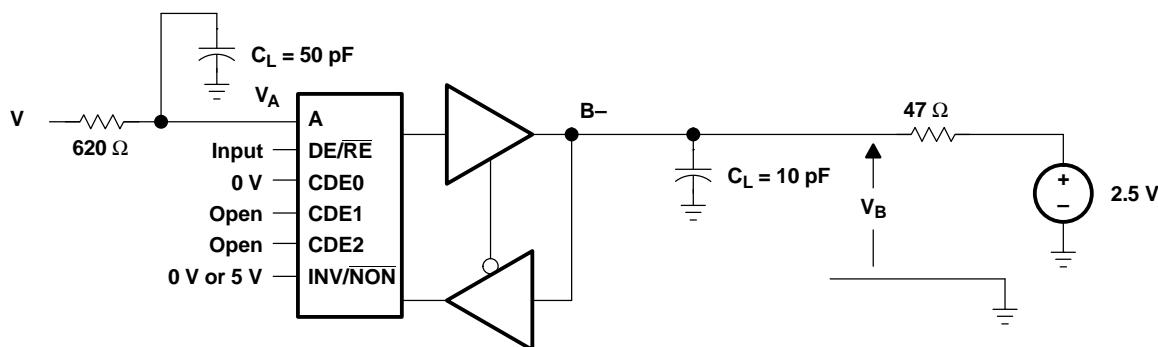
PARAMETER MEASUREMENT INFORMATION (continued)



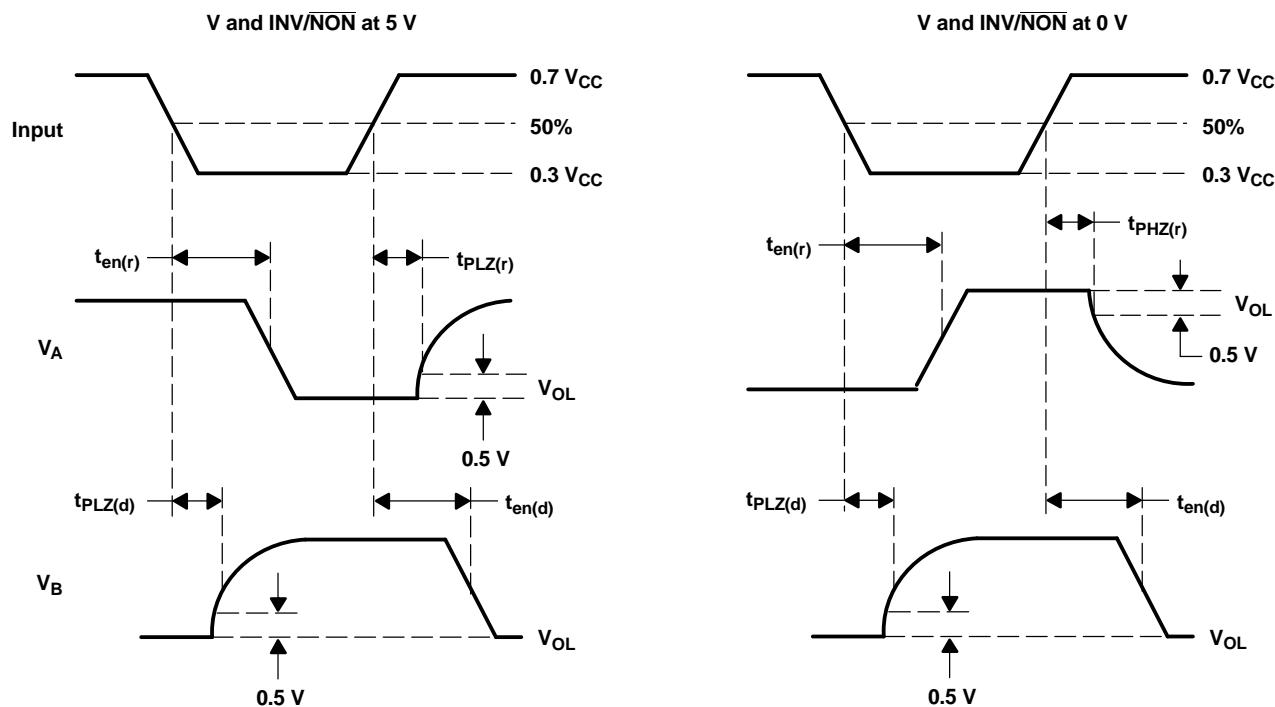
- A. All input pulses are supplied by a generator having the following characteristics: t_f or $t_r < 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ± 5 ns, $Z_o = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 19. Single-Ended Driver Switching Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulselwidth = 500 ns ± 50 ns, $Z_o = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 20. Single-Ended Transceiver Enable and Disable Timing Measurements

PARAMETER MEASUREMENT INFORMATION (continued)

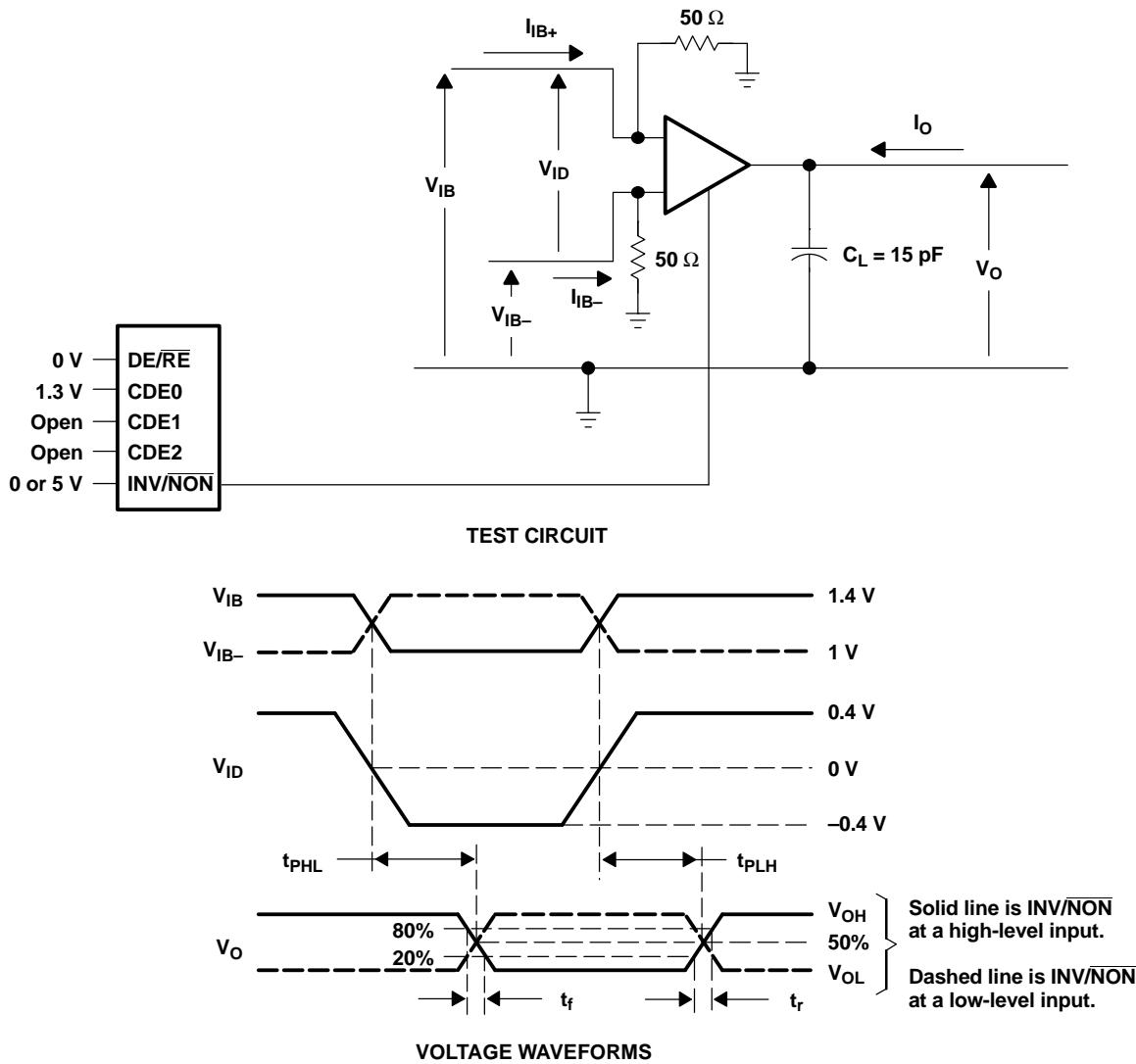
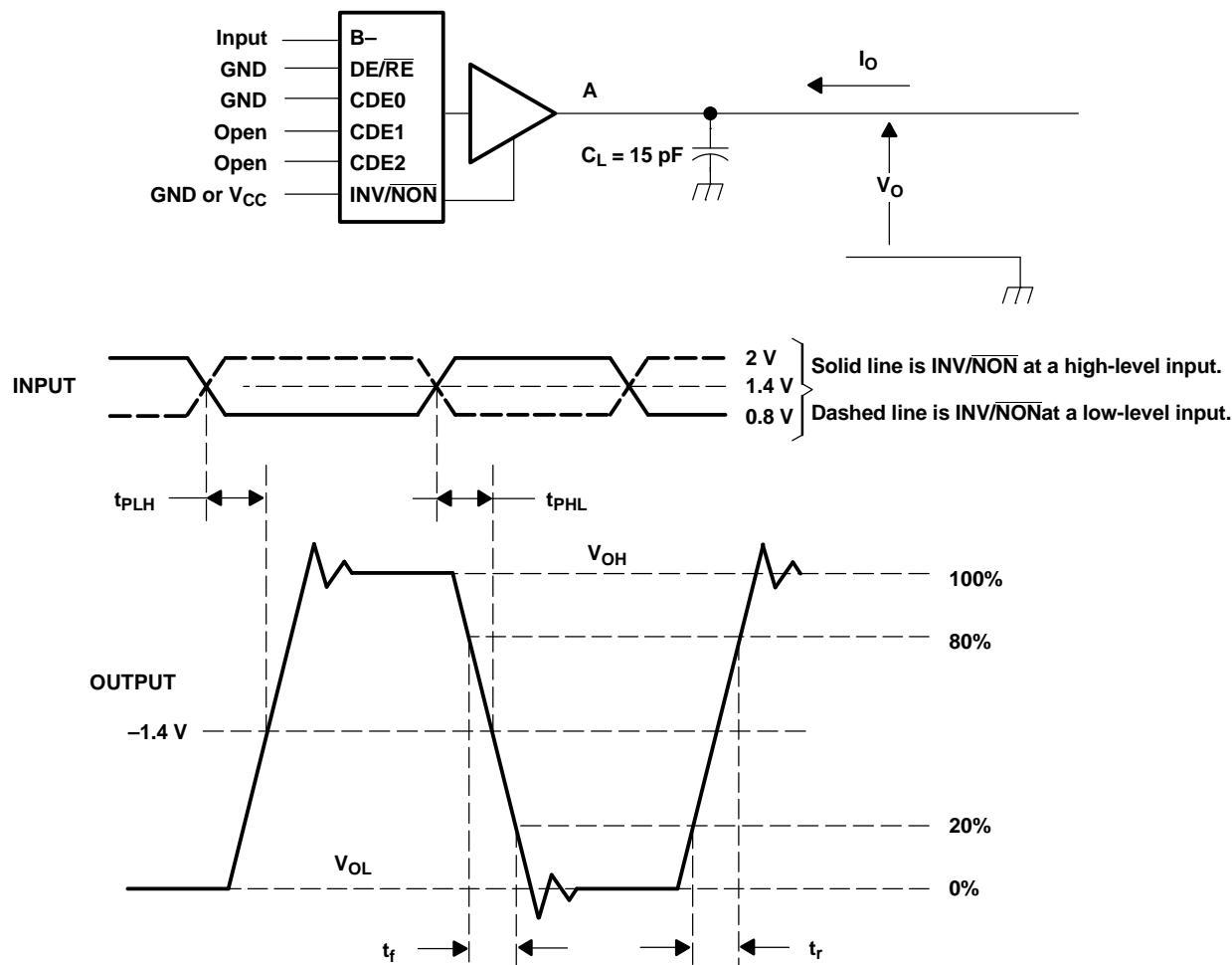


Figure 21. LVD Receiver Switching Characteristic Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics: t_f or $t_r < 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ± 5 ns.
- B. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 22. Single-Ended Receiver Timing Test Circuit

APPLICATION INFORMATION

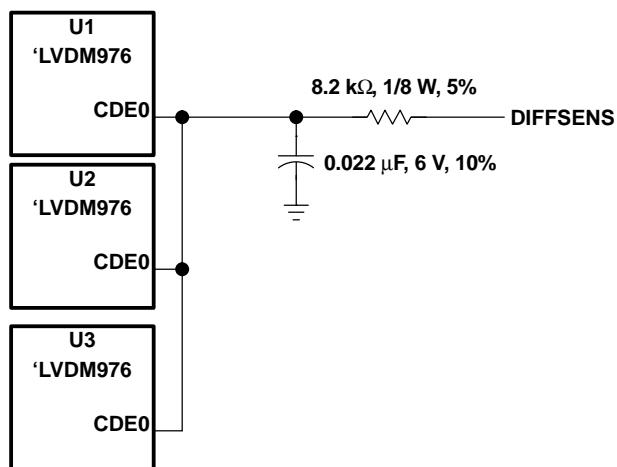


Figure 23. Low-Pass Filter for Connecting DIFFSENS to CDE0

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Mailing Address: Texas Instruments
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