TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9322FA,TC9322FB

Single Chip DTS Microcontroller (DTS-21)

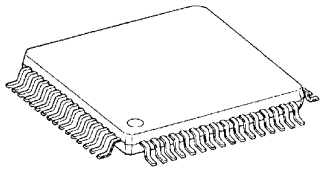
The TC9322FA and TC9322FB are a 4 bit CMOS microcontroller for signal chip digital tuning systems. It is capable of functioning at a low voltage of 3 V and features a built-in prescaler of operating 230 MHz, PLL and LCD drivers.

The CPU has 4 bit parallel addition and subtraction instructions (e.g., AI, SI), logic operation instructions (e.g., OR, AND), composite judging and compare instructions (e.g., TM, SL), and time-base functions.

The package is an pin 64, 0.5/0.65-mm-pitch quad flat pack package. In addition to various input/output ports and a dedicated key-input port, which are controlled by powerful input/output instructions (IN 1, 2, OUT 1, 2), there are many dedicated LCD pins, a buzzer port, a 6 bit A/D converter, an IF counter, and other pins.

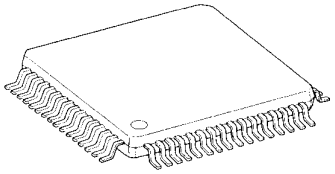
Low-voltage and low-current consumption make this microcontroller suitable for portable DTS equipment.

TC9322FA



LQFP64-P-1010-0.50

TC9322FB



QFP64-P-1212-0.65

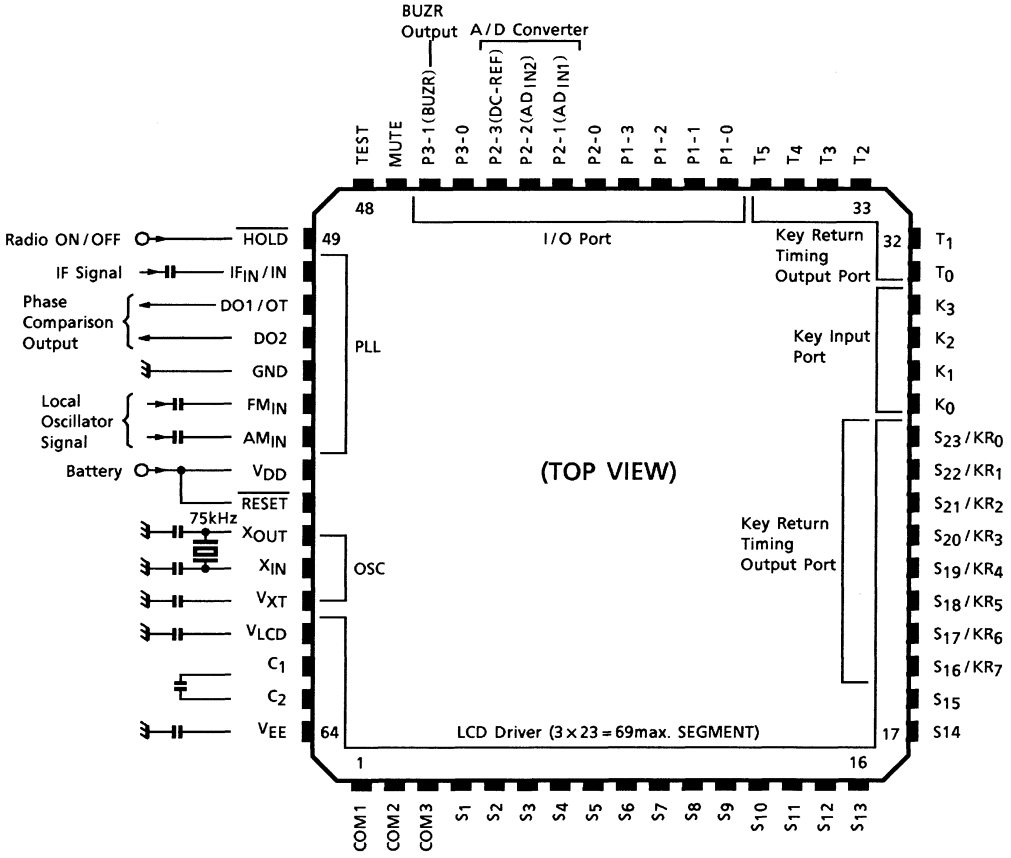
Weight
LQFP64-P-1010-0.50: 0.32 g (typ.)
QFP64-P-1212-0.65: 0.45 g (typ.)

Features

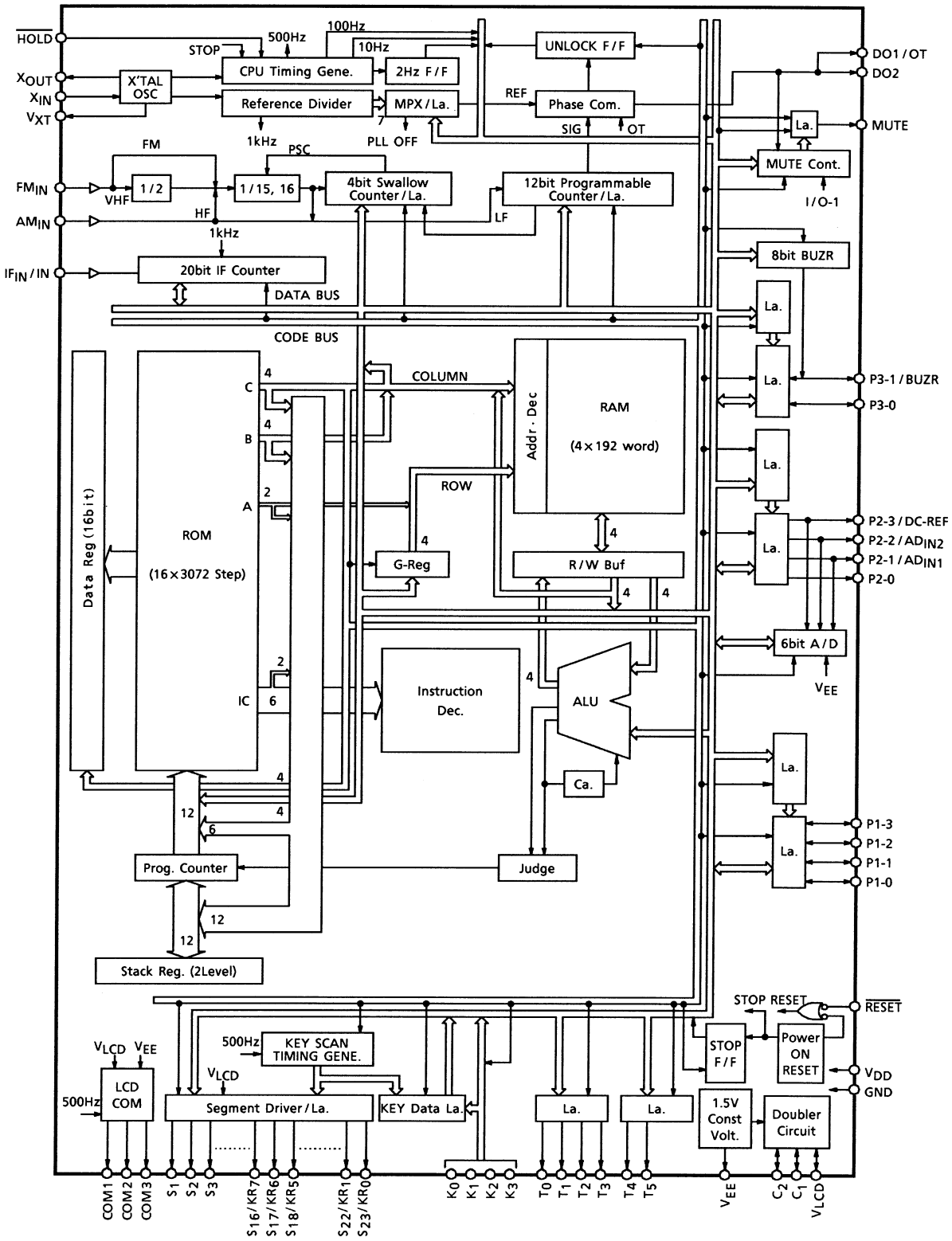
- 4 bit microcontroller for digital tuning systems.
- Operating voltage V_{DD} = 1.8~3.6 V, with low current consumption because of CMOS circuitry (with only CPU operating, when V_{DD} = 3 V, I_{DD} = 80 μA max)
- Built-in prescaler (1/2 fixed divider +2 modulus prescaler: fmax ≧ 230 MHz)
- Features built-in 1/3-duty, 1/2-bias LCD drivers and a built-in 3 V booster circuit for the display.
- Data memory (RAM) and ports are easily backed up.
- Program memory (ROM): 16 bit × 3072 steps
- Data memory (RAM): 4 bit× 192 words
- 60-instruction set (all one-word instructions)
- Instruction execution time: 40 μs (with 75 kHz crystal) (MVGS, DAL instructions: 80 μs)
- Many addition and subtraction instructions (12 types addition, 12 types subtraction)
- Powerful composite judging instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN)
- Data can be transmitted between addresses on the same row. (MVSR instruction)
- Register indirect transfer available (MVGD, MVGS instruction).
- 16 powerful general registers (located in RAM)
- Stack levels: 2
- JUMP or CAL instruction can be used anywhere in the 3072 steps of program memory (ROM) as there are no pages or fields.
- 16 bit of any address in the 1024 steps in program memory (ROM) can be referenced (DAL instruction).
- Features independent frequency input pins (FM_{IN} and AM_{IN}) and two (DO1 and DO2) phase comparison outputs for FM/VHF and AM.
- Seven reference frequencies can be selected by program.
- Powerful input/output instructions (IN 1, 2, OUT 1, 2)
- Dedicated input ports (K_0~K_3) for key input. 26 LCD drive pins (69 segments maximum) available.
- 17 I/O ports: 10 with input/output programmable in 1bit units, and 7 output-only port. The 2 IF_{IN}, and DO1 pins can be switched by instruction to IN (input-only) or OT (output-only).

- Three back-up modes available by instruction: only CPU operation, crystal oscillation only, clock stop.
- Features a built-in 2 Hz timer F/F and a built-in 10/100 Hz interval pulse output (internal port for time base).
- Allows PLL lock status detection.
- 8 of the LCD segment outputs (S_{16}~S_{23}) can also operate as key return timing outputs (KR_0~KR_7). The I/O ports are not dedicated key return timing outputs but can have other uses as well.
- Built-in 20 bit, general-purpose IF counter can detect stations during auto-tuning by counting the intermediate frequencies of each band.
- Built-in 8 bit buzzer output circuit can produce 254 different tone signals.
- Features a built-in 2-channel, 6 bit A/D converter.
- To prevent CPU malfunctions, a built-in supply voltage drop detection circuit shuts down the CPU when voltage falls below 1.5 V.

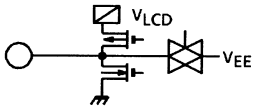
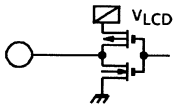
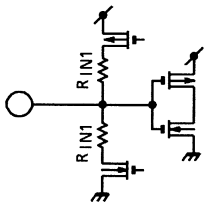
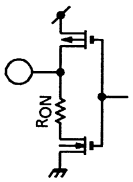
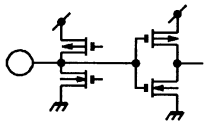
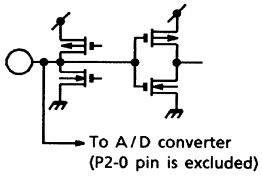
Pin Assignment (top view)

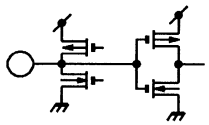
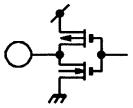
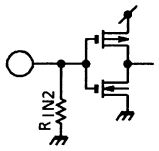
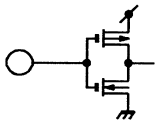


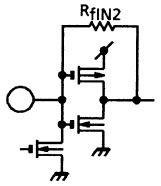
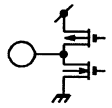
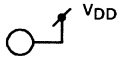
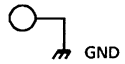
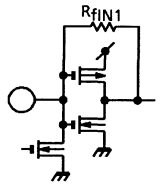
Block Diagram

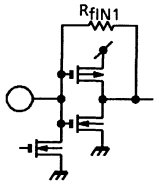
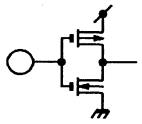
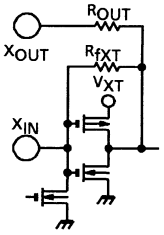
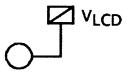


Explanation of Function

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	COM1	LCD common outputs	Output common signals to the LCD panel. Through a matrix with pins S_1~S_{23}, a maximum of 69 segments can be displayed. Three levels, V_{LCD}, V_{EE}, and GND, are output at 83 Hz every 2 ms. V_{EE} is output after SYSTEM RESET and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0".	
2	COM2			
3	COM3			
4~18	S_1~S_{15}	LCD segment output	Segment signal output pins for the LCD panel. Together with COM1, COM2, and COM3, a matrix is formed that can display a maximum of 69 segments. The signals for the key matrix and the segment signals from pins S_{16}/KR_7~S_{23}/KR_0 are output on a time division basis. $4 \times 8 = 32$ key matrix can be created in conjunction with key input ports K_0~K_3.	
19~26	S_{16}/KR_7~ S_{23}/KR_0	LCD segment output/Key return timing output		
27~30	K_0~K_3	Key input ports	4 bit input ports for key matrix input. Combined in a matrix with key return timing outputs of the LCD segment pins, data from a maximum of $4 \times 8 = 32$ keys can be input and pins are pulled up. On the key seteutining output pins, data from $4 \times 6 = 24$ keys can be input and pins are pulled down. The WAIT mode is released when high level is applied to key input ports set to pull-down.	
31~36	T_0~T_5	Key return timing output port	These ports output the timing signal for key matrix. To form the key matrix, load resistance has been built-in the N-channel side. When the key matrix combined with push-key, that does not need a key matrix diode.	
37~40	P1-0~P1-3	I/O port 1	The input and output of these 4 bit I/O ports can be programmed in 1 bit units. By altering the input to I/O ports set to input, the CLOCK STOP and WAIT modes can be released, and the MUTE bit of the MUTE pin can be set to "1".	
41~44	P2-0 P2-1/AD_{IN1} P2-2/AD_{IN2} P2-3/ DC-REF	I/O port 2 /AD analog voltage input /AD analog voltage input /Reference voltage input	4 bit I/O ports. Input and output may be programmed in 1 bit units. Pins P2-1 through P2-2 can also be used for analog input to the built-in 6 bit, 2-channel A/D converter. Conversion time of the built-in A/D converter using the successive comparison method is 280 μs. The necessary pin can be programmed to AD analog input in 1 bit units, and P2-3 can be set to the reference voltage input. Internal power supply (V_{DD}) or constant voltage (V_{EE}) can be used as the reference voltage. In addition, constant voltage (V_{EE}) can be input to the AD analog input so battery voltage, etc., can be easily detected. The reference voltage input, for which a built-in operational amp is used, has high impedance. The A/D converter, and their control are all executed by program.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
45~46	P3-0 P3-1/BUZR	I/O port 3 /Buzzer output	2 bit I/O ports, whose input/output can be programmed in 1 bit units. The P3-1 pin also functions as the output for the built-in buzzer circuit. The buzzer sound can be output in 254 different tones between 18.75 kHz and 147 Hz, and at a duty of 50%. The buzzer output, and all associated controls can be programmed.	
47	MUTE	Muting output port	1 bit output port. Normally, this port is used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input of I/O port 1. MUTE bit output logic can be changed; PLL phase difference can also be output using this pin.	
48	TEST	TEST mode control input	Input pin used for controlling TEST mode. High level indicates TEST mode, while low level indicates normal operation. The pin is normally used at low level or no-connection (NC). (a pull-down resistor is built-in).	
49	$\overline{\text{HOLD}}$	HOLD mode control input	Input pin for request/release HOLD mode. Normally, this pin is used to input radio mode selection signals or battery detection signals. HOLD mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request/release of the HOLD mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the $\overline{\text{HOLD}}$ pin is at low level stops the clock generator and the CPU and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the $\overline{\text{HOLD}}$ pin. Memory back-up is released when the $\overline{\text{HOLD}}$ pin goes high in MODE-0, or when the level of the $\overline{\text{HOLD}}$ pin level in MODE-1. When memory back-up mode is entered by executing a WAIT instruction, any change in the $\overline{\text{HOLD}}$ pin input releases the mode. In memory back-up mode, current consumption is low (below 10 μA), and all the output pins (e.g., display output, output ports) are automatically set to low level.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
50	IF_{IN}/IN	IF signal input/Input port	IF counter's IF signal input pin for counting the IF signals of the FM and AM bands and detecting the automatic stop position. The input frequency is between 0.35~12 MHz (0.2 V_{p-p} (min)). A built-in input amp and C coupling allow operation at low-level input. The IF counter is a 20 bit counter with optional gate times of 1, 4, 16, and 64 ms. 20 bits of data can be readily stored in memory. This input pin can be programmed for use as an input port (IN port). CMOS input is used when the pin is set as an IN port.	
51 52	DO1/OT DO2	Phase comparison output /Output port Phase comparison output	PLL's phase comparison tri-state output pins. When the programmable counter's prescaler output is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, output is at low level. When output equals the reference frequency, high impedance output is obtained. Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for the FM/VHF and AM bands. Pin DO1 can be programmed to high impedance or programmed as an output port (OT). Thus, the pins can be used to improve lock-up time or used as output ports.	
56	V_{DD}	Power-supply pins	Pins to which power is applied. Normally, V_{DD} = 1.8~3.6 V (3.0 V typ.) is applied. In back-up mode (when CKSTP instructions are being executed), voltage can be lowered to 1.0 V. If voltage falls below 1.5 V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the voltage rises above 1.5 V, the CPU restarts. STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program. When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated and rendered non-operative by program. In that case, all four bits of the internal TEST port should be set to "1". If more than 1.8 V is applied when the pin voltage is 0, the device's system is reset and the program starts from address "0". (power on reset) Note: To operate the power on reset, the power supply should start up in 10~100 ms.	
53	GND			
54	FM_{IN}	FM programmable counter input	Programmable counter input pin for FM, VHF band. The 1/2 + pulse swallow system (VHF mode) and the pulse swallow system (FM mode) are selectable freely by program. At the VHF mode, local oscillation output (VCO output) of 50~230 MHz (0.2 V_{p-p} (min)) is input and FM mode, 40~130 MHz (0.2 V_{p-p} (min)) is input. A built-in input amp and C coupling allow operation at low-level input. Note: When in the PLL OFF mode or when set to AM_{IN} input, the input is pulled down.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
55	AM_{IN}	AM local oscillator signal input	Programmable counter input pin for AM band. The pulse swallow system (HF mode) and direct dividing system (LF mode) are freely selectable by program. At the HF mode, local oscillation output (VCO output) of 1~45 MHz (0.2 V_{p-p} (min)) is input and LF mode, 0.5~12 MHz (0.2 V_{p-p} (min)) is input. Built-in input amp operates with low-level input using a C coupling. Note: When in PLL OFF mode or when set to FM_{IN} input, the input is pulled down.	
57	$\overline{RESET}$	Reset input	Input pin for system reset signals. $\overline{RESET}$ takes place while at low level; at high level, the program starts from address "0". Normally, if more than 1.8 V is supplied to V_{DD} when the voltage is 0, the system is reset (power on reset). Accordingly, this pin should be set to high level during operation.	
58	X_{OUT}	Crystal oscillator pins	Crystal oscillator pins. A reference 75 kHz crystal oscillator is connected to the X_{IN} and X_{OUT} pins. The oscillator stops oscillating during CKSTP instruction execution. The V_{XT} pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47 μF typ.) is connected.	
59	X_{IN}			
60	V_{XT}			
61	V_{LCD}	Voltage doubler boosting pin	Voltage doubler boosting pin for driving the LCD. A capacitor (0.1 μF typ.) is connected to boost the voltage. The V_{LCD} pin outputs voltage (3.0 V), which has been doubled from the constant voltage (V_{EE}: 1.5 V) using the capacitors connected between C_1 and C_2. That potential is supplied to the LCD drivers. If the internal V_{LCD} OFF bit is set to "1" by program, an external power supply can be input through the V_{LCD} pin to drive the LCD. At this time, the $V_{LCD}/2$ potential, whose V_{LCD} voltage is divided using registers, is output from the C_2 pin.	
62	C_1			
63	C_2			
64	V_{EE}	Constant voltage supply pin	1.5 V constant voltage supply pin for driving the LCD. A stabilizing capacitor (0.1 μF typ.) is connected. This is a reference voltage for the A/D converter, key input, and the LCD common output's bias potential.	—

Note 1: When the device is reset (voltage higher than 1.8 V, or when $\overline{RESET}$ = low → high) I/O ports are set to input, the pins for I/O ports and additional functions (e.g., A/D converter) are set to I/O port input pins, while the IF_{IN}/IN pins become IF input pins.

Note 2: When in PLL OFF mode (when the three bits in the internal reference ports all show "1"), the IF_{IN} and FM_{IN}, AM_{IN} pins are pulled down, and DO1 and DO2 are at high impedance.

Note 3: When in CLOCK STOP mode (during execution of CKSTP instruction), the output ports and the LCD output pins are all at low level, while the constant voltage circuit (V_{EE}), the voltage doubler circuit (V_{LCD}), and the power supply for the crystal oscillator (V_{XT}) are all off.

Note 4: When the device is being reset, the contents of the output ports and internal ports are undefined and initialization by program is necessary.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~4.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	100	mW
Operating temperature	T_{opr}	−10~60	°C
Storage temperature	T_{stg}	−55~125	°C

Electrical Characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 3.0 V)

Characteristics	Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Range of operating supply voltage	V_{DD}	—	*		1.8	3.0	3.6	V
Range of memory retention voltage	V_{HD}	—	Crystal ocillation stopped * (CKSTP instruction executed)		1.0	~	3.6	V
Operating current	I_{DD1}	—	Under ordinary operation and PLL on operation, no output load FM_{IN} = 230 MHz input	V_{DD} = 3.0 V	—	7.0	12	mA
		—	Under ordinary operation and PLL on operation, no output load FM_{IN} = 130 MHz input	V_{DD} = 3.0 V	—	6.0	10	
	I_{DD2}	—	Under CPU operation only (PLL off, display turned on)	V_{DD} = 3.0 V	—	40	80	μA
	I_{DD3}	—	Soft Wait mode (crystal oscllator, display circuit operating, CPU stopped, PLL off)		—	25	50	
	I_{DD4}	—	Hard Wait mode (crystal oscillator operating only)		—	15	30	
Memory retention current	I_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)		—	0.1	10	μA
Crystal oscillation frequency	f_{XT}	—	*		—	75	—	kHz
Crystal oscillation startup time	t_{ST}	—	Crystal oscillation f_{XT} = 75 kHz		—	—	1.0	s

Note 5: For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8~3.6 V, Ta = −10~60°C.

Voltage Doubler Circuit

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Voltage doubler reference voltage	V_{EE}	—	GND reference (V_{EE})	1.3	1.5	1.7	V
Constant voltage temperature characteristics	D_V	—	GND reference (V_{EE})	—	−5	—	mV/°C
Voltage doubler boosting voltage	V_{LCD}	—	GND reference (V_{LCD})	2.6	3.0	3.4	V

Operating Frequency Ranges for Programmable Counter and IF Counter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FM_{IN} (VHF mode)	f_{VHF}	—	Sine wave input when V_{IN} = 0.2 V_{p-p} *	50	~	230	MHz
FM_{IN} (FM mode)	f_{FM}	—	Sine wave input when V_{IN} = 0.2 V_{p-p} *	40	~	130	MHz
AM_{IN} (HF mode)	f_{HL}	—	Sine wave input when V_{IN} = 0.2 V_{p-p} *	1	~	45	MHz
AM_{IN} (LF mode)	f_{LF}	—	Sine wave input when V_{IN} = 0.2 V_{p-p} *	0.5	~	12	MHz
IF_{IN}	f_{IF}	—	Sine wave input when V_{IN} = 0.2 V_{p-p} *	0.35	~	12	MHz
Input amplitude	V_{IN}	—	FM_{IN}, AM_{IN}, IF_{IN} input *	0.2	~	V_{DD} − 0.8	V_{p-p}

Note 5: For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8~3.6 V, Ta = −10~60°C.

LCD Common Output/Segment Output (COM1~COM3, S_1~S_{23})

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{LCD} = 3 V, V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL1}	—	V_{LCD} = 3 V, V_{OL} = 0.3 V	0.5	1.0	—	
Output voltage 1/2 level		V_{BS}	—	No load	1.3	1.5	1.7	V

$\overline{HOLD}$ Input Port

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH1}	—	—	2.4	~	3.0	V
	"L" level	V_{IL1}	—	—	0	~	1.2	

A/D Converter (A/D_{IN1}, A/D_{IN2}, DC-REF)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	V_{AD}	—	AD_{IN1}, AD_{IN2}	0	~	V_{DD}	V
Analog reference voltage range	V_{REF}	—	DC-REF, V_{DD} = 2.0~3.6 V	1.0	~	V_{DD} × 0.9	V
Resolution	V_{RES}	—	—	—	6.0	—	bit
Conversion total error	—	—	V_{DD} = 2.0~3.6 V	—	±1.0	±4.0	LSB
Analog input leak	I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V (AD_{IN1}, AD_{IN2}, DC-REF)	—	—	±1.0	μA

KEY Input Port (K_0~K_3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
N-ch/P-ch input resistance		R_{IN1}	—	—	75	150	300	kΩ
Input voltage	"H" level	V_{IH2}	—	When input with pull-down resistance	1.8	~	3.0	V
	"L" level	V_{IL2}	—	When input with pull-down resistance	0	~	0.3	
Input voltage	"H" level	V_{IH3}	—	When input with pull-up resistance	2.7	~	3.0	V
	"L" level	V_{IL3}	—	When input with pull-up resistance	0	~	1.2	
Input leak current		I_{LI}	—	When input resistance off, V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA

Timing Output Port (T0~T5)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.3 V, Use LCD key-return mode	0.5	1.0	—	
N-ch load resistance		R_{ON}	—	No used LCD key-return mode	75	150	300	kΩ

DO1/OT, DO2 Output; MUTE Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.3 V	0.5	1.0	—	
Output off leak current		I_{TL}	—	V_{TLH} = 3.0 V, V_{TLL} = 0 V (DO1, DO2)	—	—	±100	nA

General-Purpose I/O Ports (P1-0~P3-1)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.3 V	0.5	1.0	—	
Input leakage current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH4}	—	—	2.4	~	3.0	V
	"L" level	V_{IL4}	—	—	0	~	0.6	

IN, $\overline{\text{RESET}}$ Input Ports

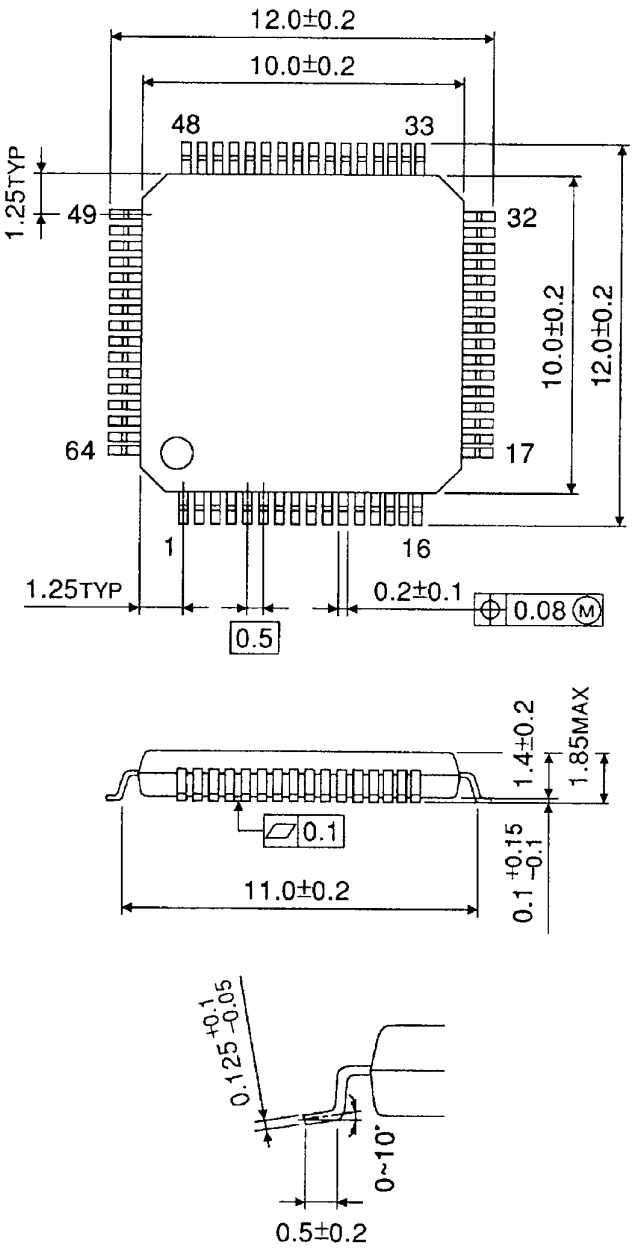
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leakage current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH4}	—	—	2.4	~	3.0	V
	"L" level	V_{IL4}	—	—	0	~	0.6	

Others

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pull-down resistance	R_{IN2}	—	(TEST)	25	50	100	kΩ
X_{IN} amp feedback resistance	R_{fXT}	—	(X_{IN}-X_{OUT})	—	20	—	MΩ
X_{OUT} output resistance	R_{OUT}	—	(X_{OUT})	—	3	—	kΩ
Input amp feedback resistance	R_{fIN1}	—	(FM_{IN}, AM_{IN})	150	300	600	kΩ
	R_{fIN2}	—	(IFM_{IN})	500	1000	2000	
Voltage used to detect supply voltage drop	V_{STP}	—	(V_{DD})	1.3	1.5	1.6	V
Supply voltage drop detection temperature characteristics	D_S	—	(V_{DD})	—	−2	—	mV/°C

Package Dimensions

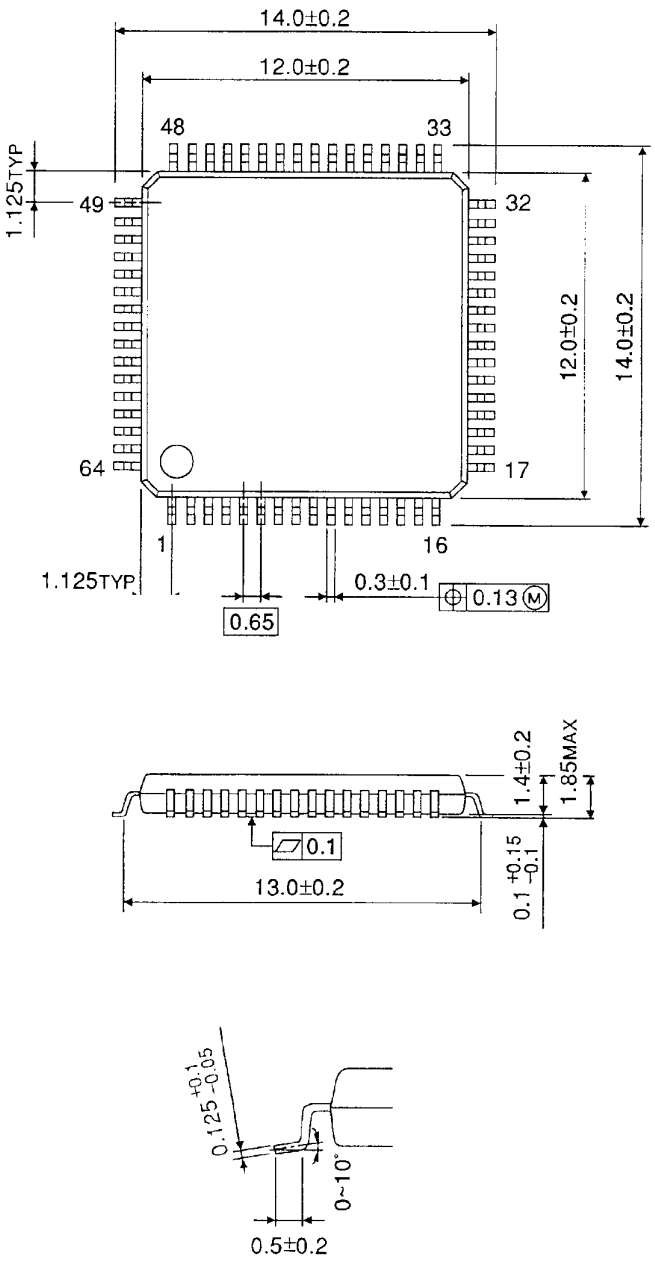
LQFP64-P-1010-0.50 Unit : mm



Weight: 0.32 g (typ.)

Package Dimensions

QFP64-P-1212-0.65 Unit : mm



Weight: 0.45 g (typ.)

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