



November 2014

FAN7080_GF085 Half Bridge Gate Driver



Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation fully operational to + 600V
- Tolerance to negative transient voltage on VS pin
- VS-pin dv/dt immune.
- Gate drive supply range from 5.5V to 20V
- Under-voltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- High side output in phase with input
- IN input is 3.3V/5V logic compatible and available on 15V input
- Matched propagation delay for both channels
- Dead time adjustable

Typical Applications

- Junction Box
- Half and full bridge application in the motor drive system

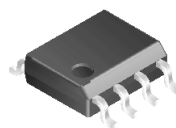


For Fairchild's definition of "green" Eco Status, please visit:
http://www.fairchildsemi.com/company/green/rohs_green.html

Description

The FAN7080_GF085 is a half-bridge gate drive IC with reset input and adjustable dead time control. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dV/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to $V_{S} = -5V$ (typical) at $V_{BS} = 15V$. Logic input is compatible with standard CMOS outputs. The UVLO circuits for both channels prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. Combined pin function for dead time adjustment and reset shutdown make this IC packaged with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 250mA and 500mA respectively, which is suitable for junction box application and half and full bridge application in the motor drive system.

SOIC-8

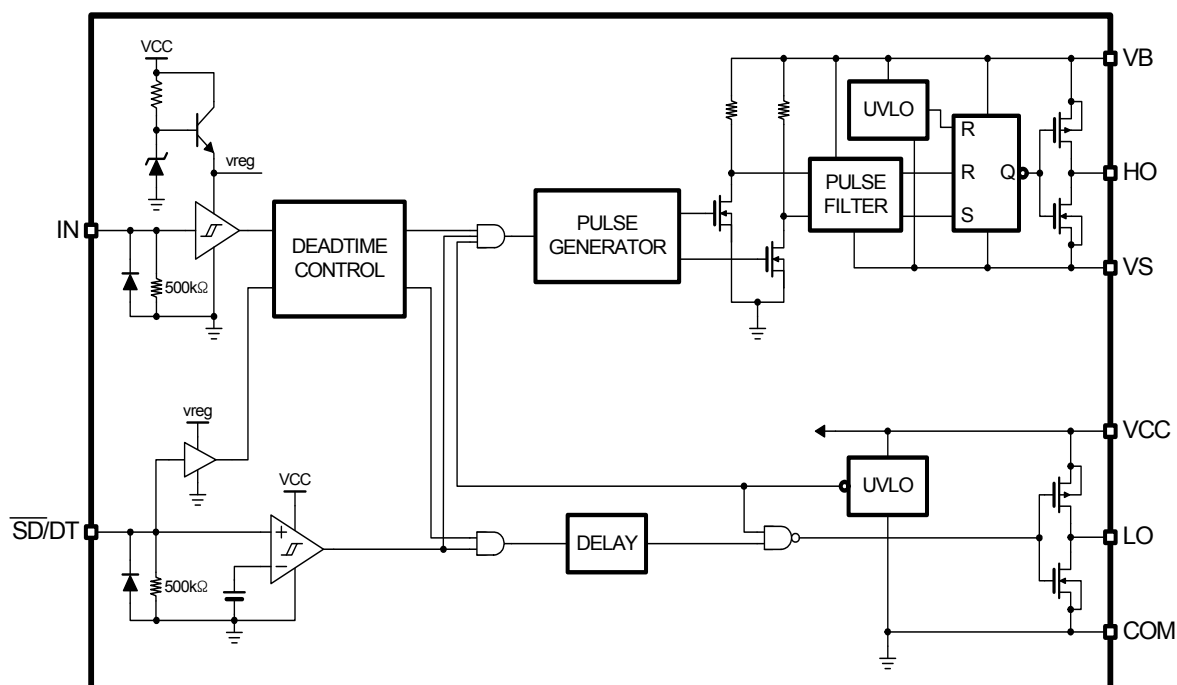


Ordering Information

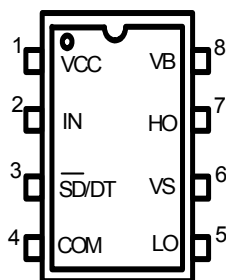
Device	Package	Operating Temp.
FAN7080M_GF085	SOIC-8	-40 °C ~ 125 °C
FAN7080MX_GF085	SOIC-8	-40 °C ~ 125 °C

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	VCC	P	Driver supply voltage
2	IN	I	Logic input for high and low side gate drive output
3	SD/DT	I	Shut down input and dead time setting
4	COM	P	Ground
5	LO	A	Low side gate drive output for MOSFET Gate connection
6	VS	A	High side floating offset for MOSFET Source connection
7	HO	A	High side drive output for MOSFET Gate connection
8	VB	P	Driver output stage supply

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Parameter	Symbol	Min.	Max.	Unit
High side floating supply offset voltage	VS	VB-25	VB+0.3	V
High side floating supply voltage	VB	-0.3	625	V
High side floating output voltage	VHO	VS-0.3	VB+0.3	V
Low side output voltage	VLO	-0.3	VCC + 0.3	V
Supply voltage	VCC	-0.3	25	V
Input voltage for $\overline{\text{IN}}$	VIN	-0.3	VCC+0.3	V
Input injection current. Full function, no latch up;(Guaranteed by design). Test at 10V and 17V on Eng.Samples	IIN	-	+1	mA
Power Dissipation	Pd		0.625	W
Thermal resistance, junction to ambient	Rthja		200	°C/W
Electrostatic discharge voltage (Human Body Model)	V _{ESD}	1K		V
Charge device model	V _{CDM}	500		V
Junction Temperature	T _J		150	°C
Storage Temperature	T _S	-55	150	°C

Note: 1) The thermal resistance and power dissipation rating are measured bellow conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural convection(StillAir)

JESD51-3 : Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Parameter	Symbol	Min.	Max.	Unit
High side floating supply voltage(DC) Transient:-10V@ 0.1 us	VB ¹⁾	VS + 6	VS + 20	V
High side floating supply offset voltage(DC) Transient: -25V(max) @0.1us @VBS<25V	VS	-5	600	V
High side floating output voltage	VHO	VS	VB	V
Low side output voltage	VLO	0	VCC	V
Allowable offset voltage Slew Rate ²⁾	dv/dt	-	50	V/ns
Supply voltage for logic part	VCC	5.5	20	V
Logic input voltage	VIN	0	VCC	V
Switching Frequency ³⁾	Fs		200	KHz
Minimum Pulse Width ^{2),4)}	T _{pulse}	1100	-	ns
Ambient Temperature	Ta	-40	125	°C

Note: 1) The Vs offset is tested with all supplies biased at 15V differential.

2) Guaranteed by design.

3) When VDT= 1.2V.

4) When VDT= 1.2V. Refer to Figure 1a, 1b, 1c and 1d on page 6.

Statics Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{BS} = 15\text{V}$, $V_S = 0\text{V}$, $C_L = 1\text{nF}$.

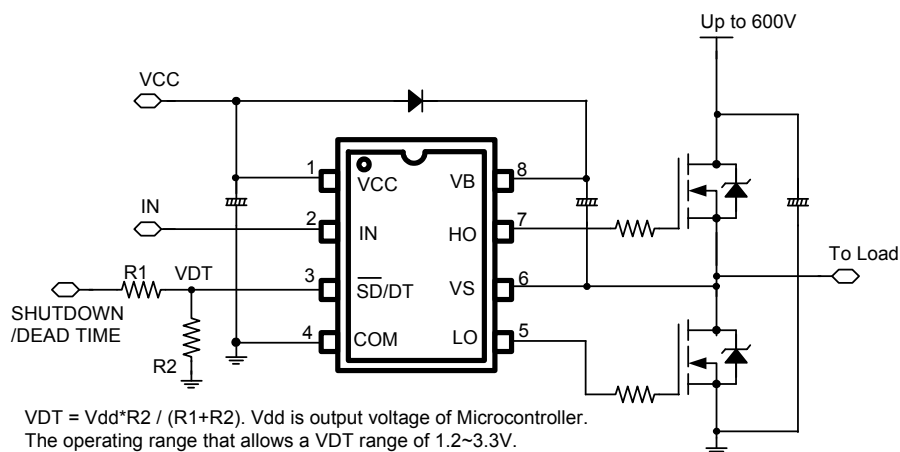
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Vcc and VBS supply Characteristics						
VCC and VBS supply under voltage positive going threshold	VCCUV+ VBSUV+	-	-	4.2	5.5	V
VCC and VBS supply under voltage negative going threshold	VCCUV- VBSUV-	-	2.8	3.6	-	V
VCC and VBS supply under voltage hysteresis	VCCUVH VBSUVH	-	0.2	0.6	-	V
Under voltage lockout response time	tduvcc tduvbs	VCC: 6V-->2.5V or 2.5V-->6V VBS: 6V-->2.5V or 2.5V-->6V	0.5 0.5	- -	20 20	us us
Offset supply leakage current	ILK	VB=VS=600V	-	20	50	uA
Quiescent VBS supply current	IQBS	VIN=0 OR 5V, VS=DT = 1.2V	20	75	150	uA
Quiescent Vcc supply current	IQCC	VIN=0 OR 5, VS=DT = 1.2V	-	350	1000	uA
Input Characteristics						
High logic level input voltage	VIH		2.7	-	-	V
Low logic level input voltage	VIL		-	-	0.8	V
High logic level input bias current for IN	IIN+	VIN=5V	-	10	50	uA
Low logic level input bias current for IN	IIN-	VIN=0V	-	0	2	uA
VSDT dead time setting range	VDT		1.2	-	5	V
VSDT shutdown threshold voltage	VSD		-	0.8	1.2	V
High logic level resistance for $\overline{\text{SD}}/\text{DT}$	RSMT	VSDT=5V	100	500	1100	K Ω
Low logic level input bias current for $\overline{\text{SD}}/\text{DT}$	ISDT-	VSDT=0V	-	1	2	uA
Output characteristics						
High level output voltage, VCC-VHO	VOH(HO)	IO=0	-	-	0.1	V
Low level output voltage, VHO	VOL(HO)	IO=0	-	-	0.1	V
Output high short circuit pulse current	IO+(HO)		250	300	-	mA
Output low short circuit pulse current	IO-(HO)		500	600	-	mA
Equivalent output resistance	ROP(HO)		-	-	60	Ω
	RON(HO)		-	-	30	Ω
High level output voltage, VB-VLO	VOH(LO)	IO=0	-	-	0.1	V
Low level output voltage, VLO	VOL(LO)	IO=0	-	-	0.1	V
Output high short circuit pulse current	IO+(LO)		250	-	-	mA
Output low short circuit pulse current	IO-(LO)		500	-	-	mA
Equivalent output resistance	ROP(LO)		-	-	60	Ω
	RON(LO)		-	-	30	Ω

Dynamic Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{BS} = 15\text{V}$, $V_S = 0\text{V}$, $C_L = 1\text{nF}$.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Turn-on propagation delay	t_{on}	$V_S = 0\text{V}$	-	750	1500	ns
Turn-off propagation delay	t_{off}	$V_S = 0\text{V}$	-	130	250	ns
Turn -on rising time	t_r	-	-	40	150	ns
Turn -off falling time	t_f	-	-	25	400	ns
Dead time, LS turn-off to HS turn-on and HS turn-on to LS turn-off	DT	$V_{IN} = 0$ or 5V @ $V_{DT} = 1.2\text{V}$ $V_{IN} = 0$ or 5V @ $V_{DT} = 3.3\text{V}$	250 1600	650 2100	1200 2600	ns
Dead time matching time	MDT	$DT1 - DT2$ @ $V_{DT} = 1.2\text{V}$ $DT1 - DT2$ @ $V_{DT} = 3.3\text{V}$	-	35 -	110 300	ns
Delay Matching, HS and LS turn-on	MTON	$V_{DT} = 1.2\text{V}$	-	25	110	ns
Delay Matching, HS and LS turn-off	MTOFF	$V_{DT} = 1.2\text{V}$	-	15	60	ns
Shutdown propagation delay	T_{sd}		-	180	330	ns
Switching Frequency	F_{s1}	$V_{CC} = V_{BS} = 20\text{V}$	-	-	200	KHz
	F_{s2}	$V_{CC} = V_{BS} = 5.5\text{V}$	-	-	200	KHz

Typical Application Circuit



Typical Waveforms

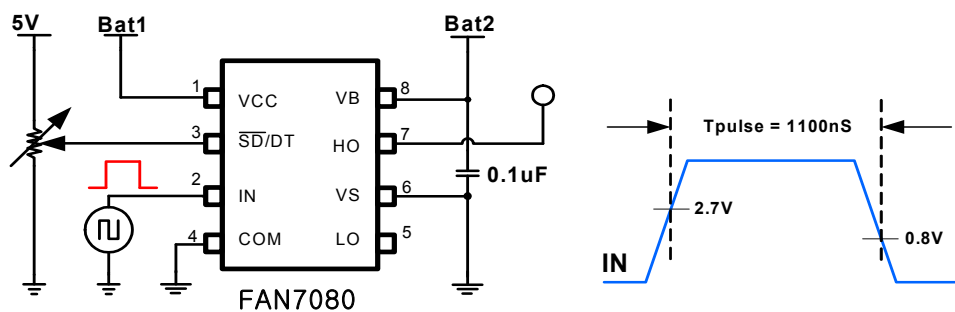


Figure 1a. Short Pulse Width Test Circuit and Pulse Width Waveform

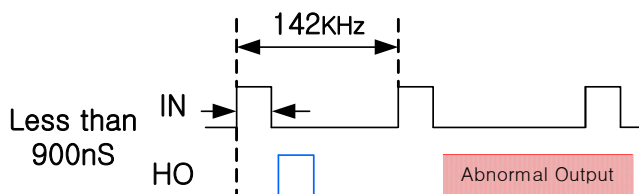


Figure 1b. Abnormal Output Waveform with pulse width

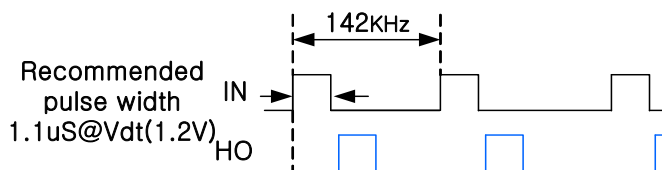


Figure 1c. Recommendation of pulse width Output Waveform

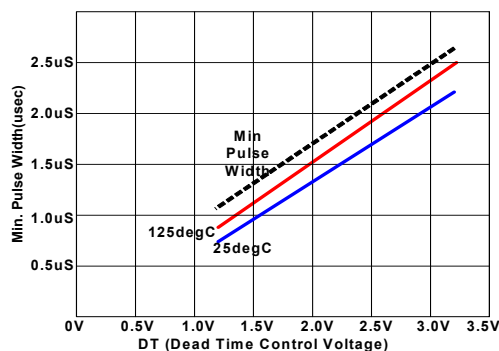


Figure 1d. Pulse Width VS Vdt

Typical Waveforms

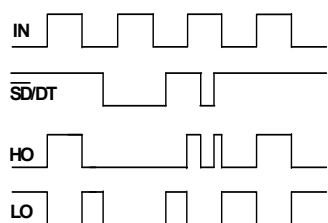


Figure 2. Input/output Timing Diagram

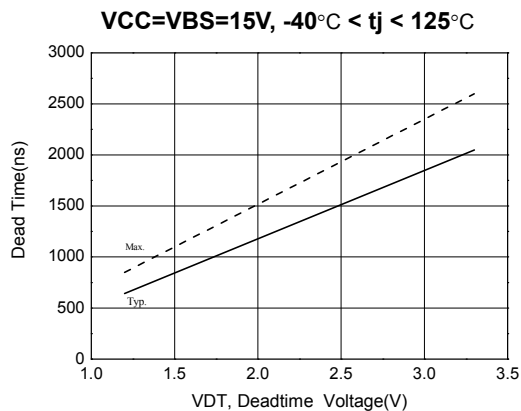


Figure 3. Dead Time VS VDT

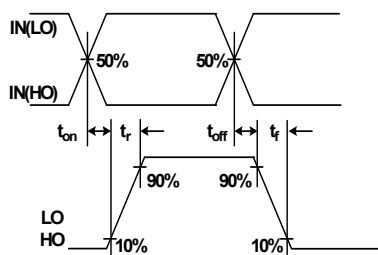


Figure 4a. Switching Time Waveform Definitions

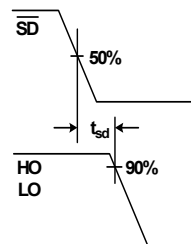


Figure 4b. Shutdown Waveform Definitions

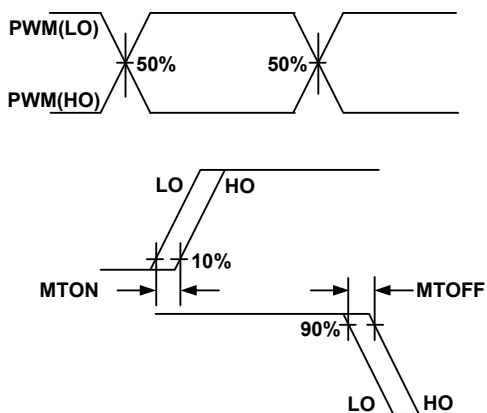


Figure 5. Delay Matching Waveform Definitions

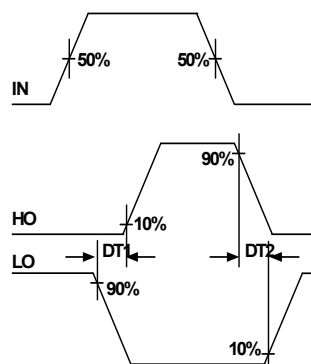


Figure 6. Dead Time Waveform Definitions

Performance Graphs

(This performance graphs based on ambient temperature $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$)

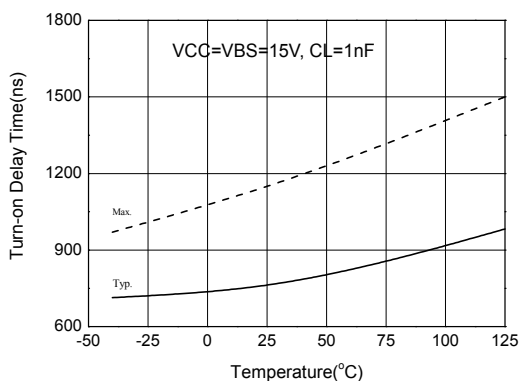


Figure 7a. Turn-On Delay Time of HO vs VBS Temperature

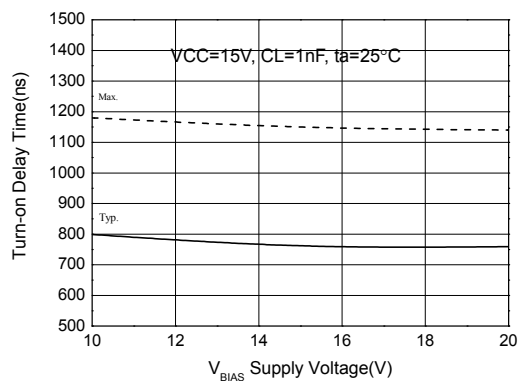


Figure 7b. Turn-On Delay Time of HO vs VBS Supply Voltage

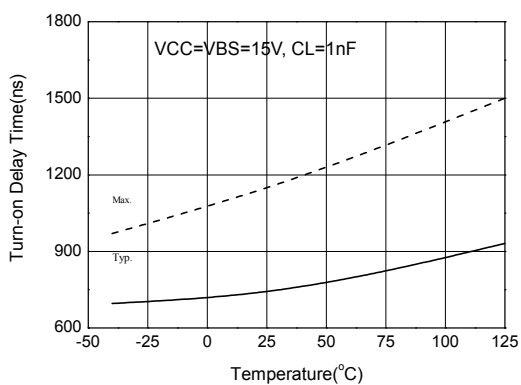


Figure 8a. Turn-On Delay Time of LO vs Temperature

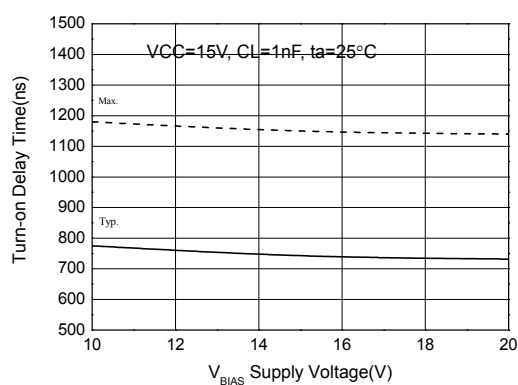


Figure 8b. Turn-On Delay Time vs of LO VBS Supply Voltage

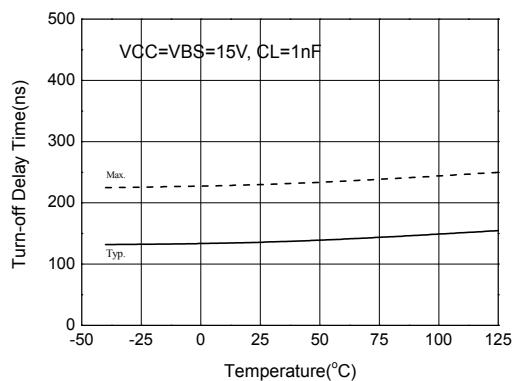


Figure 9a. Turn-Off Delay Time of HO vs Temperature

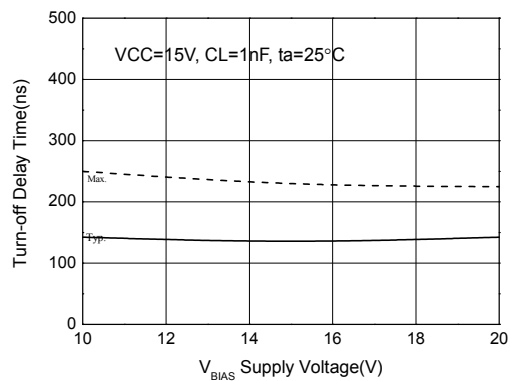


Figure 9b. Turn-Off Delay Time of HO vs VBS Supply Voltage

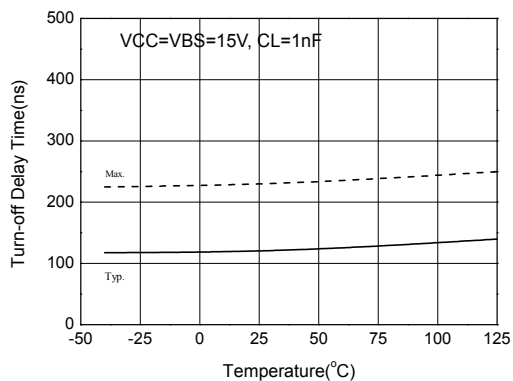


Figure 10a. Turn-Off Delay Time of LO vs Temperature

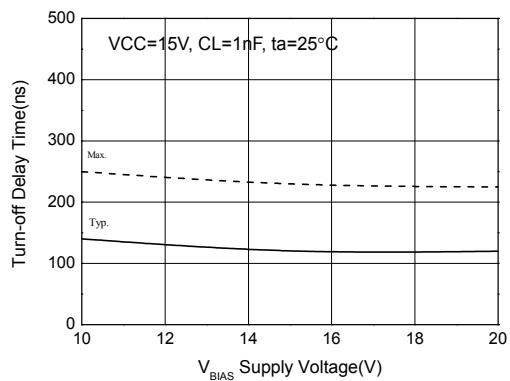


Figure 10b. Turn-Off Delay Time of LO vs VBS Supply Voltage

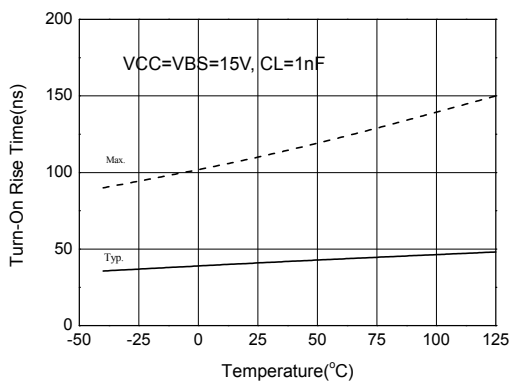


Figure 11a. Turn-On Rise Time of HO vs Temperature

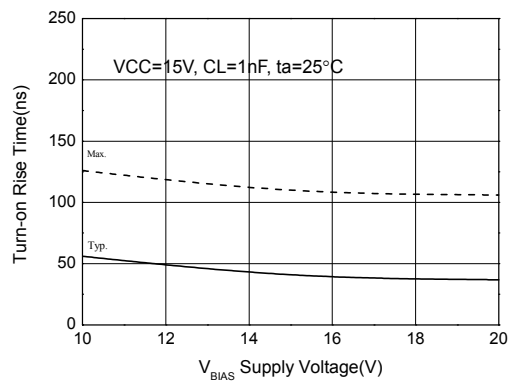


Figure 11b. Turn-On Rise Time vs of HO VBS Supply Voltage

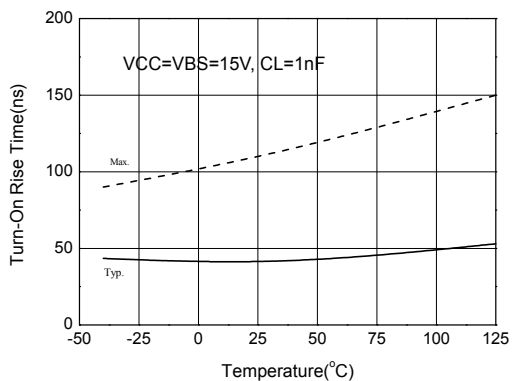


Figure 12a. Turn-On Rise Time of LO vs Temperature

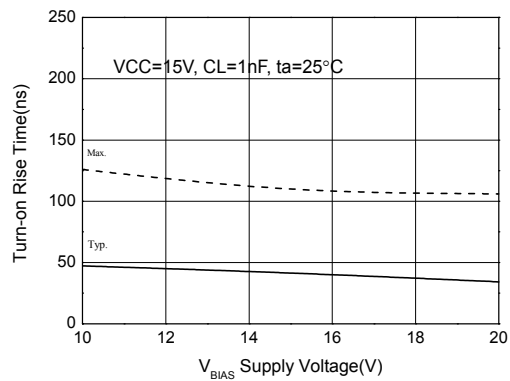


Figure 12b. Turn-On Rise Time of LO vs VBS Supply Voltage

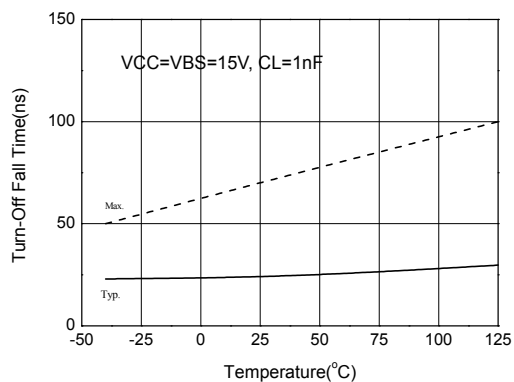


Figure 13a. Turn-Off Fall Time of HO vs Temperature

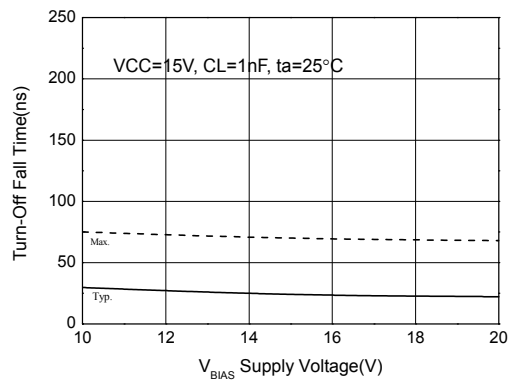


Figure 13b. Turn-Off Fall Time of HO vs VBS Supply Voltage

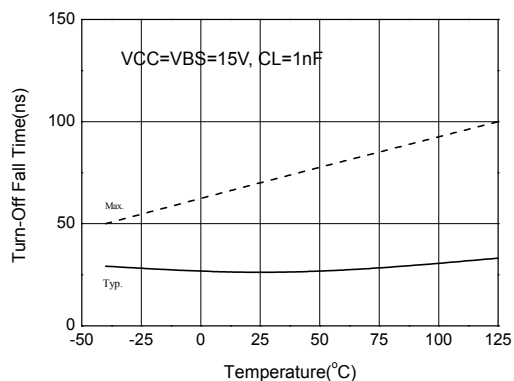


Figure 14a. Turn-Off Fall Time of LO vs Temperature

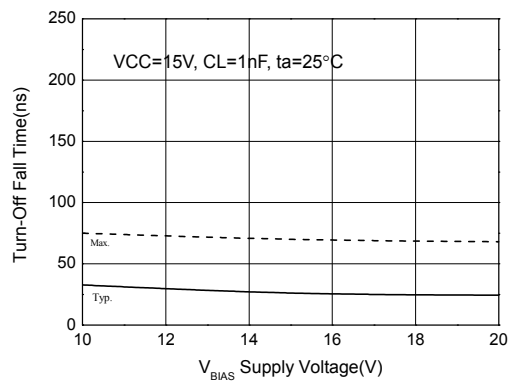


Figure 14b. Turn-Off Fall Time of LO vs BS Supply Voltage

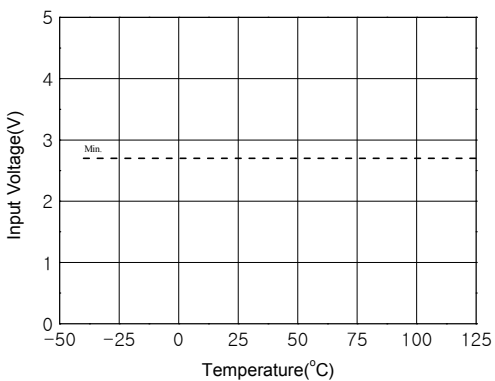


Figure 15a. Logic 0 Input Voltage vs Temperature

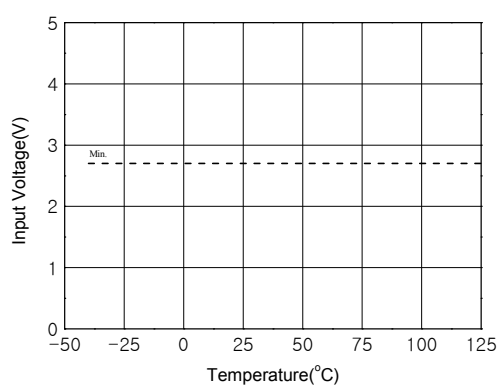


Figure 15b. Logic 1 Input Voltage vs Temperature

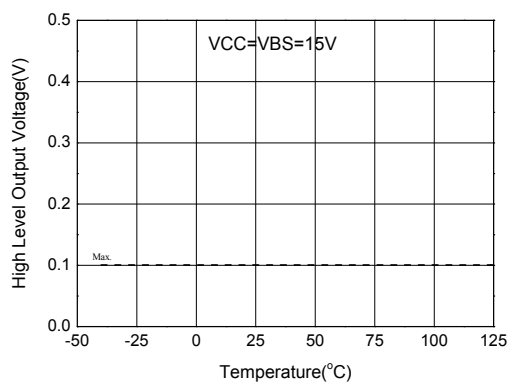


Figure 16a. High Level Output of HO vs Temperature

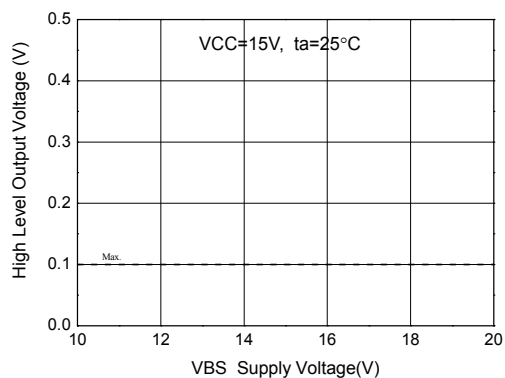


Figure 16b. High Level Output of HO vs VBS Supply Voltage

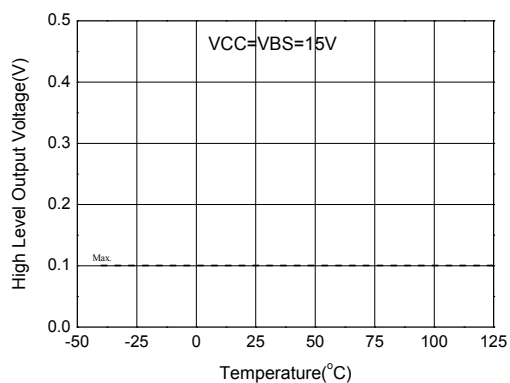


Figure 17a. High Level Output of LO vs Temperature

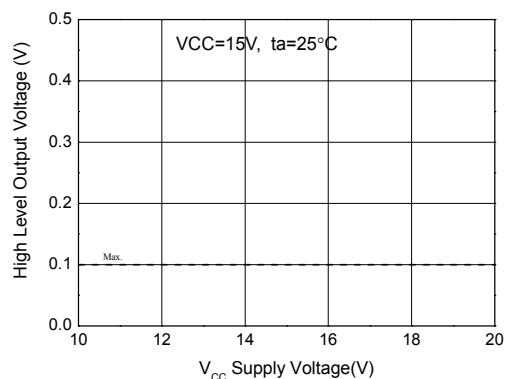


Figure 17b. High Level Output of LO vs VCC Supply Voltage

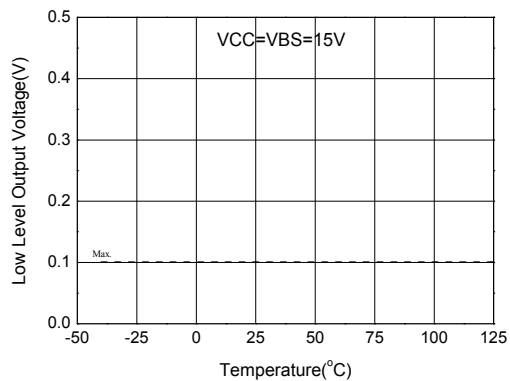


Figure 18a. Low Level Output of HO vs Temperature

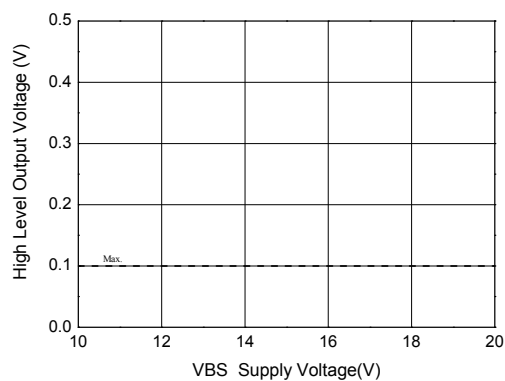


Figure 18b. Low Level Output of HO vs VBS Supply Voltage

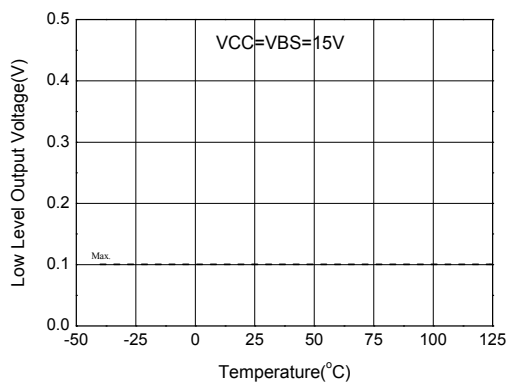


Figure 19a. Low Level Output of LO vs Temperature

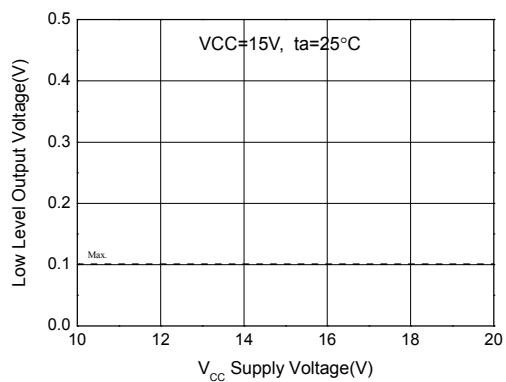


Figure 19b. Low Level Output of LO vs VCC Supply Voltage

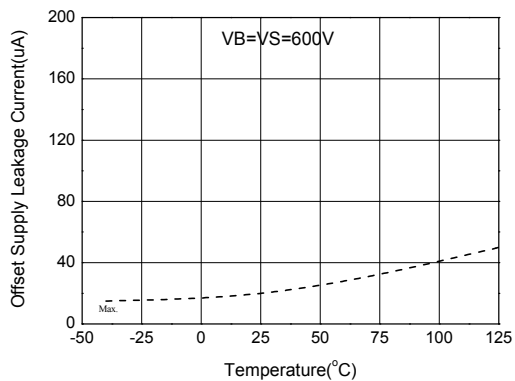


Figure 20a. Offset Supply leakage Current vs Temperature

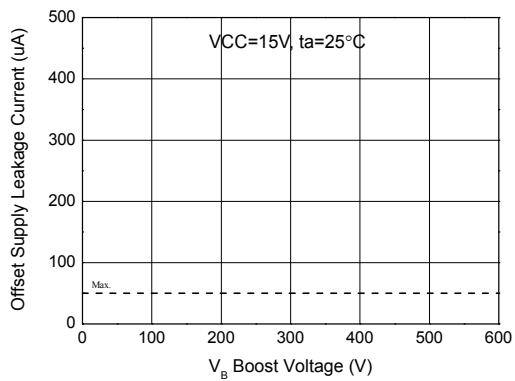


Figure 20b. Offset Supply leakage Current vs VB Boost Voltage

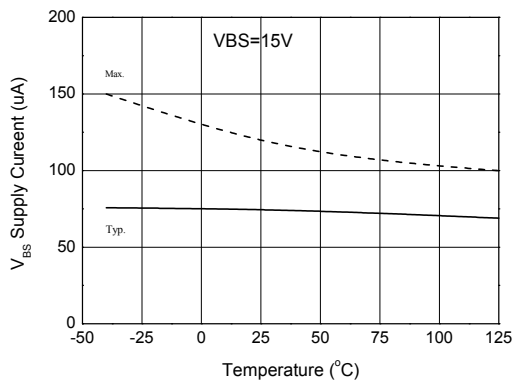


Figure 21. VBS Supply Current vs Temperature

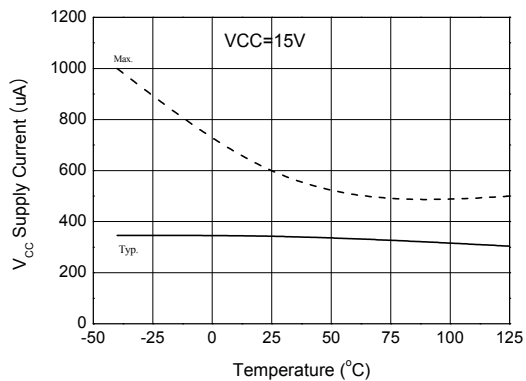


Figure 22. VCC Supply Current vs Temperature

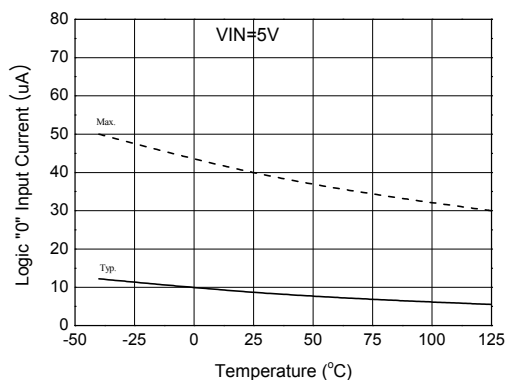


Figure 23a. Logic 1 Input Current vs Temperature

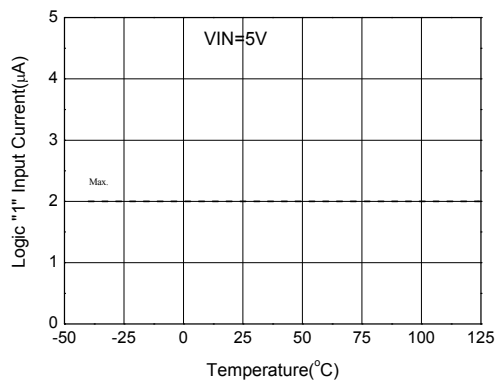


Figure 23b. Logic 0 Input Current vs Temperature

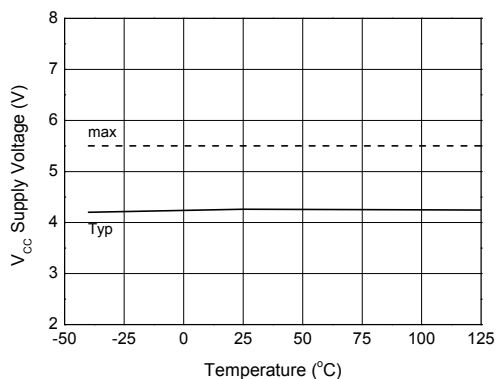


Figure 24a. VCC UnderVoltage Threshold (+) vs Temperature

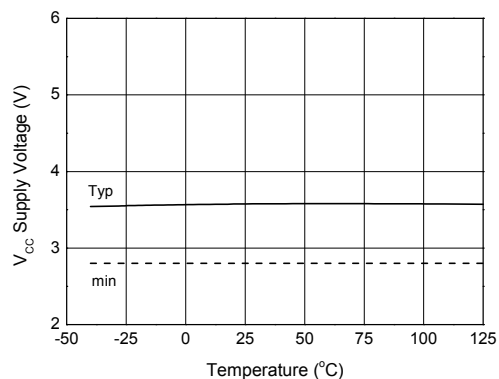


Figure 24b. VCC UnderVoltage Threshold(-) vs Temperature

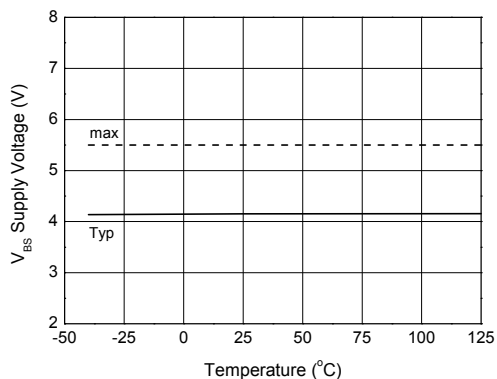


Figure 25a. VBS UnderVoltage Threshold (+) vs Temperature

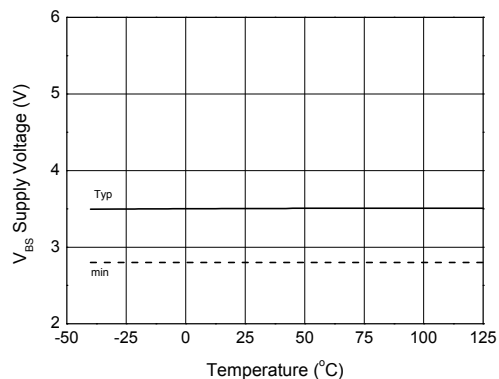


Figure 25b. VBS UnderVoltage Threshold(-) vs Temperature

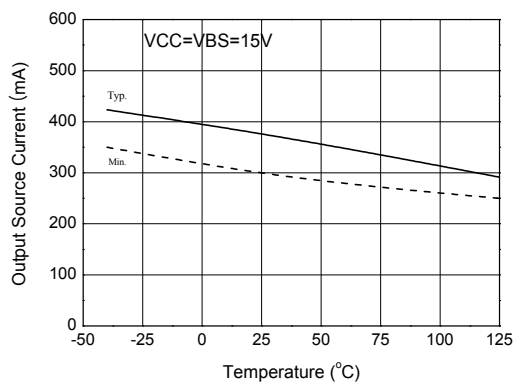


Figure 26a. Output Source Current of HO vs Temperature

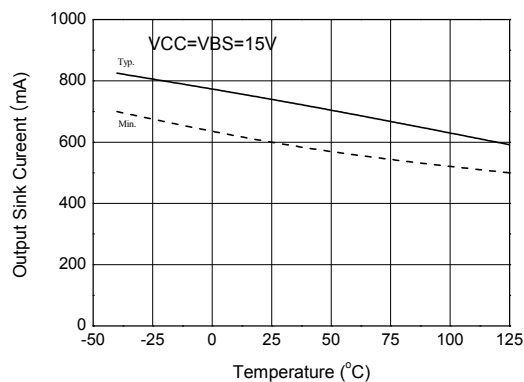


Figure 26b. Output Sink Current of HO vs Temperature

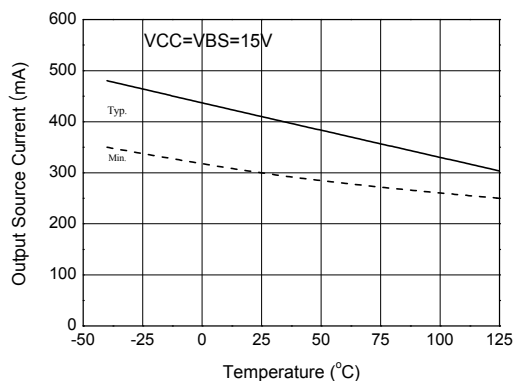


Figure 27a. Output Source Current of LO vs Temperature

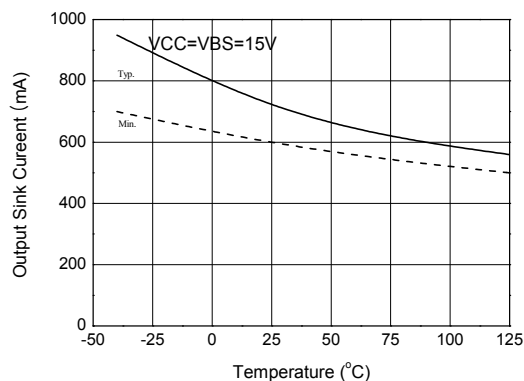


Figure 27b. Output Sink Current of LO vs Temperature

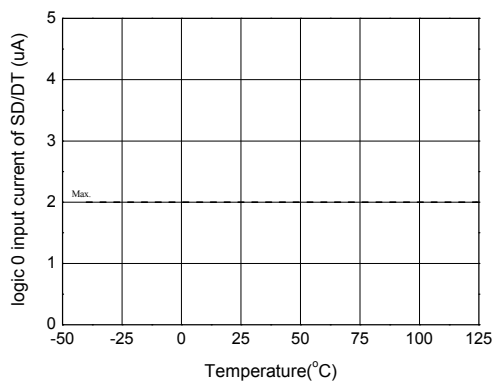


Figure 28. Logic 0 Input Current of SD/DT vs Temperature

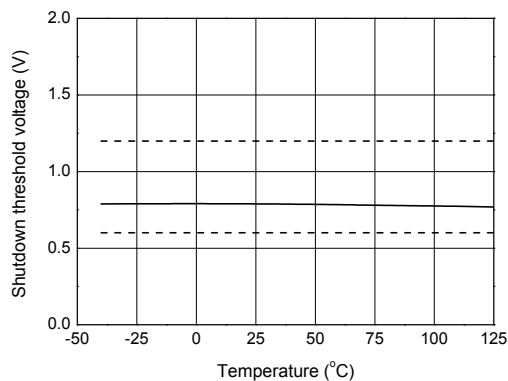


Figure 29. Shutdown Threshold of vs Temperature

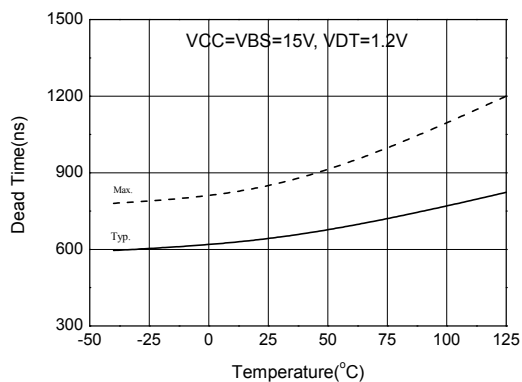


Figure 30. Deadtime vs Temperature

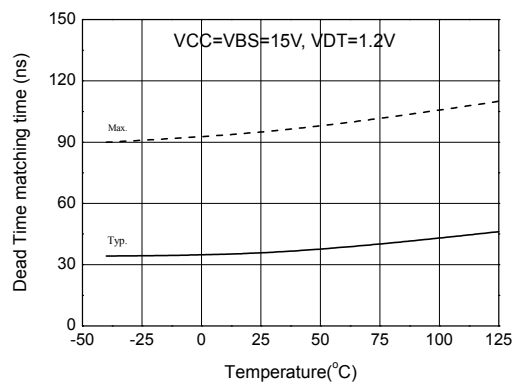


Figure 31. Deadtime Matching Time vs Temperature

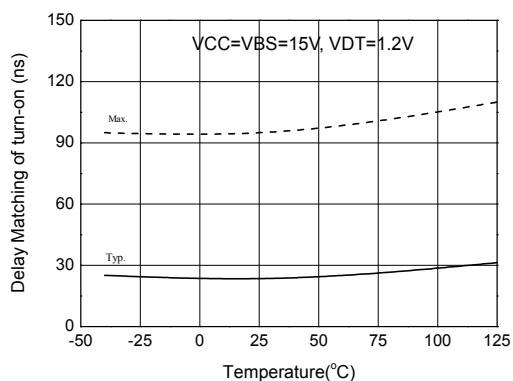


Figure 32. Turn-On Delay Matching vs Temperature

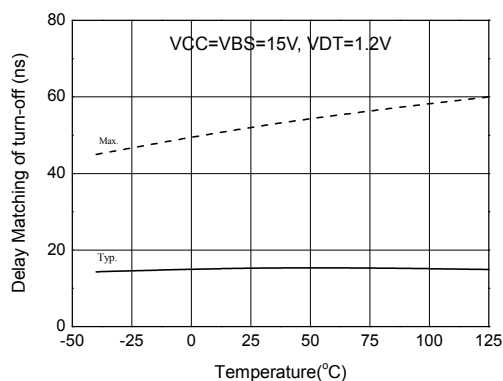


Figure 33. Turn_Off Delay Matching vs Temperature

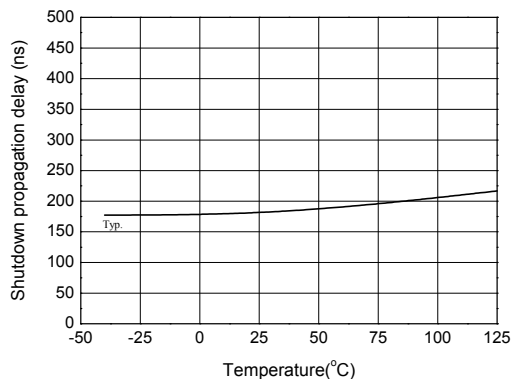


Figure 34. Shutdown Propagation Delay vs Temperature

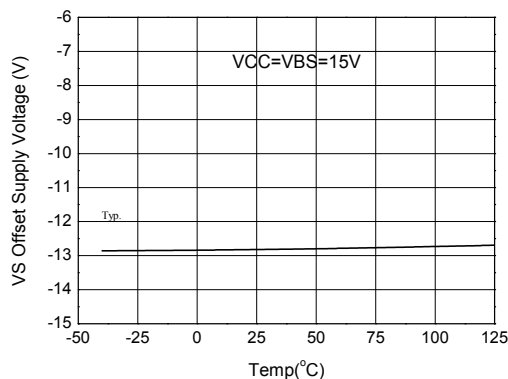
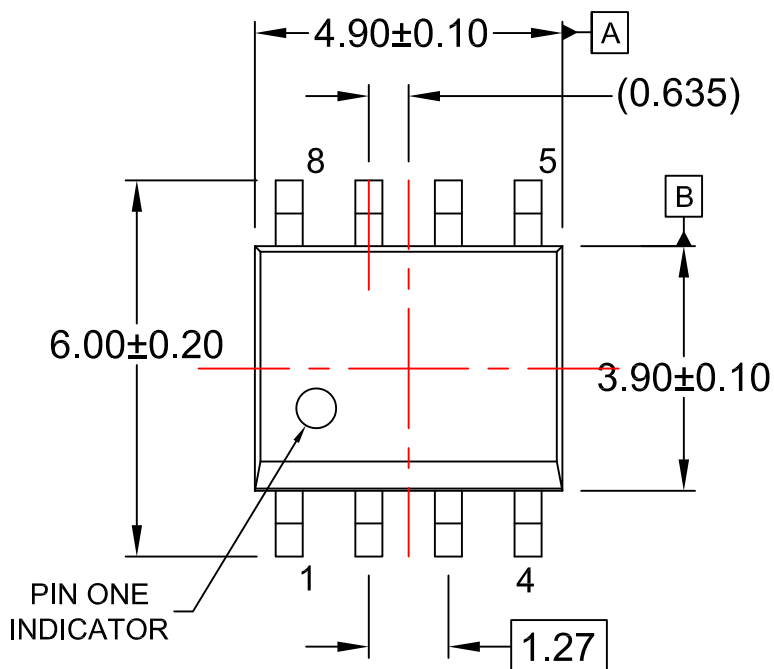
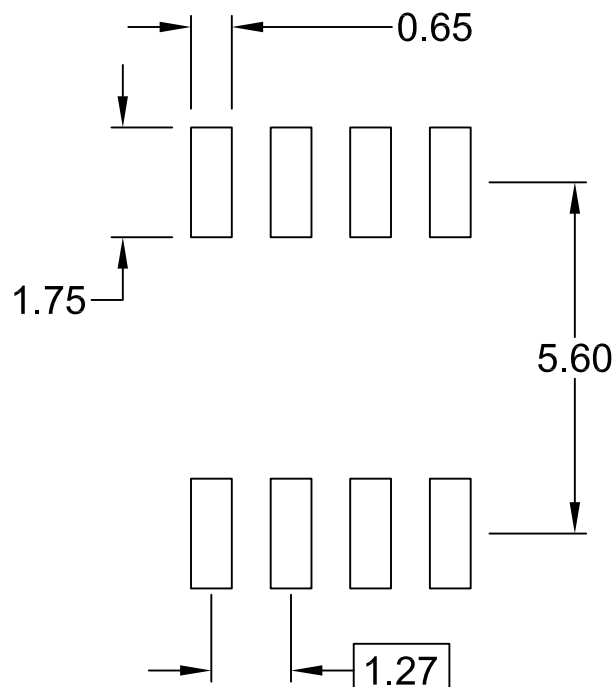


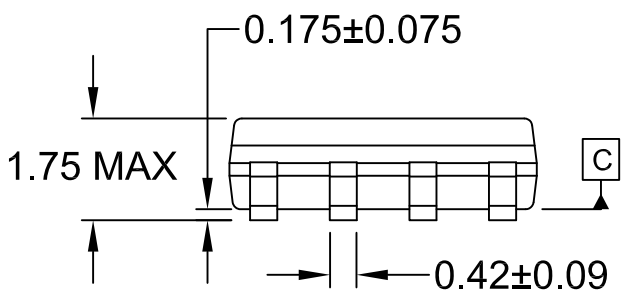
Figure 35. Maximum VS Negative Offset of vs Temperature



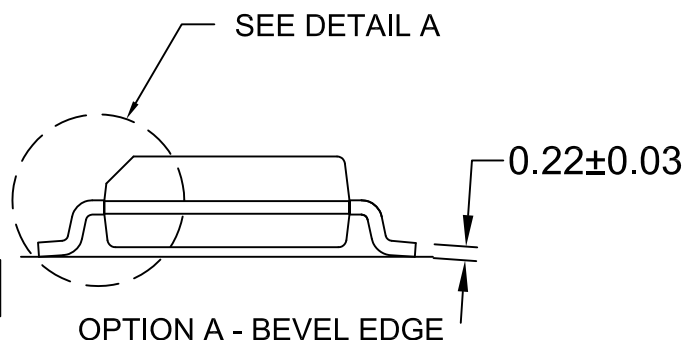
$\oplus$ 0.25 (M) C B A



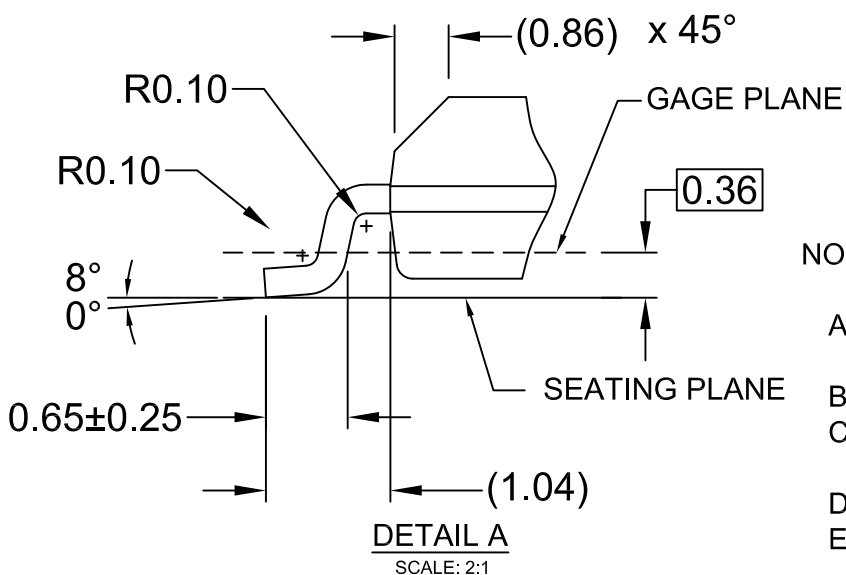
LAND PATTERN RECOMMENDATION



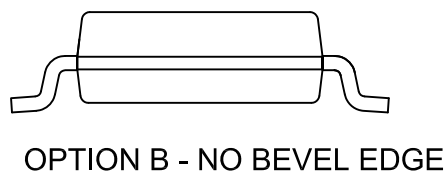
$\frac{1}{2}$ 0.10



OPTION A - BEVEL EDGE



DETAIL A
SCALE: 2:1



OPTION B - NO BEVEL EDGE

NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16



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CTL™	IntelliMAX™	Saving our world, 1mW/W/kW at a time™	TinyWire™
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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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