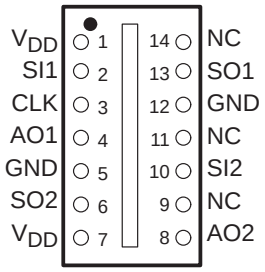
- **Contains Two 64-Bit Static Shift Registers**
- **Offers Extendable Data I/O for Expanding the Number of Sensors**
- **Contains Analog Buffer With Sample-and-Hold for Analog Output Over Full Clock Period**
- **Single-Supply Operation**
- **Operates With 500-kHz Shift Clock**
- **14-Pin Encapsulated Clear Plastic Package**
- **Advanced LinCMOS™ Technology**

(TOP VIEW)



NC – No internal connection

description

The TSL215 integrated opto sensor consists of two sections of 64 charge-mode pixels arranged in a 128 × 1 linear array. Each pixel measures 120 µm × 70 µm with 125-µm center-to-center spacing. Operation is simplified by internal logic requiring only clock and start-integration-pulse signals.

The TSL215 is intended for use in a wide variety of applications including linear and rotary encoding, bar-code reading, edge detection and positioning, and contact imaging.

The TSL215 is supplied in a 14-pin dual-in-line clear plastic package.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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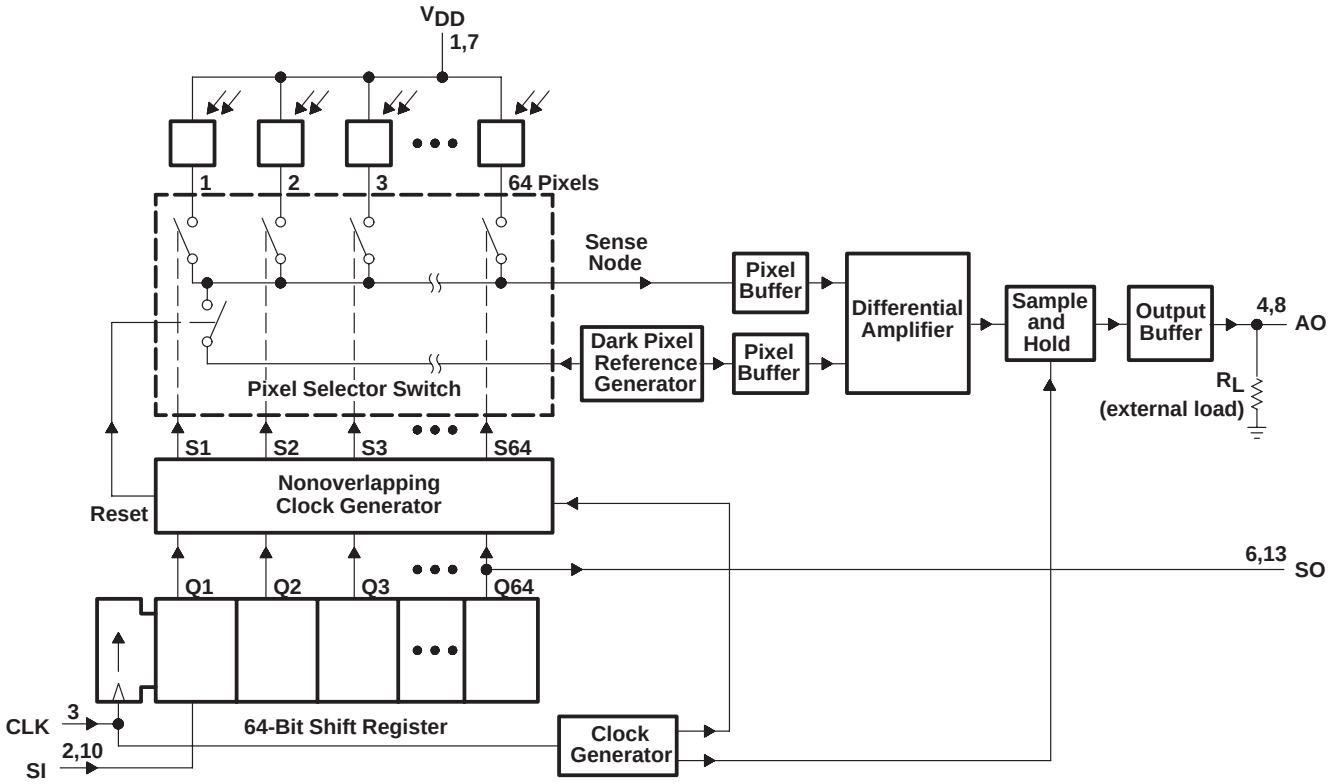
functional block diagram of each section



Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
AO1	4	Analog output of section 1
AO2	8	Analog output of section 2
CLK	3	Clock. The clock controls charge transfer, pixel output, and reset.
GND	5, 12	Ground (substrate). All voltages are referenced to the substrate.
NC	9, 11, 14	No internal connection
SI1	2	Serial input (section 1). The serial input defines the end of the integration period and initiates the pixel output sequence.
SI2	10	Serial input (section 2). The serial input defines the end of the integration period and initiates the pixel output sequence.
SO1	13	Serial output (section 1). The serial output provides a signal to drive the SI2 input.
SO2	6	Serial output (section 2). The serial output provides a signal to drive the SI1 input of another TSL215 sensor for cascading.
V_{DD}	1, 7	Supply voltage. These supply power to the analog and digital circuits.

detailed description

sensor elements

The line of sensor elements, called pixels, consists of 128 discrete photosensing areas. Light energy striking a pixel generates electron-hole pairs in the region under the pixel. The field generated by the bias on the pixel causes the electrons to collect in the element while the holes are swept into the substrate. The amount of charge accumulated in each element is directly proportional to the amount of incident light and the integration time.

device operation

Operation of the 128 × 1 array sensor is a function of two time periods: an integration period during which a charge is accumulated in the pixels and an output period during which signals are transferred to the output. The integration period is defined by the interval between the externally supplied (SI) pulses and includes the output period (see Figure 1). The required length of the integration period depends on the amount of incident light and the desired output signal level. A single TSL215 can be connected in either a serial or parallel configuration.

serial configuration

The serial connection shown in Figure 1 is accomplished by connecting the analog outputs (AO1 and AO2) together and connecting the SO1 output to the SI2 input. As shown in Figure 1, the external SI signal is supplied to only the SI1 input. This causes the first section of 64 pixels to be clocked out in synchronization with CLK. In conjunction with the 64th pixel, the SI pulse is shifted out on the SO1 output. This SO1 pulse is then fed to the SI2 input. The 65th clock cycle terminates the output of the last pixel from the first section and clears the shift register of that section in preparation for the next SI pulse to that section. The rising edge of the 65th cycle also puts AO1 into the high-impedance state. The appearance of the SI2 signal and the 65th clock cycle initiates the output cycle of the second section. The second section of 64 pixels appears at AO2, and the SO2 signal is shifted out on the 128th clock cycle. The rising edge of the 129th clock cycle resets the second section and puts AO2 into the high-impedance state. Both AO1 and AO2 remain in this high-impedance state until a new external SI pulse appears on SI1. When the TSL215 is connected as shown in Figure 1, the analog output appears as a continuous string representing the 128 pixels.

parallel configuration

Parallel operation of the TSL215 (see Figure 2) is accomplished by connecting the serial input lines (SI1 and SI2) together and connecting each AO line (AO1 and AO2) to its own load resistor (R_L). This supplies the external serial input pulse to both SI1 and SI2 simultaneously. Each AO line must be independent of the other line since both sections are active simultaneously. Pixels 1 through 64 appear on AO1, while pixels 65 through 128 appear on AO2. These two sections of 64 pixels begin clocking out concurrently, each on its respective output. On the 64th clock cycle, both SO1 and SO2 are shifted out of each respective register. The rising edge of the 65th cycle terminates the output of the 64th pixel from each section and also resets both section's shift registers. Both AO lines then go to the high-impedance state until the next external SI signal appears.

sense node

On completion of the integration period, the charge contained in each pixel is transferred in turn to the sense node under the control of the clock (CLK) and serial-input (SI) signals. The signal voltage generated at this node is directly proportional to the amount of charge and inversely proportional to the capacitance of the sense node.

reset

An internal reset signal is generated by the nonoverlapping clock generator (NOCG) and occurs every clock cycle. Reset establishes a known voltage on the sense node in preparation for the next charge transfer. This voltage is used as a reference level for the differential signal amplifier.

detailed description (continued)

shift register

Both 64-bit shift registers control the transfer of charge from the pixels to the output stages and provide timing signals for the NOCG. The serial input (SI) signal provides the input to the shift register and is shifted under direct control of CLK out to the serial output (SO) on the 64th clock cycle. This SO pulse can then be used as the SI pulse for the next section or next device.

The output period for each section is initiated by the presence of the SI input pulse coincident with a rising edge of CLK (see Figures 1, 2, and 3). The analog output voltage corresponds to the level of the first pixel after settling time (t_s) and remains constant for a minimum time (t_v). A voltage corresponding to each succeeding pixel is available at each rising edge of CLK. The output period of a section ends when the active section sees the rising edge of the 65th clock cycle, at which time the output assumes the high-impedance state. Once the output period has been initiated by an SI pulse, CLK must be allowed to complete [(n × 64)+1] (where n is the number of sections running in series) positive-going transitions in order to reset the internal logic to a known state. To achieve minimum integration time, the SI pulse may be present on the [(n × 64)+2] rising clock to immediately restart the output phase.

sample-and-hold

The sample-and-hold signal generated by the NOCG is used to hold the analog output voltage of each pixel constant until the next pixel is clocked out. The signal is sampled while CLK is high and held constant while CLK is low.

nonoverlapping clock generators

The NOCG circuitry provides internal control signals for the sensor, including reset and pixel-charge sensing. The signals are synchronous and are controlled by the outputs of the shift register.

initialization

Initialization of the sensor elements may be necessary on power up or during operation after any period of CLK or SI inactivity exceeding the integration time. The initialization phase consists of 12 to 15 consecutively performed output cycles and clears the pixels of any charge that may have accumulated during the inactive period.

multiple-unit operation

Multiple-sensor devices can be connected together in a serial or parallel configuration. The serial connection is accomplished by connecting analog outputs (AO) together and connecting the SO output of each sensor device to the SI input of the next device. The SI signal is applied to only the first device. Each succeeding device receives its SI input from the SO output of the preceding device. For m-cascaded devices, the SI pulse is applied to the first device after every m•128th positive-going CLK transitions. A common clock signal is applied to all the devices simultaneously. Parallel operation of multiple devices is accomplished by supplying CLK and SI signals to all the devices simultaneously. The output of each device is then separately used for processing.

output enable

The internally generated output-enable signal enables the output stage of each section during the output period (64 clock cycles). During the remainder of the integration period, the output stage is in the high-impedance state that allows output interconnections of multiple devices without interference.

absolute maximum ratings, T_A = 25°C (unless otherwise noted) (see Note 1)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.5 V to 7 V
Digital output voltage range, V_O . . . . . –0.5 V to V_{DD} + 0.5 V
Digital output current, I_O . . . . . 3 mA
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating case temperature range, T_C (see Note 2) . . . . . –10°C to 85°C
Storage temperature range . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the network GND.
2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5		5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Analog output external resistive load, R_L		330		Ω
Wavelength of light source, λ		750		nm
Clock input frequency, f_{clock}	10		500	kHz
Pulse duration, CLK low, $t_{w(CLKL)}$	1			µs
Sensor integration time, t_{int} (see Figures 1 and 2)		5		ms
Setup time, SI before CLK↑, $t_{su(SI)}$	50			ns
Hold time, SI after CLK↑, $t_{h(SI)}$	50			ns
Total number of TSL215 outputs connected together			8	
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{DD} = 5 V, T_A = 25°C, f_{clock} = 180 kHz, λ_p = 565 nm, R_L = 330 Ω, C_L = 330 pF, t_{int} = 5 ms, E_e = 20 μW/cm² (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Low-level output voltage	I_O = 0			0.1	V
High-level output voltage		4.4			V
Analog output voltage, saturation level	E_e = 60 μW/cm²	3	3.4		V
Analog output voltage (white, average over 64 pixels)		1.75	2.2		V
Analog output voltage (dark, each pixel)	E_e = 0		0.25	0.4	V
Output voltage (white) change with change in V_{DD}	V_{DD} = 5 V ±5%, See Note 4		±2%		
Dispersion of analog output voltage	See Note 5			±10%	
Linearity of analog output voltage	t_{int} = 2 ms to 5 ms, See Note 6	0.85		1.15	
Pixel recovery time	See Note 7		25	40	ms
Supply current	I_{DD} (average), See Note 4		4	12	mA
High-level input current	$V_I = V_{DD}$			0.5	μA
Low-level input current	V_I = 0			0.5	μA
Input capacitance			5		pF

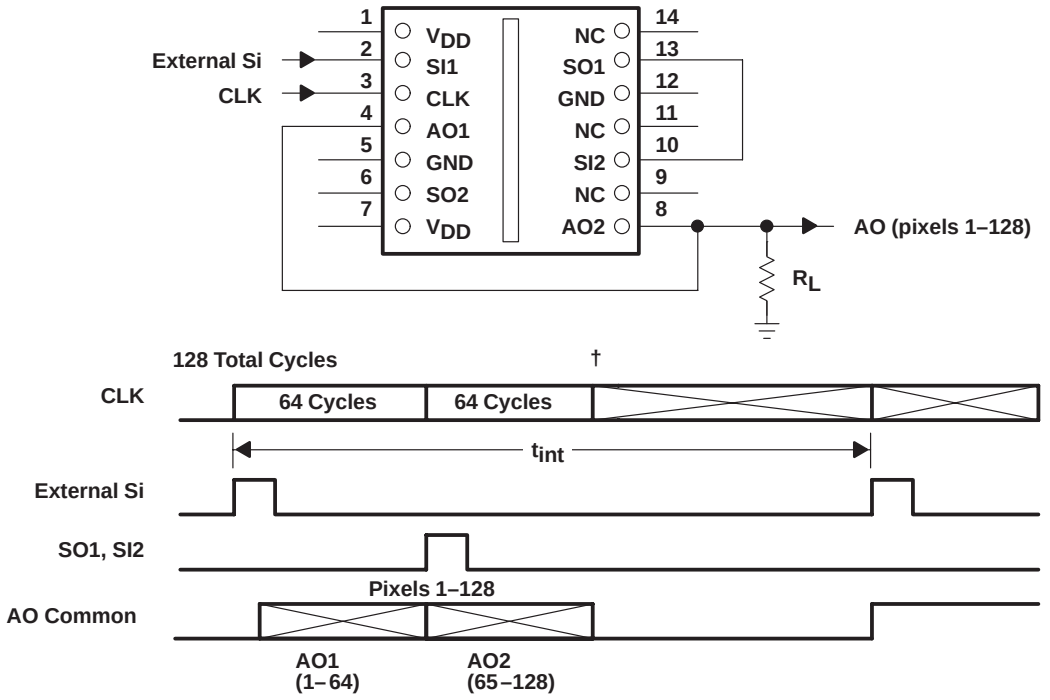
† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 3. The input irradiance (E_e) is supplied by an LED array with λ_p = 565 nm.
4. Device tested in parallel mode with only one section active
5. Dispersion of analog output voltage is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test.
6. Linearity of analog output voltage is calculated by averaging over 64 pixels and measuring the maximum deviation of the voltage at 2 ms and 3.5 ms from a line drawn between the voltage at 2.5 ms and 5 ms.
7. Pixel recovery time is the time required for a pixel to go from the analog-output-voltage (white, average over 64 pixels) level to analog-output-voltage (dark, each pixel) level or vice versa after a step change in light input.

operating characteristics, R_L = 330 Ω, C_L = 330 pF, V_{DD} = 5 V, T_A = 25°C, t_{int} = 5 ms, E_e = 20 μW/cm², f_{clock} = 500 kHz (unless otherwise noted)

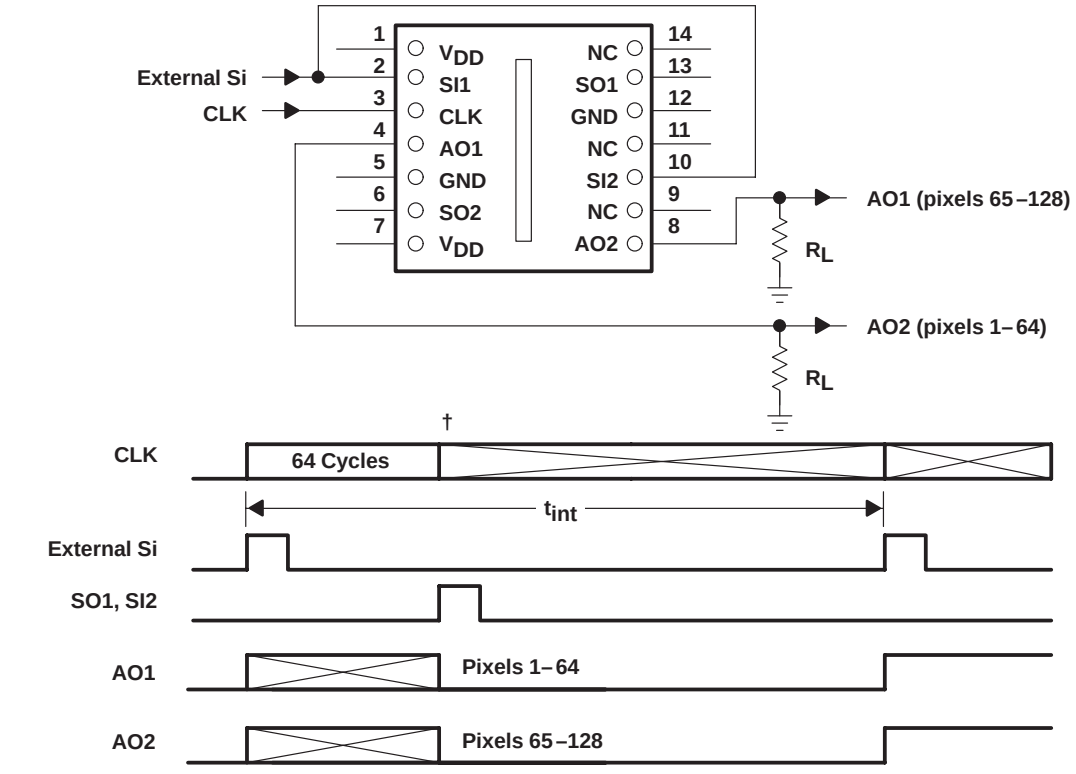
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(SO)}$	Rise time, SO	See Figure 3 and Note 8		25		ns
$t_{f(SO)}$	Fall time, SO			25		ns
$t_{pd(SO)}$	Propagation delay time, SO			70		ns
t_s	Settling time				1	μs
t_v	Valid time				1/2 f_{clock}	μs

NOTE 8: Clock duty cycle is assumed to be 50%.



† CLK continues or goes low after 129 cycles.

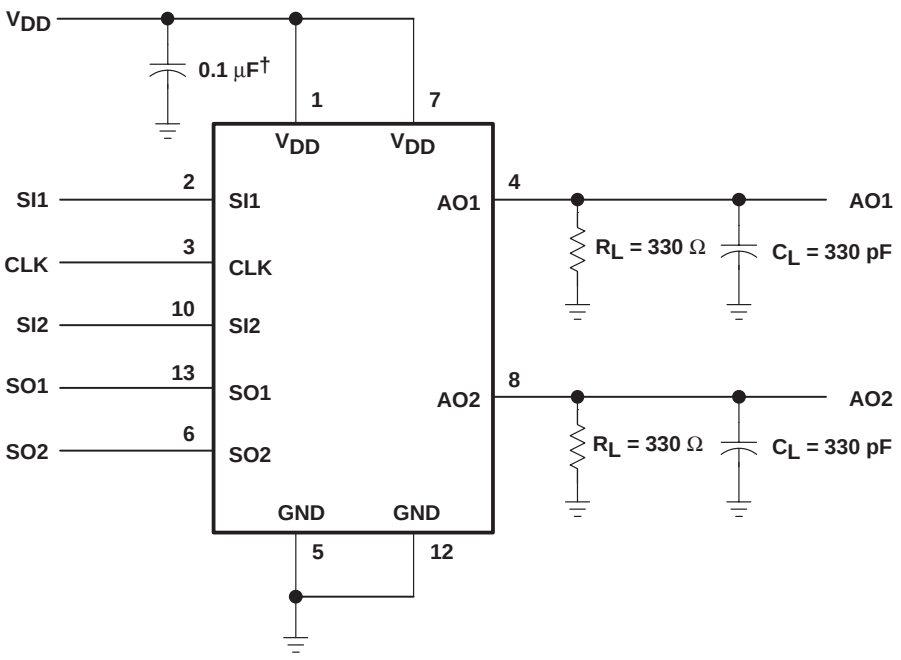
Figure 1. Serial Configuration



† CLK continues or goes low after 65 cycles.

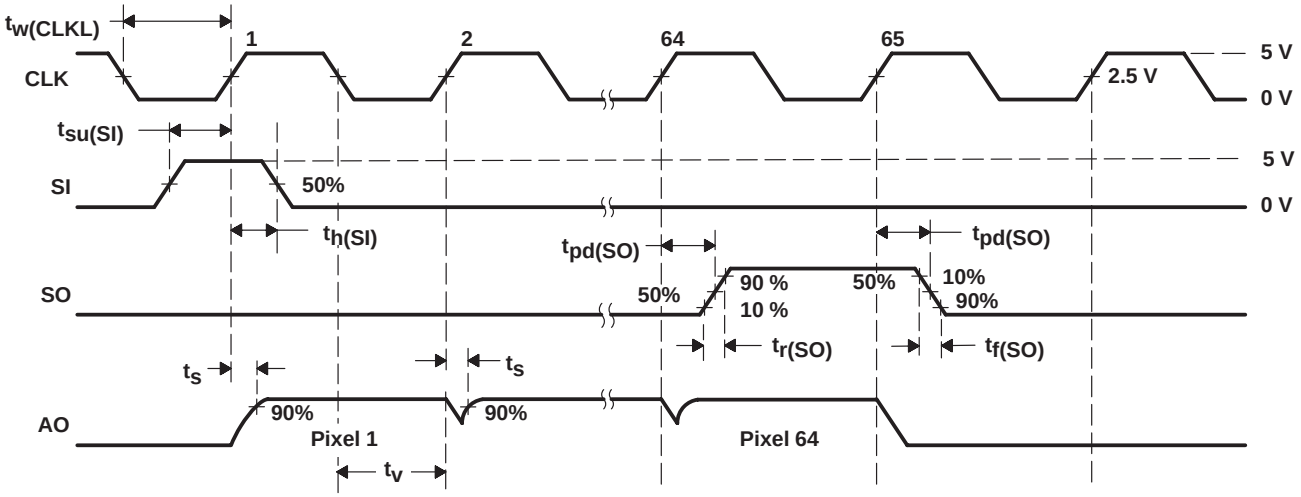
Figure 2. Parallel Configuration

PARAMETER MEASUREMENT INFORMATION



† Supply bypass capacitor with short leads should be placed as close to the device as possible.

TEST CIRCUIT



OPERATIONAL WAVEFORMS

Figure 3. Test Circuit and Operational Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED RESPONSIVITY vs WAVELENGTH OF INCIDENT LIGHT

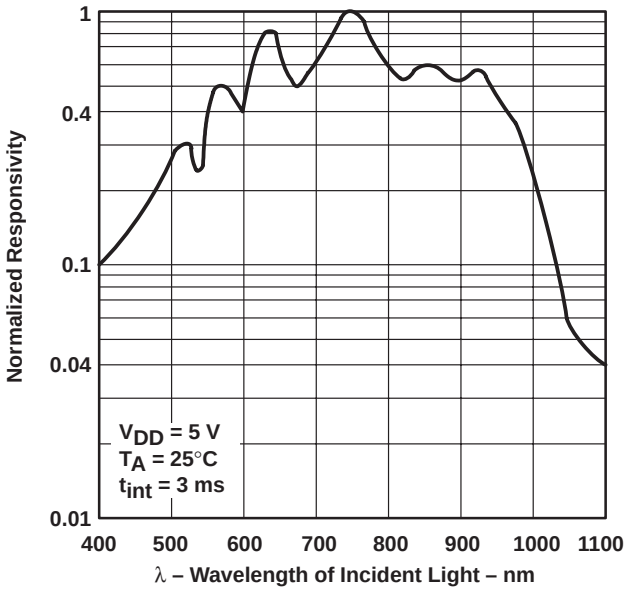


Figure 4

INTEGRATION TIME vs IRRADIANCE FOR CONSTANT AVERAGE ANALOG OUTPUT VOLTAGE

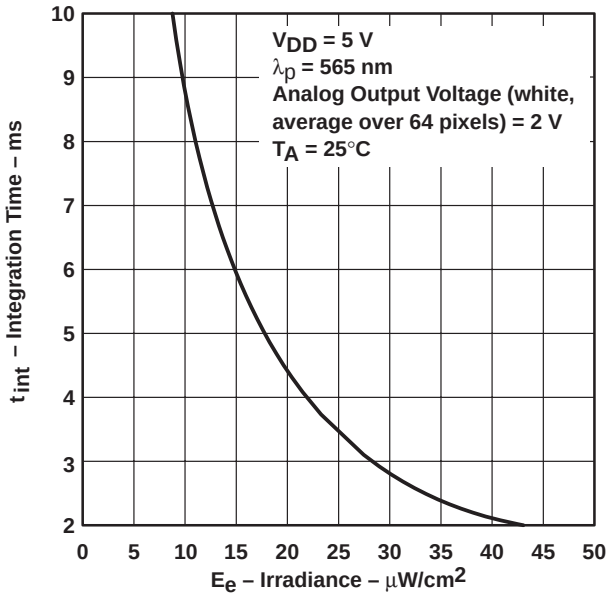


Figure 5

ANALOG OUTPUT VOLTAGE (DARK) vs INTEGRATION TIME

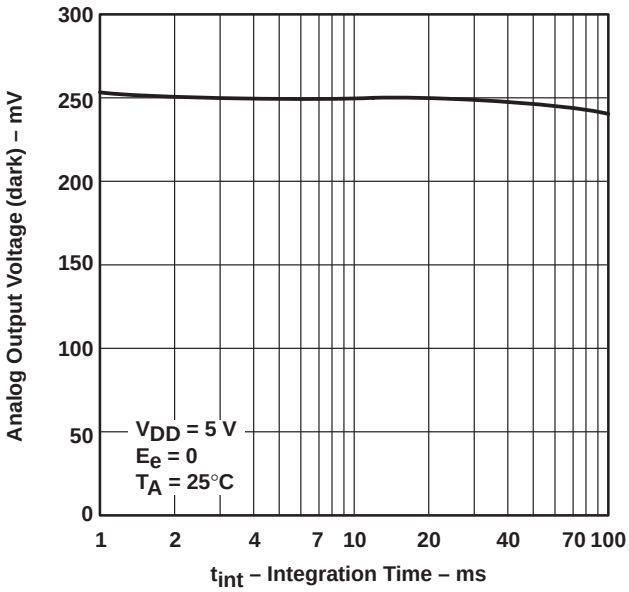


Figure 6

NORMALIZED OUTPUT VOLTAGE vs INTEGRATION TIME

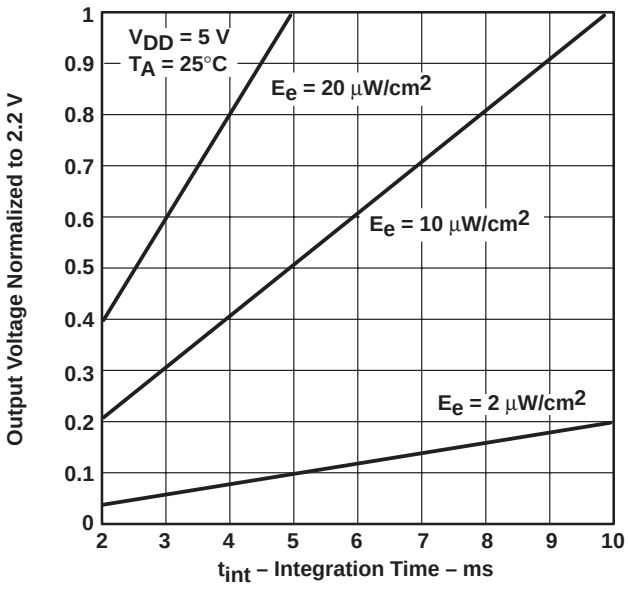
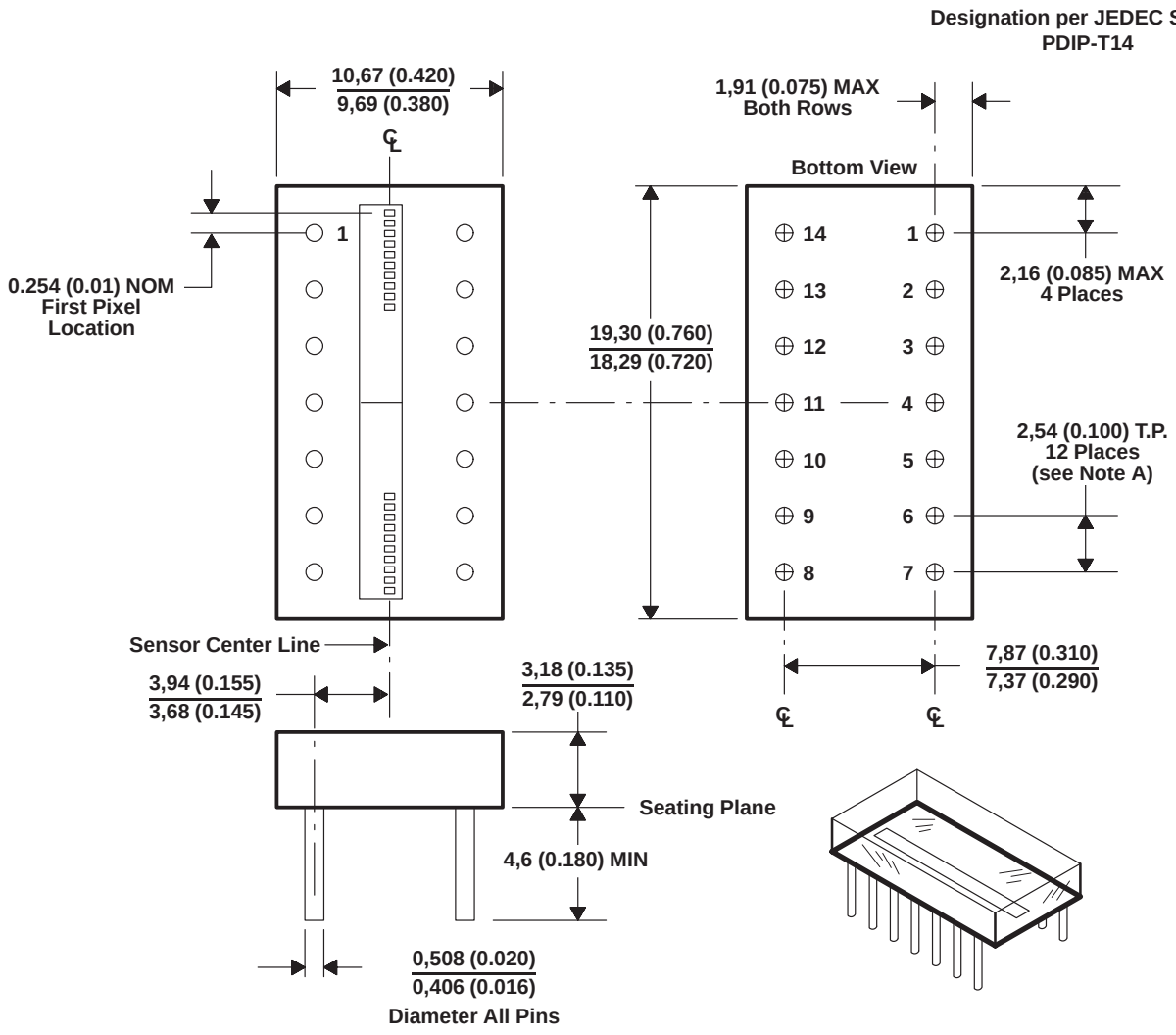


Figure 7

MECHANICAL DATA

This assembly consists of a sensor chip mounted on a printed-circuit board in a clear molded plastic package. The distance between the top surface of the package and the surface of the sensor is nominally 1 mm (0.040 inch).



NOTE A: The true-position spacing is 2,54 mm (0.100 inch) between lead centerlines. Each pin centerline is located within 0,25 mm (0.010 inch) of its true longitudinal positions.

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