

ISL28110, ISL28210

Precision Low Noise JFET Operational Amplifiers

FN6639

Rev 3.00

November 29, 2012

The ISL28110, ISL28210, are single and dual JFET amplifiers featuring low noise, high slew rate, low input bias current and offset voltage, making them the ideal choice for high impedance applications where precision and low noise are important. The combination of precision, low noise, and high speed combined with a small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision medical and analytical instrumentation, sensor conditioning, precision power supply controls, industrial controls and photodiode amplifiers.

The ISL28110 single amplifier and the ISL28210 dual amplifiers are available in the 8 Ld SOIC package. All devices are offered in standard pin configurations and operate over the extended temperature range from -40°C to +125°C.

Features

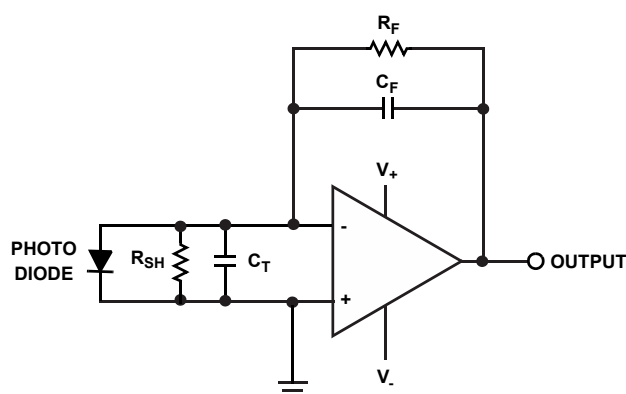
- Wide supply range 9V to 40V
- Low voltage noise. 6nV/ $\sqrt{\text{Hz}}$
- Input bias current. 2pA
- High slew rate. 23V/ μs
- High bandwidth 12.5MHz
- Low input offset 300 μV , Max
- Offset drift. Grade C 10 $\mu\text{V}/^\circ\text{C}$
- Low current consumption 2.55mA
- Operating temperature range. -40°C to +125°C
- Small package offerings in single, and dual
- No phase reversal
- Pb-Free (RoHS compliant)

Applications

- Precision instruments
- Photodiode amplifiers
- High impedance buffers
- Medical instrumentation
- Active filter blocks
- Industrial controls

Related Literature

- [AN1594](#) ISL28210SOICEVAL1Z Evaluation Board User's Guide



BASIC APPLICATION CIRCUIT - PHOTODIODE AMPLIFIER

FIGURE 1. TYPICAL APPLICATION

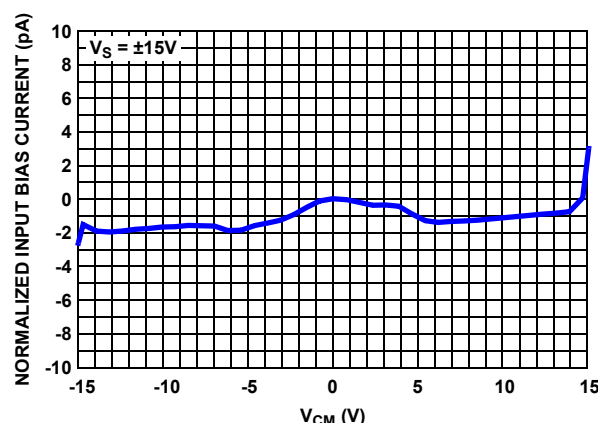
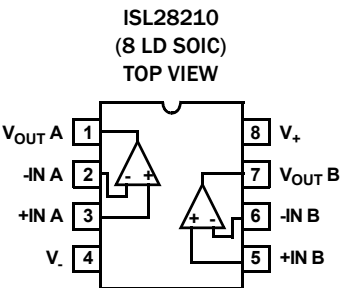
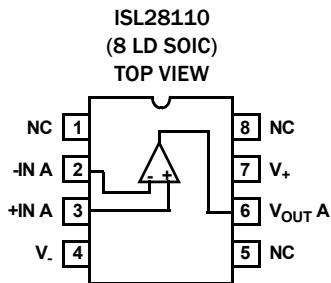


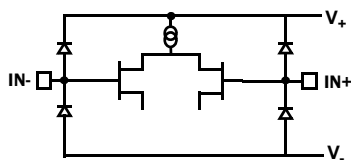
FIGURE 2. INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE

Pin Configuration

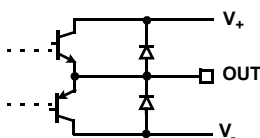


Pin Descriptions

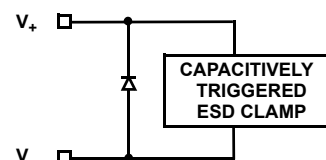
ISL28110 (8 LD SOIC)	ISL28210 (8 LD SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	+IN A	Circuit 1	Amplifier A non-inverting input
2	2	-IN A	Circuit 1	Amplifier A inverting input
6	1	V _{OUT A}	Circuit 2	Amplifier A output
4	4	V ₋	Circuit 3	Negative power supply
	5	+IN B	Circuit 1	Amplifier B non-inverting input
	6	-IN B	Circuit 1	Amplifier B inverting input
	7	V _{OUT B}	Circuit 2	Amplifier B output
7	8	V ₊	Circuit 3	Positive power supply
1, 5, 8		NC		No connect
		PAD		Thermal Pad is electrically isolated from active circuitry. Pad can float, connect to Ground or to a potential source that is free from signals or noise sources.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TCV _{OS} ($\mu\text{V}/^{\circ}\text{C}$)	PACKAGE (Pb-free)	PKG. DWG. #
ISL28110FBZ	28110 FBZ -C	10 (C Grade)	8 Ld SOIC	M8.15E
ISL28210FBZ	28210 FBZ -C	10 (C Grade)	8 Ld SOIC	M8.15E
ISL28210SOICEVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications..
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL28110](#), [ISL28210](#). For more information on MSL please see techbrief [TB363](#).

Absolute Voltage Ratings

Maximum Supply Voltage	42V
Maximum Supply Turn On Voltage Slew Rate	1V/ μ s
Maximum Differential Input Voltage	33V
Min/Max Input Voltage	$V_- - 0.5V$ to $V_+ + 0.5V$
Max/Min Input Current for Input Voltage $>V_+$ or $<V_-$	$\pm 20mA$
Output Short-Circuit Duration (1 output at a time)	Indefinite
ESD Ratings	
Human Body Model	4000V
Machine Model	400V
Charged Device Model	2000V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^{\circ}C/W$)	θ_{JC} ($^{\circ}C/W$)
8 Ld SOIC (Notes 5, 6)		
ISL28110	125	70
ISL28210	120	50
Ambient Operating Temperature Range	$-40^{\circ}C$ to $+125^{\circ}C$	
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$	
Operating Junction Temperature	$+150^{\circ}C$	
Pb-Free Reflow Profile	see link below	
	http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#).
- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For θ_{JC} , the "case temp" location is taken at the package top center.

Electrical Specifications $V_S = \pm 5V$, $V_{CM} = 0$, $V_{OUT} = 0V$, $T_A = +25^{\circ}C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+125^{\circ}C$.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage		-300		300	μV
		$-40^{\circ}C \leq T_A \leq +125^{\circ}C$	-1300		1300	μV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	$-40^{\circ}C \leq T_A \leq +125^{\circ}C$		1	10	$\mu V/^{\circ}C$
I_B	Input Bias Current ISL28110		-2	± 0.3	2	pA
		$-40^{\circ}C < T_A < +60^{\circ}C$	-5.3		5.3	pA
		$-40^{\circ}C < T_A < +85^{\circ}C$	-36		36	pA
		$-40^{\circ}C \leq T_A \leq +125^{\circ}C$	-235		235	pA
	Input Bias Current ISL28210		-2	± 0.3	2	pA
		$-40^{\circ}C < T_A < +60^{\circ}C$	-4.5		4.5	pA
		$-40^{\circ}C < T_A < +85^{\circ}C$	-50		50	pA
		$-40^{\circ}C \leq T_A \leq +125^{\circ}C$	-245		245	pA
I_{OS}	Input Offset Current ISL28110		-1	± 0.15	1	pA
		$-40^{\circ}C < T_A < +60^{\circ}C$	-2.25		2.25	pA
		$-40^{\circ}C < T_A < +85^{\circ}C$	-30		30	pA
		$-40^{\circ}C \leq T_A \leq +125^{\circ}C$	-105		105	pA
	Input Offset Current ISL28210		-1	± 0.15	1	pA
		$-40^{\circ}C < T_A < +60^{\circ}C$	-3.5		3.5	pA
		$-40^{\circ}C < T_A < +85^{\circ}C$	-32		32	pA
		$-40^{\circ}C \leq T_A \leq +125^{\circ}C$	-245		245	pA
$C_{IN-DIFF}$	Differential Input Capacitance			8.3		pF
C_{IN-CM}	Common Mode Input Capacitance			11.8		pF
$R_{IN-DIFF}$	Differential Input Resistance			530		$G\Omega$
R_{IN-CM}	Common Mode Input Resistance			560		$G\Omega$

Electrical Specifications $V_S = \pm 5V$, $V_{CM} = 0$, $V_{OUT} = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V _{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V ₋ + 1.5		V ₊ - 1.5	V
			V ₋ + 2.5		V ₊ - 2.5	V
CMRR	Common Mode Rejection Ratio	V _{CM} = -3.5V to +3.5V		90		dB
		V _{CM} = -2.5V to +2.5V	88	100		dB
A _{VOL}	Open-loop Gain	R _L = 10kΩ to ground V _O = -3V to +3V	104	108		dB
			103			dB
DYNAMIC PERFORMANCE						
GBWP	Gain-bandwidth Product	G = 100, R _L = 100kΩ, C _L = 4pF	11	12.5		MHz
SR	Slew Rate, V _{OUT} 20% to 80%	G = -1, R _L = 2kΩ, 4V Step		20		V/μs
THD+N	Total Harmonic Distortion + Noise	G = 1, f = 1kHz, 4V _{P-P} , R _L = 2kΩ		0.0002		%
		G = 1, f = 1kHz, 4V _{P-P} , R _L = 600Ω		0.0003		%
t _s	Settling Time to 0.1% 4V Step; 10% to V _{OUT}	A _V = 1, V _{OUT} = 4V _{P-P} , R _L = 2kΩ to V _{CM}		0.4		μs
	Settling Time to 0.01% 4V Step; 10% to V _{OUT}	A _V = 1, V _{OUT} = 4V _{P-P} , R _L = 2kΩ to V _{CM}		1		μs
NOISE PERFORMANCE						
e _{nP-P}	Peak-to-Peak Input Voltage Noise	0.1Hz to 10Hz		580		nV _{P-P}
e _n	Input Voltage Noise Spectral Density	f = 10Hz		14		nV/√Hz
		f = 100Hz		7		nV/√Hz
		f = 1kHz		6		nV/√Hz
		f = 10kHz		6		nV/√Hz
i _n	Input Current Noise Spectral Density	f = 1kHz		9		fA/√Hz
OUTPUT CHARACTERISTICS						
V _{OL}	Output Voltage Low, V _{OUT} to V ₋	R _L = 10kΩ		0.8	1.0	V
					1.1	V
		R _L = 2kΩ		0.9	1.1	V
					1.2	V
V _{OH}	Output Voltage High, V ₊ to V _{OUT}	R _L to GND = 10kΩ		0.8	1.0	V
					1.1	V
		R _L to GND = 2kΩ		0.9	1.1	V
					1.2	V
I _{SC}	Output Short Circuit Current	R _L = 10Ω to V ₊ . V ₋		±50		mA
POWER SUPPLY						
V _{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	±4.5		±20V	V
PSRR	Power Supply Rejection Ratio	V _S = ± 4.5V to ±5V	102	115		dB
			100			dB
I _S	Supply Current/Amplifier			2.5	2.9	mA
					3.8	mA

Electrical Specifications $V_S = \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
INPUT CHARACTERISTICS						
V _{OS}	Input Offset Voltage		-300		300	μV
		-40 °C ≤ T _A ≤ +125 °C	-1300		1300	μV
TCV _{OS}	Input Offset Voltage Temperature Coefficient (Grade C)	-40 °C ≤ T _A ≤ +125 °C		1	10	μV/°C
I _B	Input Bias Current ISL28110		4.5	±2	4.5	pA
		-40 °C < T _A < +60 °C	-25		25	pA
		-40 °C < T _A < +85 °C	-85		85	pA
		-40 °C ≤ T _A ≤ +125 °C	-950		950	pA
I _B	Input Bias Current ISL28210		5	±2	5	pA
		-40 °C < T _A < +60 °C	-350		350	pA
		-40 °C < T _A < +85 °C	-700		700	pA
		-40 °C ≤ T _A ≤ +125 °C	-3600		3600	pA
I _{OS}	Input Offset Current ISL28110		-2.5	±0.5	2.5	pA
		-40 °C < T _A < +60 °C	-25		25	pA
		-40 °C < T _A < +85 °C	-85		85	pA
		-40 °C ≤ T _A ≤ +125 °C	-650		650	pA
I _{OS}	Input Offset Current ISL28210		-2.5	±0.5	2.5	pA
		-40 °C < T _A < +60 °C	-285		285	pA
		-40 °C < T _A < +85 °C	-445		445	pA
		-40 °C ≤ T _A ≤ +125 °C	-2000		2000	pA
C _{IN-DIFF}	Differential Input Capacitance			8.3		pF
C _{IN-CM}	Common Mode Input Capacitance			11.8		pF
R _{IN-DIFF}	Differential Input Resistance			530		GΩ
R _{IN-CM}	Common Mode Input Resistance			560		GΩ
V _{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V ₋ + 1.5		V ₊ - 1.5	V
CMRR	Common Mode Rejection Ratio	V _{CM} = -13.5V to +13.5V	80	100		dB
A _{VOL}	Open-loop Gain	R _L = 10kΩ to ground V _O = -12.5V to +12.5V	107	109		dB
		-40 °C ≤ T _A ≤ +125 °C	106			dB
DYNAMIC PERFORMANCE						
GBWP	Gain-bandwidth Product	G = 100, R _L = 100kΩ, C _L = 4pF	11	12.5		MHz
SR	Slew Rate, V _{OUT} 20% to 80%	G = -1, R _L = 2kΩ, 10V Step		20		V/μs
THD+N	Total Harmonic Distortion + Noise	G = 1, f = 1kHz, 10V _{P-P} , R _L = 2kΩ		0.00025		%
		G = 1, f = 1kHz, 10V _{P-P} , R _L = 600Ω		0.0003		%
t _s	Settling Time to 0.1% 10V Step; 10% to V _{OUT}	A _V = 1, V _{OUT} = 10V _{P-P} , R _L = 2kΩ to V _{CM}		1.3		μs
	Settling Time to 0.01% 10V Step; 10% to V _{OUT}	A _V = 1, V _{OUT} = 10V _{P-P} , R _L = 2kΩ to V _{CM}		1.6		μs

Electrical Specifications $V_S = \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$.** (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
NOISE PERFORMANCE						
$e_{n\text{P-P}}$	Peak-to-Peak Input Voltage Noise	0.1Hz to 10Hz		600		nV _{P-P}
e_n	Input Voltage Noise Spectral Density	$f = 10\text{Hz}$		18		nV/ $\sqrt{\text{Hz}}$
		$f = 100\text{Hz}$		7.8		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		6		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{kHz}$		6		nV/ $\sqrt{\text{Hz}}$
i_n	Input Current Noise Spectral Density	$f = 1\text{kHz}$		9		fA/ $\sqrt{\text{Hz}}$
OUTPUT CHARACTERISTICS						
V_{OL}	Output Voltage Low, V_{OUT} to V_-	$R_L = 10\text{k}\Omega$		0.8	1.0	V
					1.1	V
		$R_L = 2\text{k}\Omega$		0.9	1.1	V
					1.2	V
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L to GND = $10\text{k}\Omega$		0.8	1.0	V
					1.1	V
		R_L to GND = $2\text{k}\Omega$		0.9	1.1	V
					1.2	V
I_{SC}	Output Short Circuit Current	$R_L = 10\Omega$ to V_+ , V_-		± 50		mA
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 20V$	102	115		dB
			100			dB
I_S	Supply Current/Amplifier			2.55	3.1	mA
					3.9	mA

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T = +25^\circ\text{C}$, unless otherwise specified.

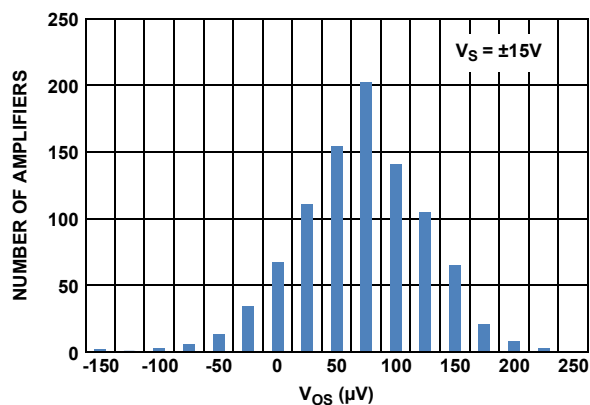


FIGURE 3. INPUT OFFSET VOLTAGE (V_{OS}) DISTRIBUTION

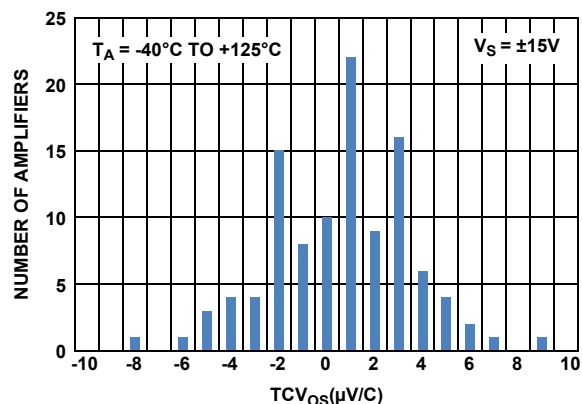


FIGURE 4. $T_C V_{OS}$ DISTRIBUTION, -40°C to $+125^\circ\text{C}$

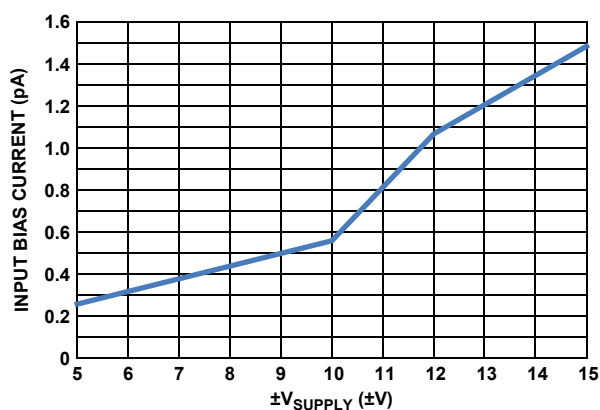


FIGURE 5. INPUT BIAS CURRENT (I_B) vs SUPPLY VOLTAGE

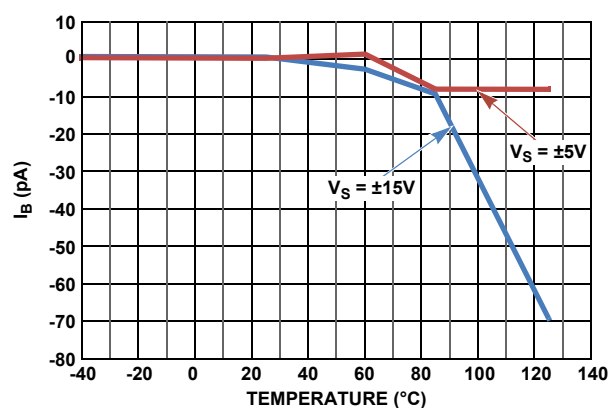


FIGURE 6. ISL28110 INPUT BIAS CURRENT (I_B) vs TEMPERATURE

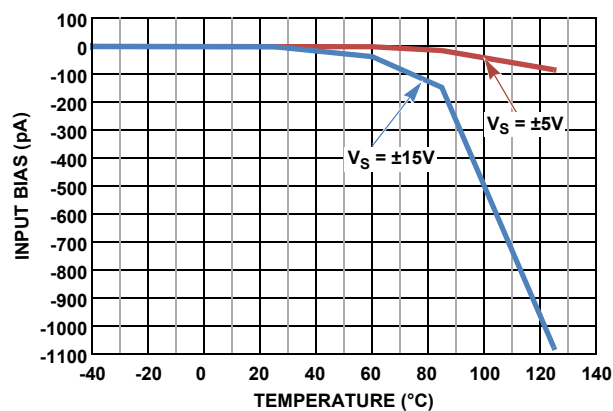


FIGURE 7. ISL28210 INPUT BIAS CURRENT (I_B) vs TEMPERATURE

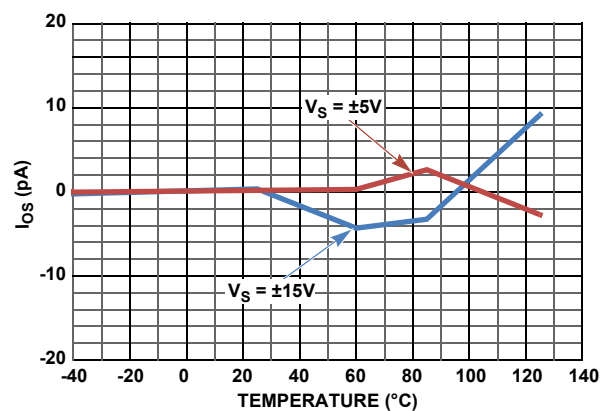


FIGURE 8. ISL28110 INPUT OFFSET CURRENT (I_{OS}) vs TEMPERATURE

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T = +25^\circ C$, unless otherwise specified. (Continued)

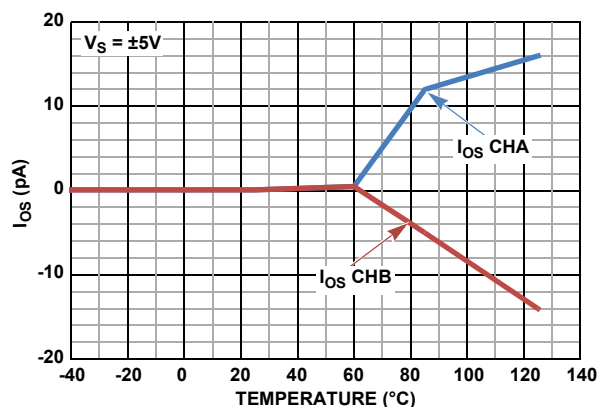


FIGURE 9. ISL28210 INPUT OFFSET CURRENT (I_{OS}) vs TEMPERATURE, $V_S = \pm 5V$

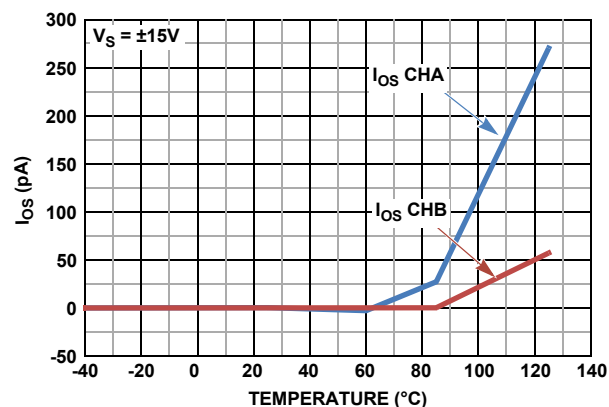


FIGURE 10. ISL28210 INPUT OFFSET CURRENT (I_{OS}) vs TEMPERATURE, $V_S = \pm 15V$

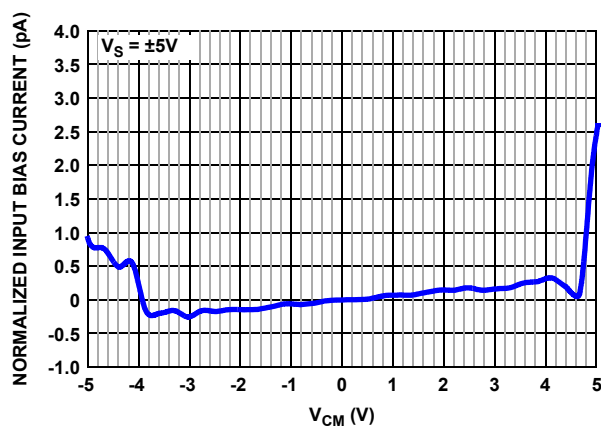


FIGURE 11. NORMALIZED INPUT BIAS CURRENT (I_B) vs INPUT COMMON MODE VOLTAGE (V_{CM}), $V_S = \pm 5V$

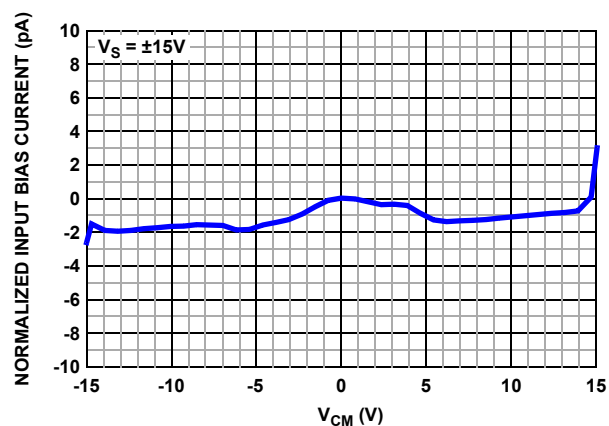


FIGURE 12. NORMALIZED INPUT BIAS CURRENT (I_B) vs INPUT COMMON MODE VOLTAGE (V_{CM}), $V_S = \pm 15V$

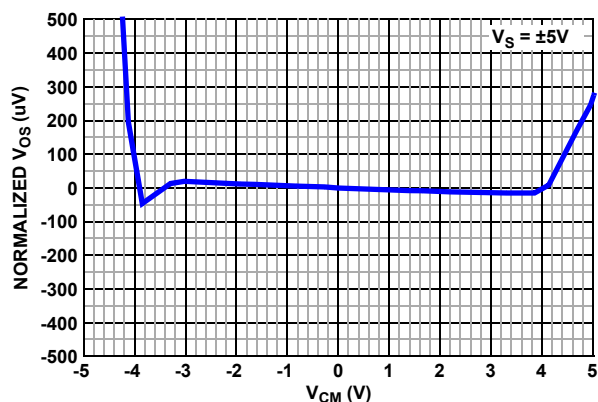


FIGURE 13. NORMALIZED INPUT OFFSET VOLTAGE (V_{OS}) vs INPUT COMMON MODE VOLTAGE (V_{CM}), $V_S = \pm 5V$

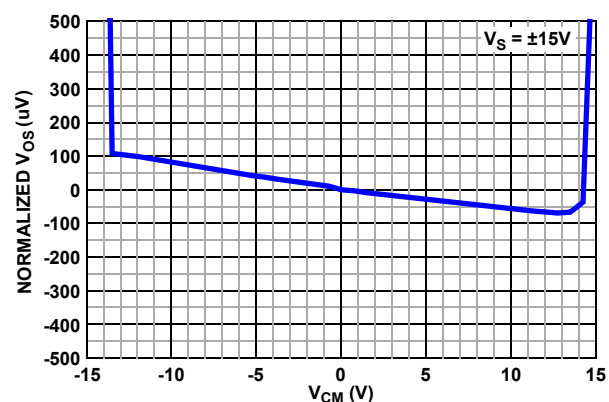


FIGURE 14. NORMALIZED INPUT OFFSET VOLTAGE (V_{OS}) vs INPUT COMMON MODE VOLTAGE (V_{CM}), $V_S = \pm 15V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T = +25^\circ\text{C}$, unless otherwise specified. (Continued)

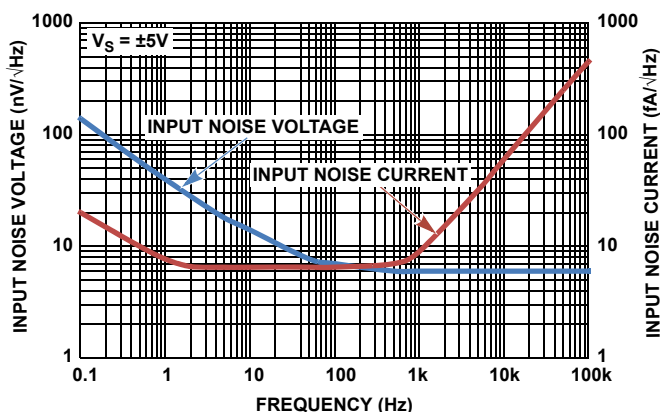


FIGURE 15. INPUT NOISE VOLTAGE (e_n) AND CURRENT (i_n) vs FREQUENCY, $V_S = \pm 5V$

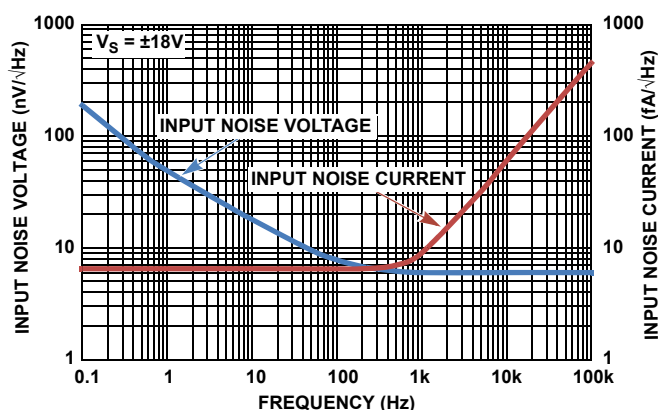


FIGURE 16. INPUT NOISE VOLTAGE (e_n) AND CURRENT (i_n) vs FREQUENCY, $V_S = \pm 18V$

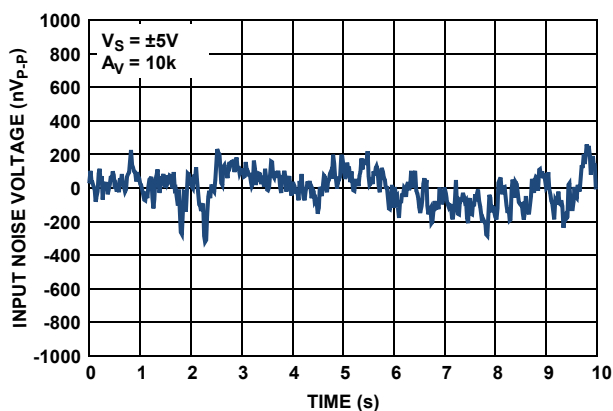


FIGURE 17. 0.1Hz to 10Hz V_{P-P} NOISE VOLTAGE, $V_S = \pm 5V$

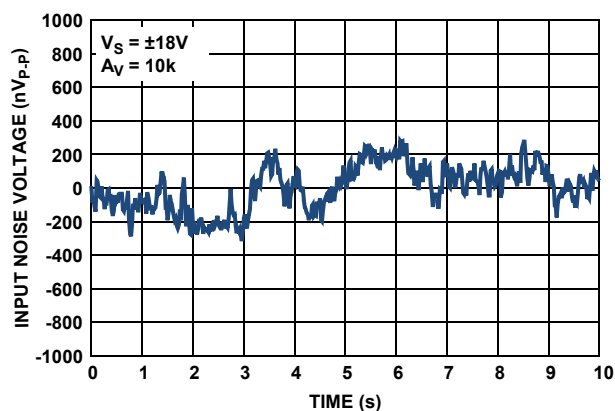


FIGURE 18. 0.1Hz to 10Hz V_{P-P} NOISE VOLTAGE, $V_S = \pm 18V$

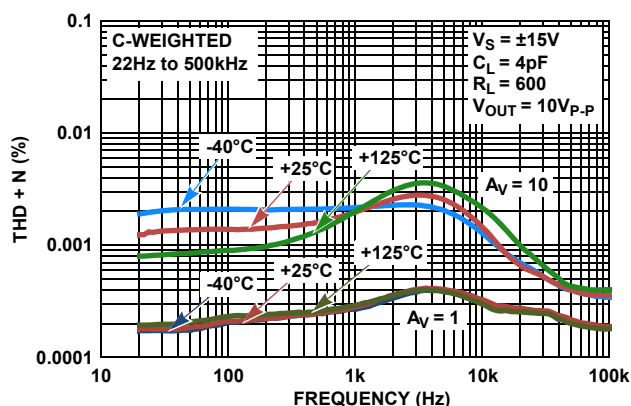


FIGURE 19. THD+N vs FREQUENCY vs TEMPERATURE, $A_V = 1, 10$, $V_{OUT} = 10V_{P-P}$, $R_L = 600\Omega$

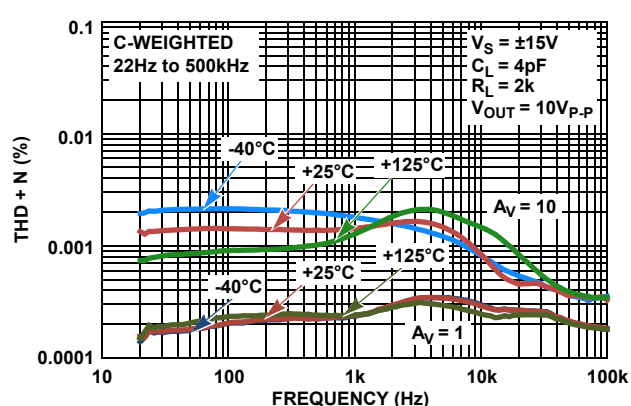


FIGURE 20. THD+N vs FREQUENCY vs TEMPERATURE, $V_{OUT} = 10V_{P-P}$, $R_L = 2k\Omega$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T = +25^\circ C$, unless otherwise specified. (Continued)

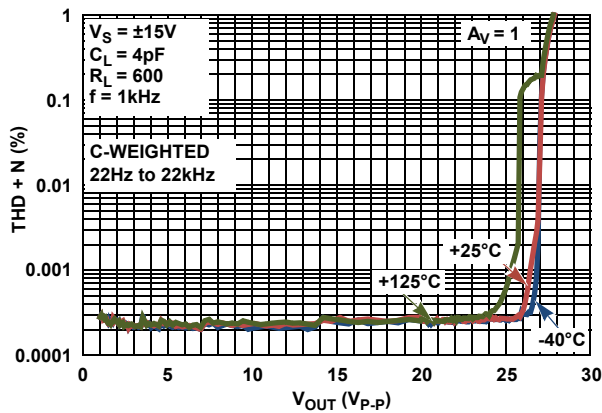


FIGURE 21. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, $A_V = 1$ $f = 1kHz$, $R_L = 600\Omega$

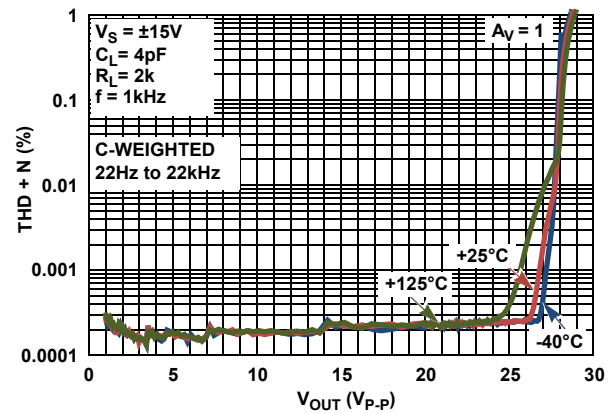


FIGURE 22. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, $A_V = 1$ $f = 1kHz$, $R_L = 2k\Omega$

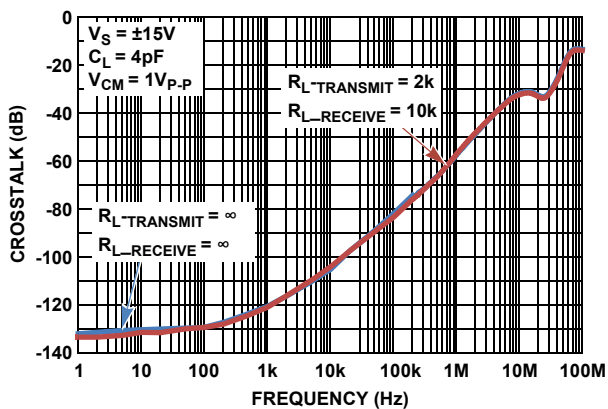


FIGURE 23. CROSSTALK vs FREQUENCY

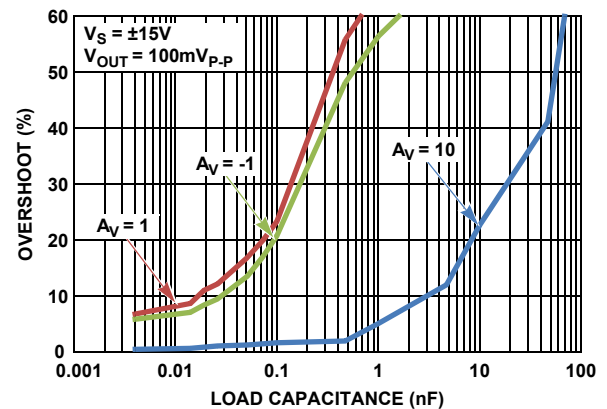


FIGURE 24. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE (C_L)

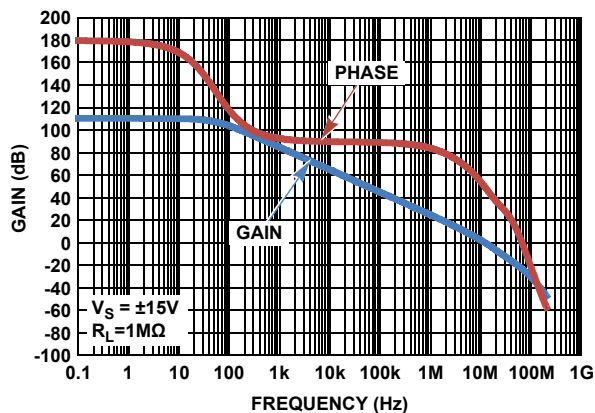


FIGURE 25. OPEN LOOP GAIN-PHASE vs FREQUENCY

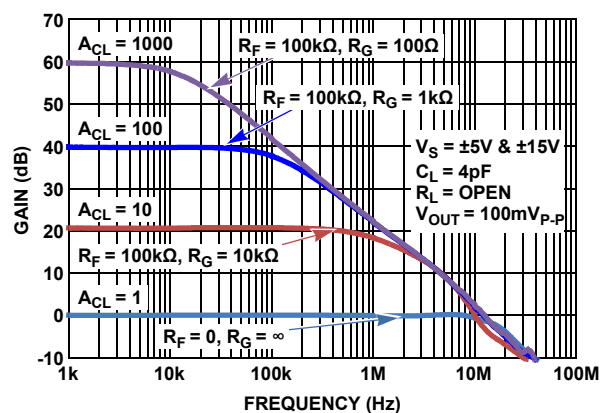


FIGURE 26. CLOSED LOOP GAIN vs FREQUENCY

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T = +25^\circ C$, unless otherwise specified. (Continued)

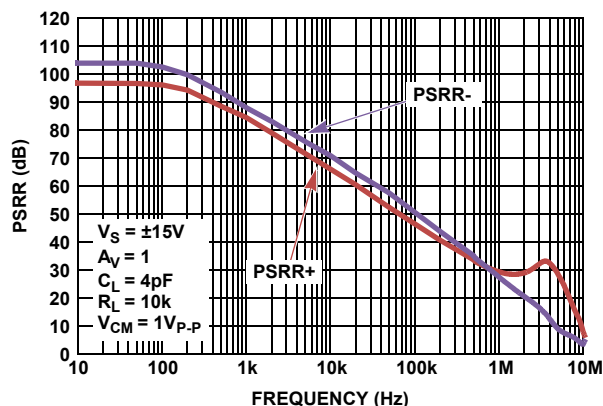


FIGURE 27. POWER SUPPLY REJECTION RATIO (PSRR) vs FREQUENCY

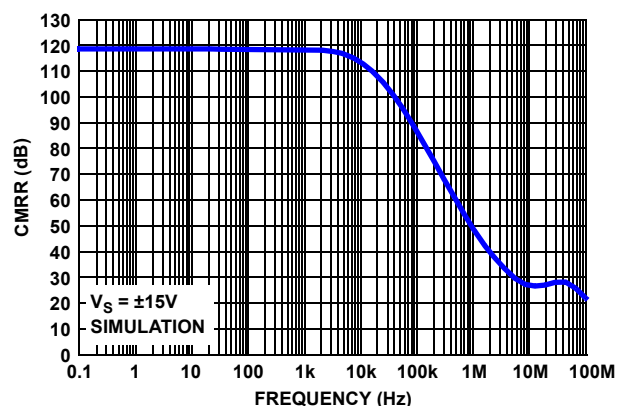


FIGURE 28. COMMON-MODE REJECTION RATIO (CMRR) vs FREQUENCY

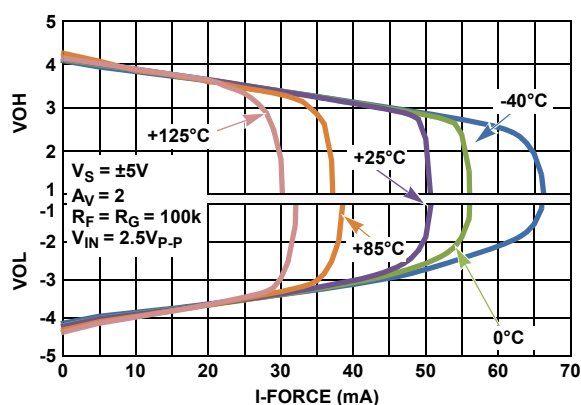


FIGURE 29. OUTPUT VOLTAGE (V_{OUT}) vs OUTPUT CURRENT (I_{OUT}) vs TEMPERATURE, $V_S = \pm 5V$

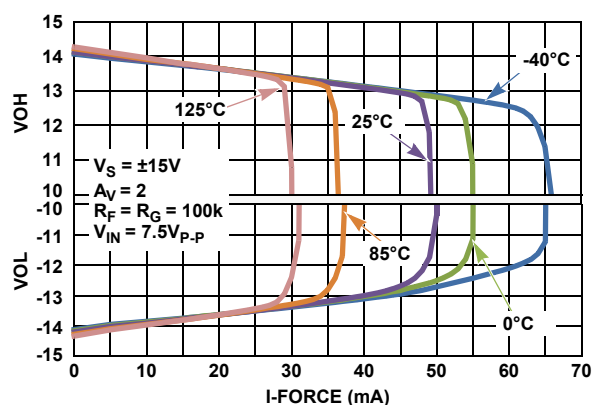


FIGURE 30. OUTPUT VOLTAGE (V_{OUT}) vs OUTPUT CURRENT (I_{OUT}) vs TEMPERATURE, $V_S = \pm 15V$

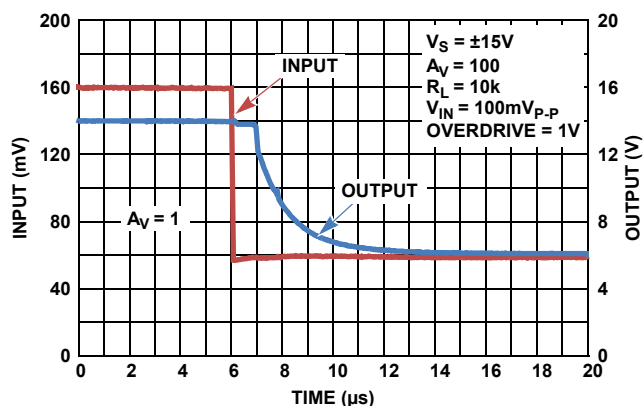


FIGURE 31. POSITIVE OUTPUT OVERLOAD RECOVERY TIME

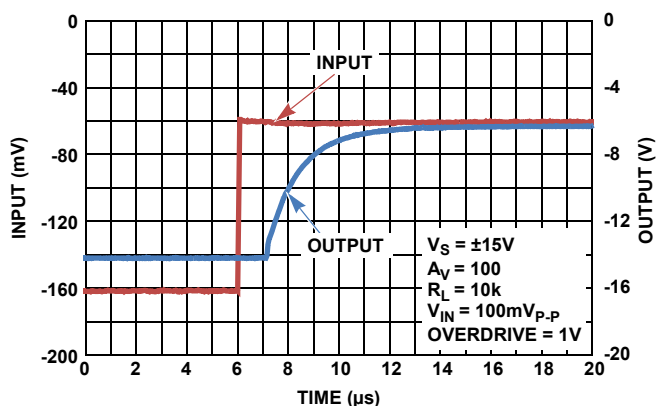


FIGURE 32. NEGATIVE OUTPUT OVERLOAD RECOVERY TIME

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T = +25^\circ C$, unless otherwise specified. (Continued)

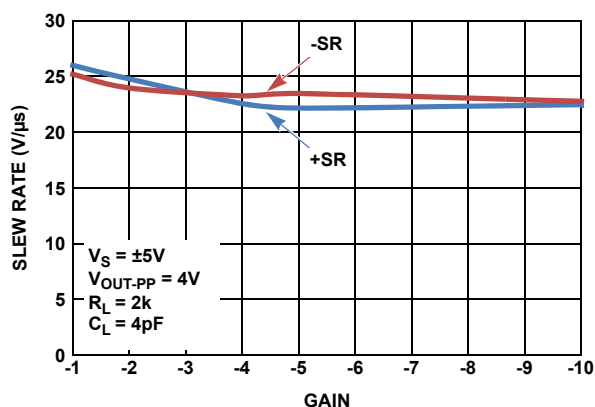


FIGURE 33. SLEW RATE vs INVERTING CLOSED LOOP GAIN, $V_S = \pm 5V$

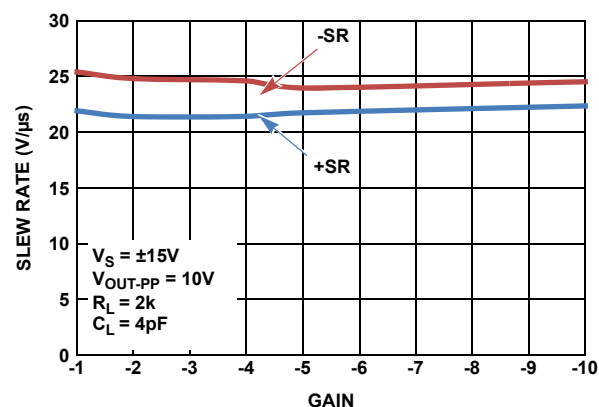


FIGURE 34. SLEW RATE vs INVERTING CLOSED LOOP GAIN, $V_S = \pm 15V$

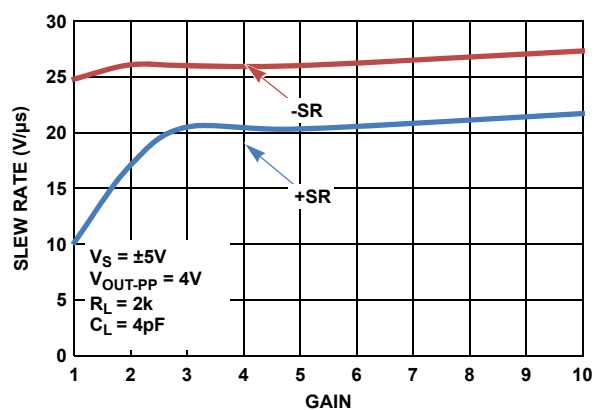


FIGURE 35. SLEW RATE vs NON-INVERTING CLOSED LOOP GAIN, $V_S = \pm 5V$

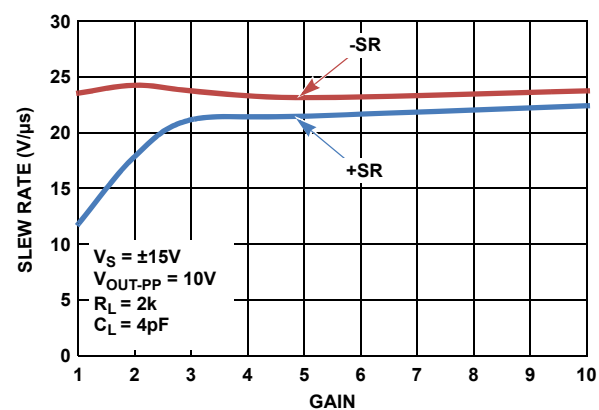


FIGURE 36. SLEW RATE vs NON-INVERTING CLOSED LOOP GAIN, $V_S = \pm 15V$

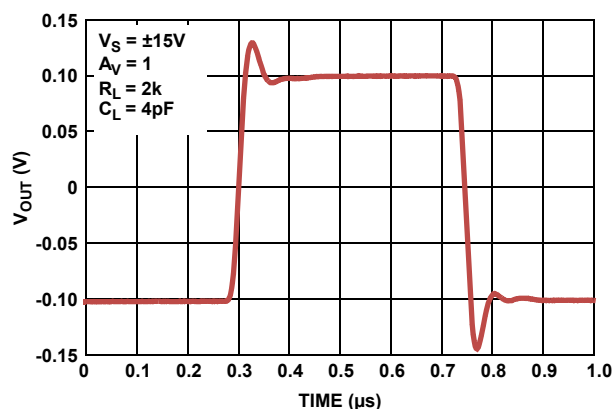


FIGURE 37. SMALL SIGNAL TRANSIENT RESPONSE

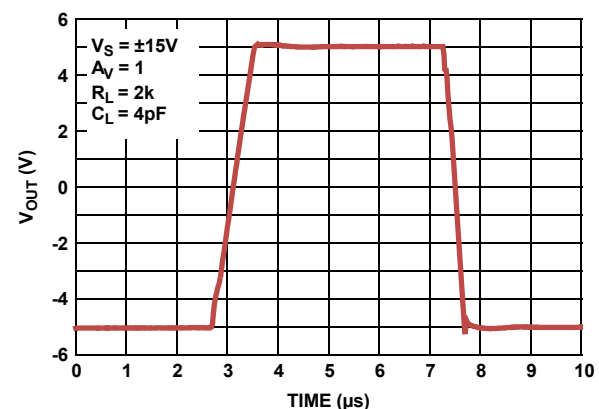


FIGURE 38. LARGE SIGNAL UNITY GAIN TRANSIENT RESPONSE

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T = +25^\circ C$, unless otherwise specified. (Continued)

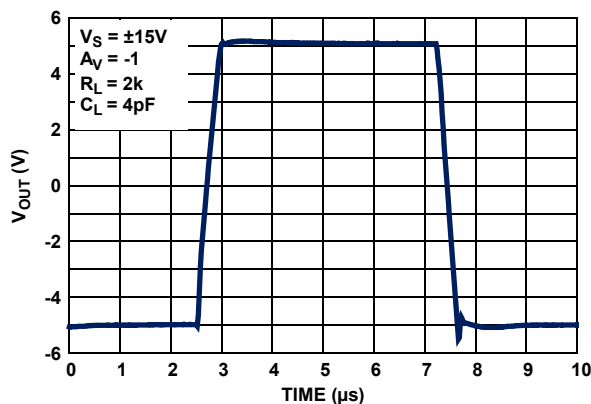


FIGURE 39. LARGE SIGNAL 10V STEP RESPONSE $A_V = -1$

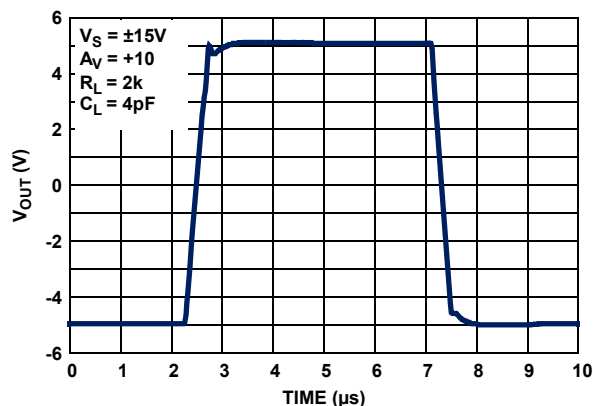


FIGURE 40. LARGE SIGNAL 10V STEP RESPONSE $A_V = +10$

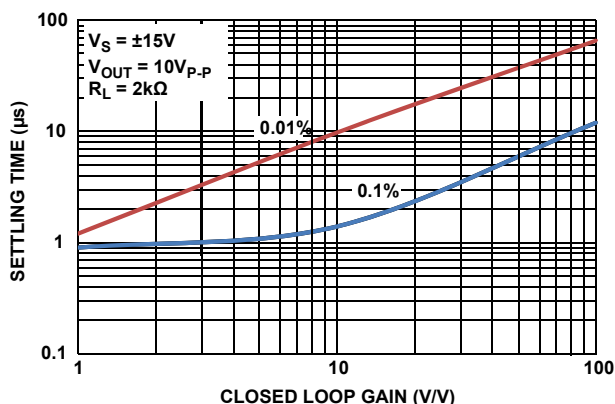


FIGURE 41. SETTLING TIME (t_S) vs CLOSED LOOP GAIN

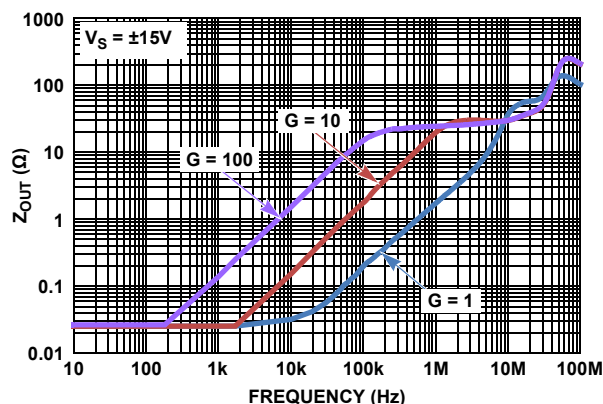


FIGURE 42. Z_{OUT} vs FREQUENCY

Applications Information

Functional Description

The ISL28110 and ISL28210 are single and dual 12.5 MHz precision JFET input op amps. These devices are fabricated in the PR40 Advanced Silicon-on-Insulator (SOI) bipolar-JFET process to ensure latch-free operation. The precision JFET input stage provides low input offset voltage (300 μV max @ $+25^\circ C$), low input voltage noise (6nV/ $\sqrt{Hz}$), and input current noise that is very low with virtually no $1/f$ component. A high current complementary NPN/PNP emitter-follower output stage provides high slew rate and maintains excellent THD+N performance into heavy loads (0.0003% @ 10V $_{P-P}$ @ 1kHz into 600 Ω).

Operating Voltage Range

The devices are designed to operate over the 9V ($\pm 4.5V$) to 40V ($\pm 20V$) range and are fully characterized at 10V ($\pm 5V$) and 30V ($\pm 15V$). The JFET input stage maintains high impedance over a maximum input differential voltage range of $\pm 33V$. Internal ESD protection diodes clamp the non-inverting and inverting inputs to one diode drop above and below the $V+$ and $V-$ the power supply rails ("Pin Descriptions" on page 2, CIRCUIT 1).

Input ESD Diode Protection

The JFET gate is a reverse-biased diode with $>33V$ reverse breakdown voltage which enables the device to function reliably in large signal pulse applications without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. No special input signal restrictions are needed for power supply operation up to $\pm 15V$, and input signal distortion caused by nonlinear clamps under high slew rate conditions are avoided. For power supply operation greater than $\pm 16V$ ($>32V$), the internal ESD clamp diodes alone cannot clamp the maximum input differential signal to the power supply rails without the risk of exceeding the 33V breakdown of the JFET gate. Under these conditions, differential input voltage limiting is necessary to prevent damage to the JFET input stage.

In applications where one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current limiting resistors may be needed at each input terminal (see Figure 43 R_{IN+} , R_{IN-}) to limit current through the power supply ESD diodes to 20mA.

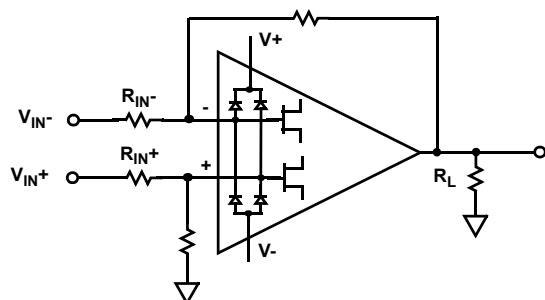


FIGURE 43. INPUT ESD DIODE CURRENT LIMITING

JFET Input Stage Performance

The ISL28110, ISL28210 JFET input stage has the linear gain characteristics of the MOSFET but can operate at high frequency with much lower noise. The reversed-biased gate PN gate junction has significantly lower gate capacitance than the MOSFET, enabling input slew rates that rival op amps using bipolar input stages. The added advantage for high impedance, precision amplifiers is the lack of a significant $1/f$ component of current noise (Figures 15, 16) as there is virtually no gate current.

The input stage JFETs are bootstrapped to maintain a constant JFET drain to source voltage which keeps the JFET gate currents and input stage frequency response nearly constant over the common mode input range of the device. These enhancements provide excellent CMRR, AC performance and very low input distortion over a wide temperature range. The common mode input performance for offset voltage and bias current is shown in Figure 44. Note that the input bias current remains low even after the maximum input stage common mode voltage is exceeded (as indicated by the abrupt change in input offset voltage).

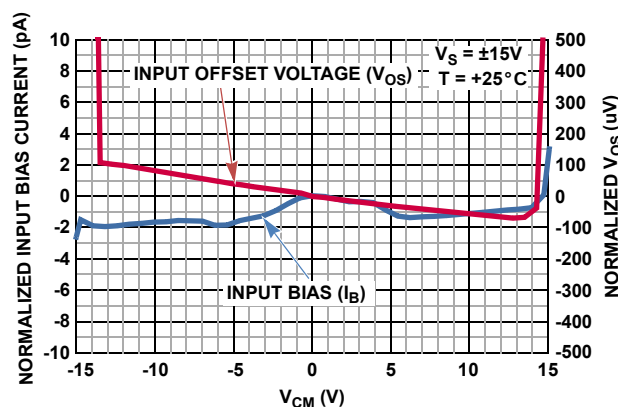


FIGURE 44. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs COMMON MODE INPUT VOLTAGE

Output Drive Capability

The complementary bipolar emitter follower output stage features low output impedance (Figure 42) and is capable of substantial current drive over the full temperature range (Figures 29, 30) while driving the output voltage close to the supply rails. The output current is internally limited to approximately $\pm 50\text{mA}$ at $+25^\circ\text{C}$. The amplifiers can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28110 and ISL28210 are immune to output phase reversal, out to 0.5V beyond the rail ($V_{\text{ABS MAX}}$) limit. Beyond these limits, the device is still immune to reversal to 1V beyond the rails but damage to the internal ESD protection diodes can result unless these input currents are limited.

Maximizing Dynamic Signal Range

The amplifiers maximum undistorted output swing is a figure of merit for precision, low distortion applications. Audio amplifiers are a good example of amplifiers that require low noise and low signal distortion over a wide output dynamic range. When these applications operate from batteries, raising the amplifier supply voltage to overcome poor output voltage swing has the penalty of increased power consumption and shorter battery life. Amplifiers whose input and output stages can swing closest to the power supply rails while providing low noise and undistorted performance, will provide maximum useful dynamic signal range and longer battery life.

Rail-to-rail input and output (RRIO) amplifiers have the highest dynamic signal range but their added complexity degrades input noise and amplifier distortion. Many contain two input pairs, one pair operating to each supply rail. The trade-offs for these are increased input noise and distortion caused by non-linear input bias current and capacitance when amplifying high impedance sources. Their rail-to-rail output stages swing to within a few millivolts of the rail, but output impedances are high so that their output swing decreases and distortion increases rapidly with increasing load current. At heavy load currents the maximum output voltage swing of RRO op amps can be lower than a good emitter follower output stage.

The ISL28110 and ISL28210 low noise input stage and high performance output stage are optimized for low THD+N into moderate loads over the full -40°C to $+125^\circ\text{C}$ temperature range. Figures 21 and 22 show the 1kHz THD+N unity gain performance vs output voltage swing at load resistances of $2\text{k}\Omega$ and 600Ω . Figure 45 shows the unity-gain THD+N performance driving 600Ω from $\pm 5\text{V}$ supplies.

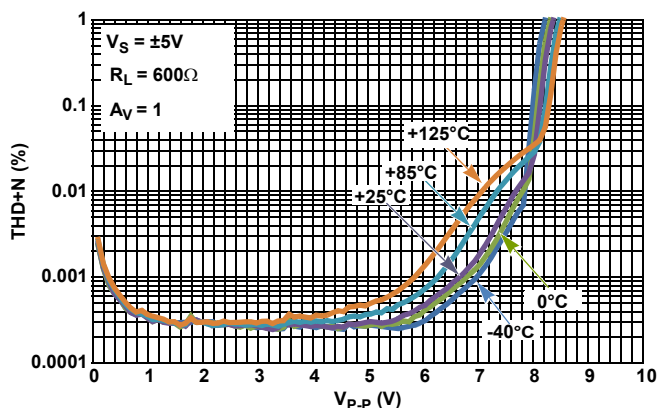


FIGURE 45. UNITY-GAIN THD+N vs OUTPUT VOLTAGE vs TEMPERATURE AT $V_S = \pm 5V$ FOR 600Ω LOAD

Power Dissipation

It is possible to exceed the $+150^\circ\text{C}$ maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad (EQ. 1)$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

ISL28110 and ISL28210 SPICE Model

Figure 46 shows the SPICE model schematic and Figure 47 shows the net list for the SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: $1/f$ and flatband noise voltage, Slew Rate, CMRR, Gain and Phase. The DC parameters are I_{OS} , total supply current and output voltage swing. The model uses typical parameters given in the "Electrical Specifications" Table beginning on page 4. The AVOL is adjusted for 125dB with the dominant pole at 7Hz. The CMRR is set 120dB, $f = 280\text{kHz}$. The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of $+25^\circ\text{C}$.

Figures 48 through 61 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Small Signal 0.1V Step, Large Signal 5V Step Response, Open Loop Gain Phase, CMRR and Output Voltage Swing for $\pm 5V$ and $\pm 15V$ supplies.

LICENSE STATEMENT

The information in this SPICE model is protected under the United States copyright laws. Intersil Corporation hereby grants users of this macro-model hereto referred to as "Licensee", a nonexclusive, nontransferable licence to use this model as long as the Licensee abides by the terms of this agreement. Before using this macro-model, the Licensee should read this license. If the Licensee does not accept these terms, permission to use the model is not granted.

The Licensee may not sell, loan, rent, or license the macro-model, in whole, in part, or in modified form, to anyone outside the Licensee's company. The Licensee may modify the macro-model to suit his/her specific applications, and the Licensee may make copies of this macro-model for use within their company only.

This macro-model is provided "AS IS, WHERE IS, AND WITH NO WARRANTY OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUY NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE."

In no event will Intersil be liable for special, collateral, incidental, or consequential damages in connection with or arising out of the use of this macro-model. Intersil reserves the right to make changes to the product and the macro-model without prior notice.



```
* source ISL28110_210_presubckt_0
* Revision A, LaFontaine Nov 4th 2010
* Model for Noise 200nV/rHz@0.1Hz
* 11nV/rHz base band, supply current 2.5mA,
* CMRR 120dB fcm=281kHz ,AVOL 125dB
* fd=7Hz
* SR = 20V/us, GBWP 12.6MHz, Output
*voltage clamp
* Copyright 2010 by Intersil Corporation
* Refer to data sheet "LICENSE
STATEMENT" *Use of this model indicates
your acceptance *with the terms and
provisions in the License *Statement.
* Connections:
```

	+input	-input	Vsupply	-Vsupply	output
*					
*					
*					
*					
*					

```
.subckt ISL28110subckt Vin+ Vin- V+ V-
VOUT
* source ISL28110_210_PRESUBCKT_0
* Voltage Noise
E_En VIN+ 4 2 0 1
V_V1 1 0 0 4
D_D1 1 2 DN
R_R1 2 0 110
* Input Stage
R_R2 VIN- 3 5e11
R_R3 3 4 5e11
C_CinDif 4 VIN- 5.87E-12
C_Cin1 V-- VIN- 7.27e-12
C_Cin2 V-- 4 7.27e-12
I_IOS 4 VIN- DC 0.3E-12
R_R4 5 VIN- 250
J_J1 7 5 6 pj110_input
J_J2 15 16 14 pj110_input
J_J3 V-- 14 15 PJ110_CASCADE
J_J4 V-- 6 7 PJ110_CASCADE
Q_Q1 19 13 14 NPN_CASCADE
Q_Q2 12 13 6 NPN_CASCADE
Q_Q4 8 13 6 NPN_CASCADE
Q_Q5 12 13 14 NPN_CASCADE
Q_Q6 19 11 20 PNP_MIRROR
Q_Q7 8 11 9 PNP_MIRROR
V_V2 V++ 10 0.7Vdc
V_V3 V++ 21 0.7Vdc
R_R5 9 10 5.5k
R_R6 20 21 5.5k
E_buffer1 11 V++ 8 V++ 1
E_buffer2 13 V-- 12 V-- 1
D_D2 8 19 DBREAK
D_D3 19 8 DBREAK
I_I1 V++ 12 DC 240E-6
C_C1 19 V++ 4e-12
C_C2 V-- 19 4e-12
R_R7 16 17 250
E EOS 17 4 VC VMID 1
* 1st Gain Stage
R_R8 18 V++ 100
D_D4 V-- 18 DBREAK
D_D5 22 V++ DX
D_D6 V-- 24 DX
V_V4 22 23 1.18
V_V5 23 24 1.18
G_G1 V++ 23 19 8 33
G_G2 V-- 23 19 8 33
R_R9 23 V++ 1
R_R10 V-- 23 1
R_R11 25 23 1k
D_D7 25 VMID DX
D_D8 VMID 25 DX
R_R12 25 VMID 1e10
G_G3 V++ VG 25 VMID 181.819E-6
G_G4 V-- VG 25 VMID 181.819E-6
D_D9 26 V++ DX
D_D10 V-- 27 DX
V_V6 26 VG 1.18
V_V7 VG 27 1.18
R_R13 VG V++ 200k
R_R14 V-- VG 200k
C_C3 8 VG 6e-12
C_C4 VG V++ 2.5e-12
C_C5 V-- VG 2.5e-12
* Mid Supply Reference
E_E2 VMID V-- V++ V-- 0.5
E_E3 V++ 0 V+ 0 1
E_E4 V-- 0 V- 0 1
I_ISY V+ V- DC 2.5E-3
* Common Mode Gain Stage 40dB/dec
G_G5 V++ 29 3 VMID 1
G_G6 V-- 29 3 VMID 1
G_G7 V++ VC 29 VMID 1
G_G8 V-- VC 29 VMID 1
L_L1 28 V++ 5.30532e-11
L_L2 30 V-- 5.30532e-11
L_L3 31 V++ 5.30532e-11
L_L4 32 V-- 5.30532e-11
R_R15 29 28 0.001
R_R16 30 29 0.001
R_R17 VC 31 0.001
R_R18 32 VC 0.001
* Second Pole Stage 40dB/dec
G_G9 V++ 33 VG VMID 0.0031415
G_G10 V-- 33 VG VMID 0.0031415
G_G11 V++ 34 33 VMID 0.0031415
G_G12 V-- 34 33 VMID 0.0031415
R_R19 33 V++ 318.319274232055
R_R20 V-- 33 318.319274232055
R_R21 34 V++ 318.319274232055
R_R22 V-- 34 318.319274232055
C_C6 33 V++ 10e-12
C_C7 V-- 33 10e-12
C_C8 34 V++ 10e-12
C_C9 V-- 34 10e-12
* Output Stage
D_D11 34 35 DX
D_D12 36 34 DX
D_D13 V-- 37 DY
D_D14 V++ 37 DX
D_D15 V++ 38 DX
D_D16 V-- 38 DY
G_G13 37 V-- VOUT 34 1.11e-2
G_G14 38 V-- 34 VOUT 1.11e-2
G_G15 VOUT V++ V++ 34 20e-3
G_G16 V-- VOUT 34 V-- 20e-3
V_V8 35 VOUT -.384
V_V9 VOUT 36 -.384
R_R23 VOUT V++ 50
R_R24 V-- VOUT 50
.model pj110_input pjf
+ vto=-1.4
+ beta=0.0025
+ lambda=0.03
+ is=2.68e-015
+ pb=0.73
+ cgd=8.6e-012
+ cgs=9.05e-012
+ fc=0.5 kf=0
+ af=1
+ tnom=35
.model NPN_CASCADE npn
+ is=5.02e-016
+ bf=150
+ va=300
+ ik=0.017
+ rb=0.01
+ re=0.011
+ rc=900
+ cje=2e-013
+ cjc=1.6e-028
+ kf=0
+ af=1
.model PJ110_CASCADE pjf
+ vto=-1.4
+ beta=0.000617
+ lambda=0.03
+ is=3.96e-016
+ pb=0.73
+ cgd=2.2e-012
+ cgs=3e-012
+ fc=0.5
+ kf=0
+ af=1
+ tnom=35
.model DBREAK d
+ bv=43
+ rs=1
.model PNP_MIRROR pnp
+ is=4e-015
+ bf=150
+ va=50
+ ik=0.138
+ rb=0.01
+ re=0.101
+ rc=180
+ cje=1.34e-012
+ cjc=4.4e-013
+ kf=0
+ af=1
.model DN D(KF=6.69e-12 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28110subckt
```

FIGURE 47. SPICE NET LIST

Characterization vs Simulation Results

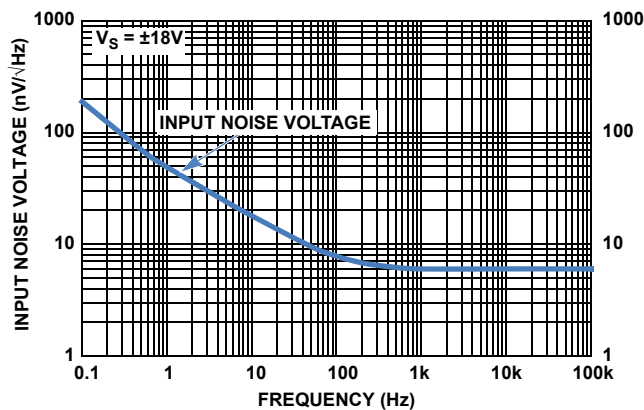


FIGURE 48. CHARACTERIZED INPUT NOISE VOLTAGE

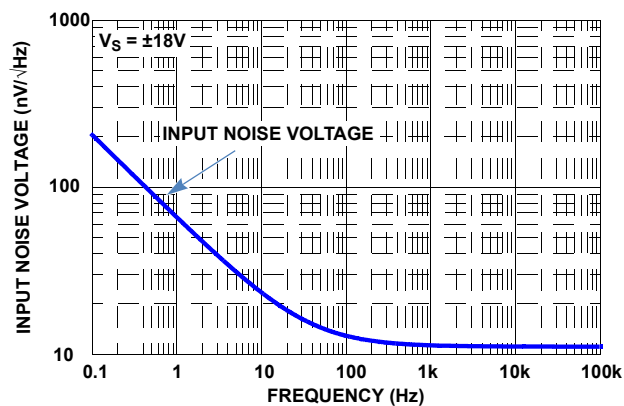


FIGURE 49. SIMULATED INPUT NOISE VOLTAGE

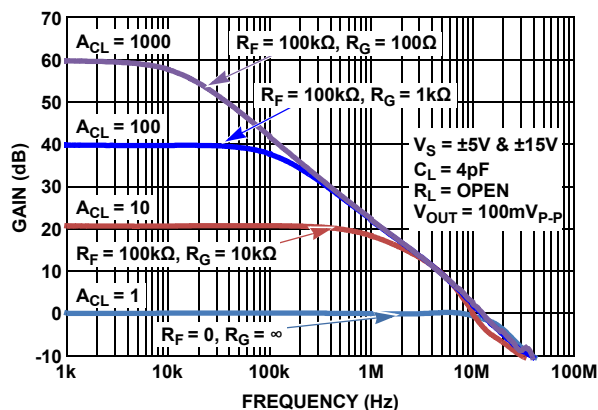


FIGURE 50. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

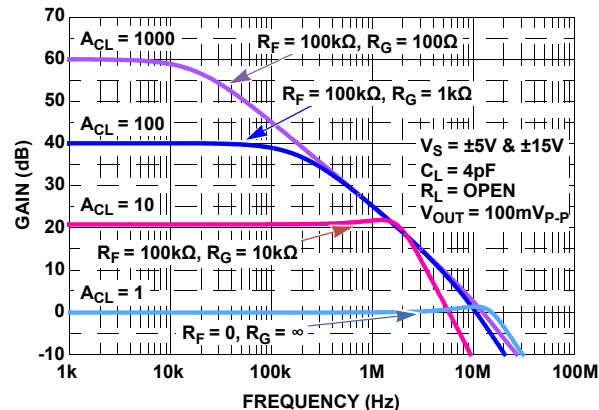
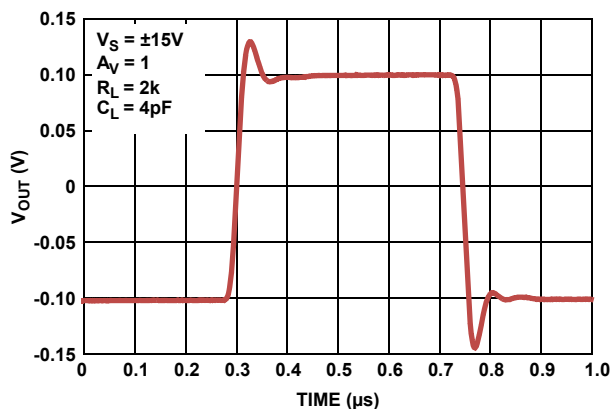
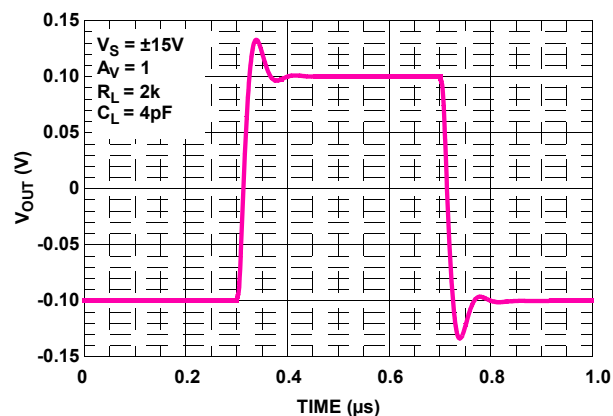


FIGURE 51. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

FIGURE 52. CHARACTERIZED SMALL SIGNAL TRANSIENT RESPONSE
vs R_L , $V_S = \pm 0.9V, \pm 2.5V$ FIGURE 53. SIMULATED SMALL SIGNAL TRANSIENT RESPONSE vs
 R_L , $V_S = \pm 0.9V, \pm 2.5V$

Characterization vs Simulation Results (Continued)

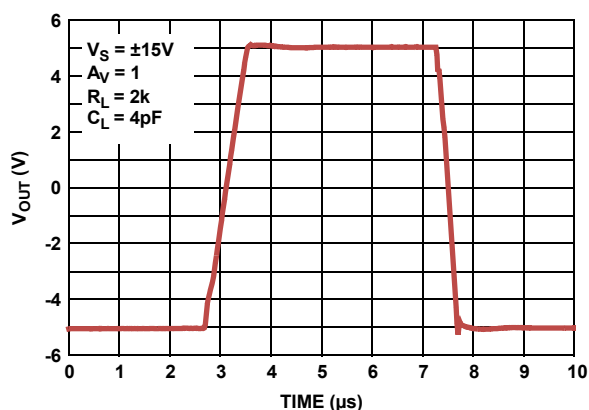


FIGURE 54. CHARACTERIZED LARGE SIGNAL TRANSIENT RESPONSE
vs R_L , $V_S = \pm 0.9V, \pm 2.5V$

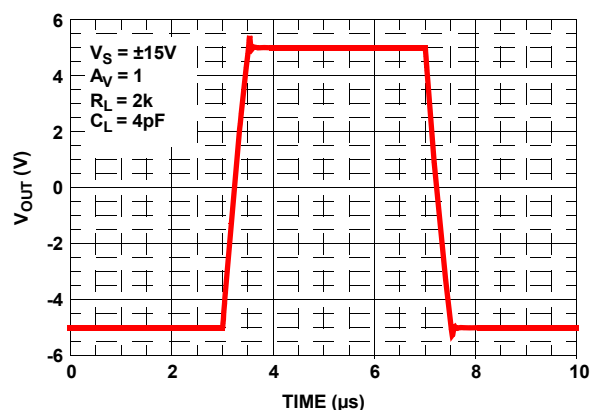


FIGURE 55. SIMULATED LARGE SIGNAL TRANSIENT RESPONSE vs
 R_L , $V_S = \pm 0.9V, \pm 2.5V$

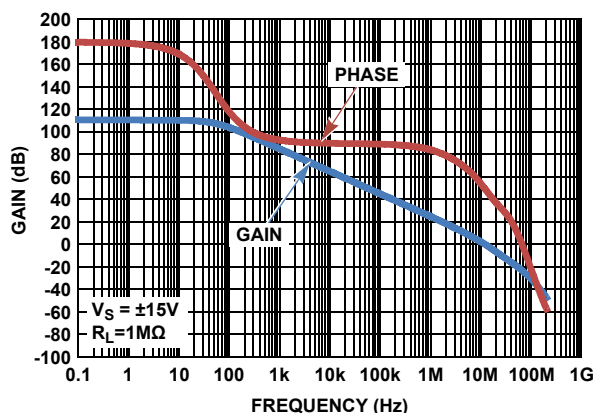


FIGURE 56. SIMULATED (DESIGN) OPEN-LOOP GAIN, PHASE vs
FREQUENCY

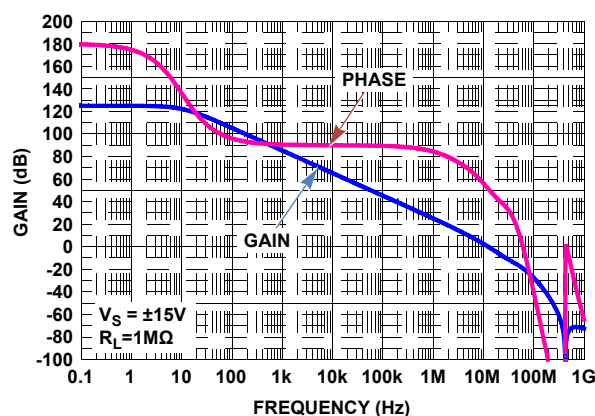


FIGURE 57. SIMULATED (SPICE) OPEN-LOOP GAIN, PHASE vs
FREQUENCY

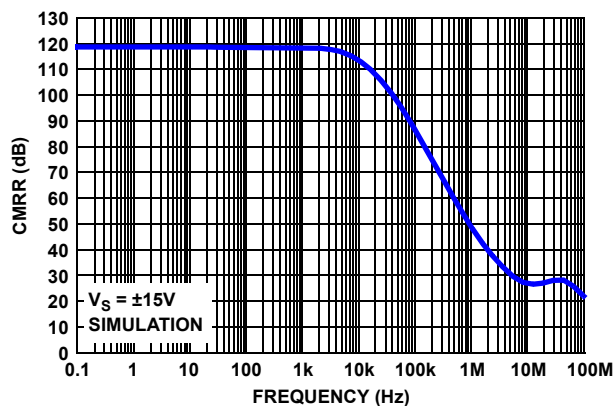


FIGURE 58. SIMULATED (DESIGN) CMRR

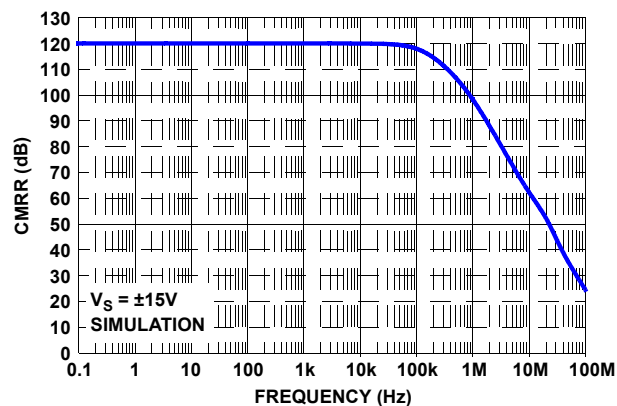
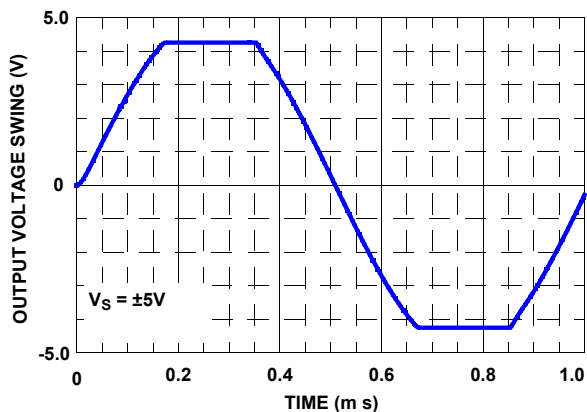
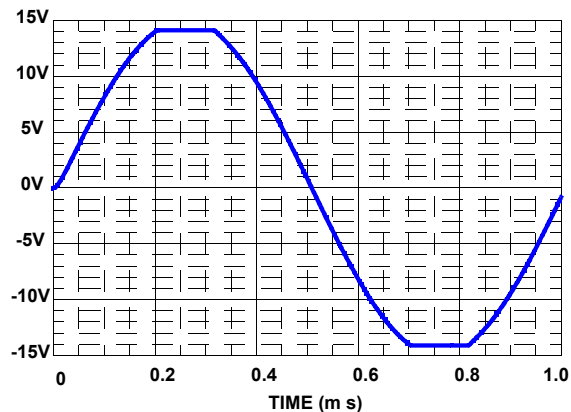


FIGURE 59. SIMULATED (SPICE) CMRR

Characterization vs Simulation Results (Continued)

FIGURE 60. SIMULATED OUTPUT VOLTAGE SWING $\pm 5V$ FIGURE 61. SIMULATED OUTPUT VOLTAGE SWING $\pm 15V$

© Copyright Intersil Americas LLC 2010-2012. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
8/31/12	FN6639.3	Removed from ordering info MSOP parts ISL28110FUBZ, ISL28110FUZ on page 3. Removed all instances of MSOP throughout document (front page, thermal information, pin descriptions and POD)
8/30/12		Added "No Phase Reversal" to Features on page 1 Removed from ordering info TDFN parts ISL28110FRTZ, ISL28210FRTZ, ISL28110FRTBZ, ISL28210FRTBZ, ISL28110FBBZ, ISL28210FBBZ on page 3. Figure 47 on page 18 Spice Net List changed -40 to -12 in Input Stage C_CinDif, C_Cin1 and C_Cin2 Removed all instances of TDFN throughout document (front page, thermal information, pin descriptions and POD)
7/14/11	FN6639.2	Converted to new datasheet template. Page 1 Added "Related Literature" and "AN1594: ISL28210SOICEVAL1Z Evaluation Board User's Guide" Page 3 Ordering Information table: Added ISL28210SOICEVAL1Z Evaluation Board
11/29/10	FN6639.1	Removed label on right side of characterization curve, Figure 48 (Input Noise Current).
11/23/10		Page 1 Updated Trademark statement Page 3 Ordering Information: Removed "coming soon" from ISL28110FBZ Page 4 Electrical Specifications: Added ISL28110 IB and IOS specs @ VS=±5V. Page 5 Electrical Specifications: Changed AVOL limits from V/mV to dB Page 5 Electrical Specifications, Dynamic Performance, Slew Rate: Added "4V Step" to conditions; changed TYP limit from 23V/μs to 20V/μs Page 6 Electrical Specifications, Dynamic Performance, Slew Rate: Added "10V Step" to conditions; changed TYP limit from 23V/μs to 20V/μs Page 6 Electrical Specifications: Added ISL28110 IB and IOS specs @ VS= ±15V. Changed AVOL limits from V/mV to dB. Changed ts, settling time to 0.1% from 0.9μs to 1.3μs and changed ts, settling time to 0.01% from 1.2μs to 1.6μs. Page 7 Replaced Elect Spec table Notes 8 & 9 (Note 8 "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested./Note 9 Limits established by characterization and are not production tested.") With: "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." Page 8 Characteristic Curves: Added ISL28110 IB vs Temperature (Fig 4) Page 8 Characteristic Curves: Added ISL28110 IOS vs Temperature (Fig 6) Pages 17-21: Added PSPICE model section
9/13/10	FN6639.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

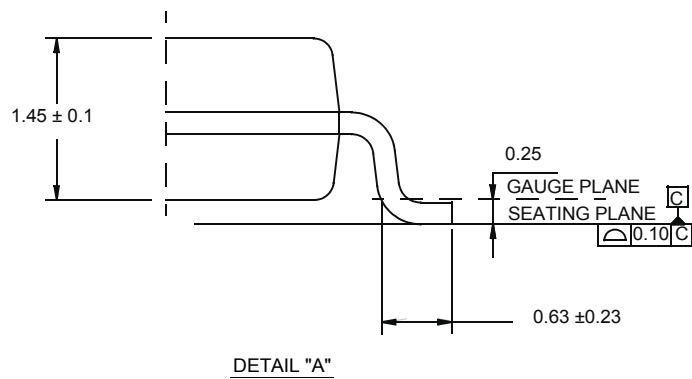
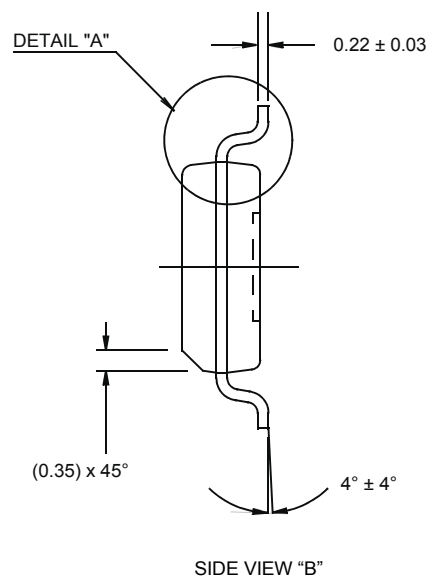
For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: [ISL28110, ISL28210](#)

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: <http://rel.intersil.com/reports/search.php>

M8.15E

Rev 0, 08/09



1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.