

**DAC124S085 12-Bit Quad, DAC104S085 10-Bit Quad,  
DAC084S085 8-Bit Quad, DAC122S085 12-Bit Dual,  
DAC102S085 10-Bit Dual, DAC082S085 8-Bit Dual**

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## 1.0 Introduction

The DAC124S085EB Design Kit (consisting of the DAC124S085 Evaluation Board and this User's Guide) is designed to ease evaluation and design-in of the National Semiconductor DAC124S085 12-Bit Quad, DAC104S085 10-Bit Quad, DAC084S085 8-Bit Quad, DAC122S085 12-Bit Dual, DAC102S085 10-Bit Dual, DAC082S085 8-Bit Dual Micro-Power Digital-to-Analog Converter with Rail-to-Rail Output. This family of pin-

compatible DACs, will be referenced throughout this document as the DAC124S085.

The evaluation board can be used with suitable test equipment, such as a pattern generator and signal analyzer, to evaluate the DAC124S085 performance.

Data transmitted to the DAC124S085 via a serial interface is converted to an analog waveform by U2/U4, the DAC124S085.

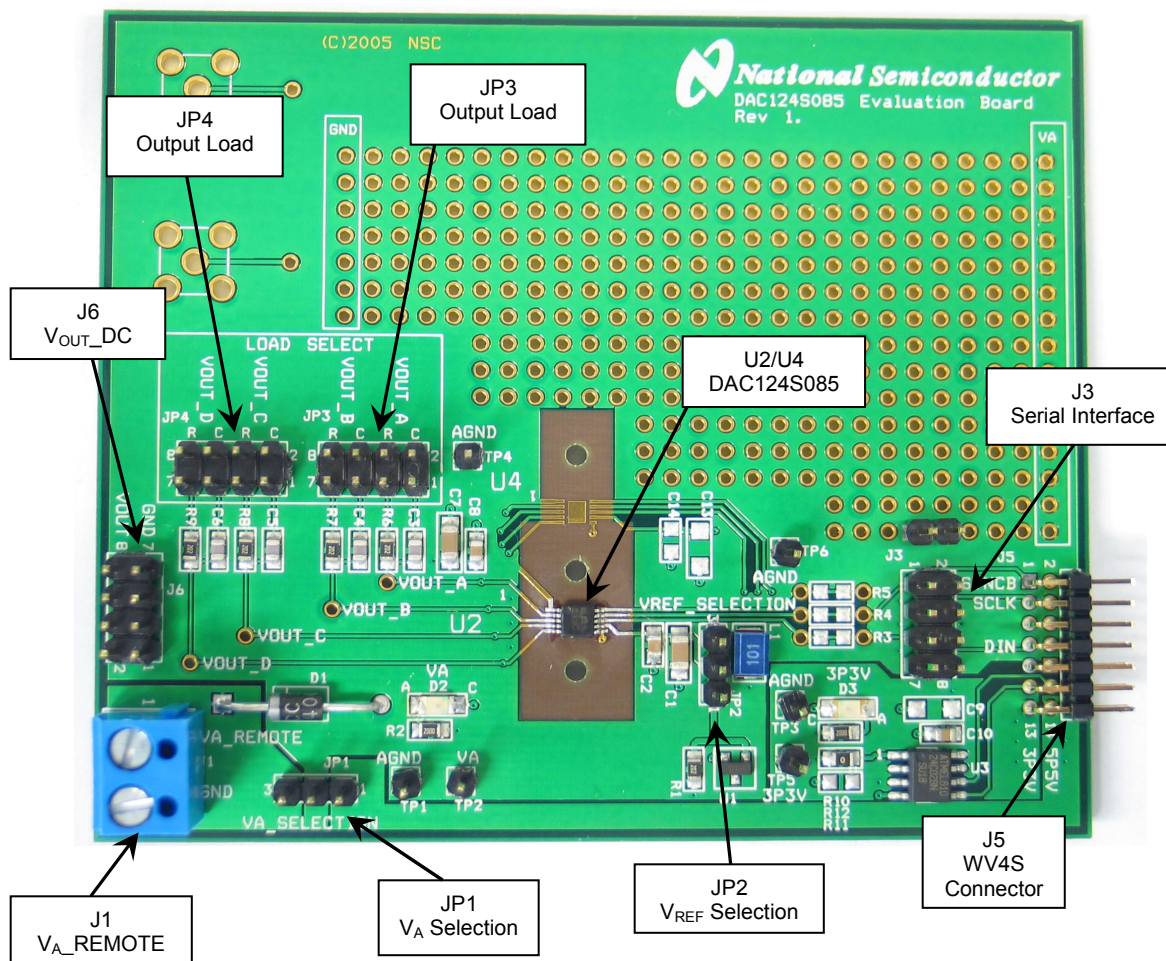


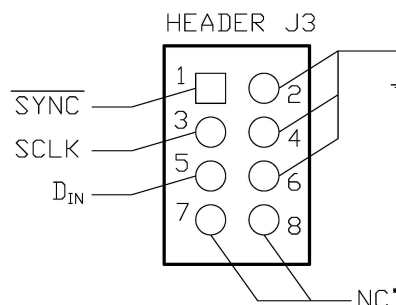
Figure 1: Component and Test Point Location

The DAC124S085 evaluation board comes fully assembled and ready for use. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement, and to *Figure 6* for the Evaluation Board schematic.

The DAC124S085 evaluation board may be used in the Stand-Alone mode while a Pattern Generator is used to drive the DAC124S085, and a Signal Analyzer is used to evaluate the analog output signal

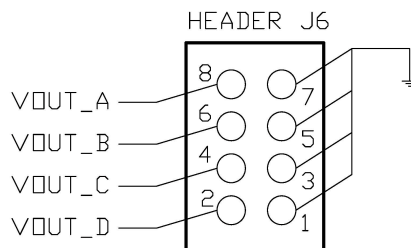
Refer to *Figure 1* for locations of test points and major components.

4. Connect your Pattern Generator to Serial Interface header J3. Refer to *Figure 3* below for connection details.



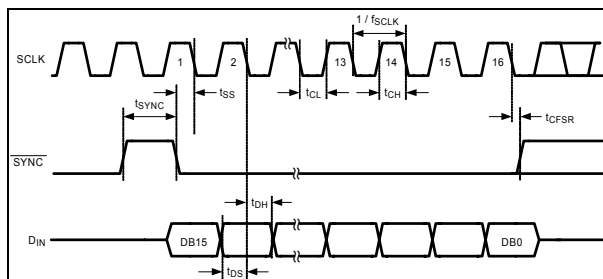
**Figure 3: J3 Serial Interface Header**  
*(\*Pins 7&8 are used for SCL and SDA, respectively, when modified for WV4.0)*

5. The Analog Output signals of each channel can be seen DC coupled at header J6. See the header schematic of *Figure 4* for details.

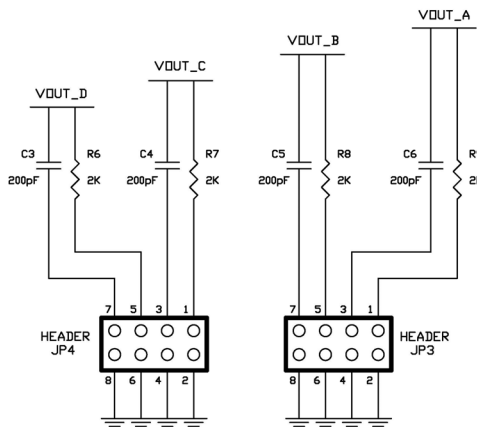


### Figure 4: J6 Output Header

6. Select the desired output load by adding jumpers to headers JP3 & JP4. See *Figure 5* and *Table 1* in Section 4.0 for jumper configurations.



**Figure 2: Digital Input Timing Diagram**  
(Refer to Appendix 2.0 for an enlarged version)



**Figure 5: JP3 & JP4 Load Select Headers**

## 4.0 Functional Description

Table 1 describes the function of the various jumpers on the DAC124S085 evaluation board. The Evaluation Board schematic is shown in *Figure 6*.

| Jumper | Pins 1 & 2                      | Pins 2 & 3                    |
|--------|---------------------------------|-------------------------------|
| JP1    | Select VA=5.5V from WV4.1 Board | Select VA_REMOTE from J1      |
| JP2    | Select 2.5V as V <sub>REF</sub> | Select VA as V <sub>REF</sub> |

| Pin   | JP3                                         | JP4                                         |
|-------|---------------------------------------------|---------------------------------------------|
| 1 & 2 | Select 200pF Output Load Capacitance VOUT_A | Select 200pF Output Load Capacitance VOUT_C |
| 3 & 4 | Select 2kΩ Output Load Resistance VOUT_A    | Select 2kΩ Output Load Resistance VOUT_C    |
| 5 & 6 | Select 200pF Output Load Capacitance VOUT_B | Select 200pF Output Load Capacitance VOUT_D |
| 7 & 8 | Select 2kΩ Output Load Resistance VOUT_B    | Select 2kΩ Output Load Resistance VOUT_D    |

**Table 1: Jumper Configurations**

### 4.1 Serial Interface

*In Stand-Alone Mode*, the serial interface must be driven by an external device. The three-wire interface (SCLK, SYNC, D<sub>IN</sub>) is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the Timing Diagram (*Figure 2*) for information on a write sequence.

The maximum digital input level of the three-wire interface is independent of the analog supply voltage (V<sub>A</sub>). The range of all digital inputs is 0V to 5.25V regardless of V<sub>A</sub>.

A write sequence begins by bringing the SYNC line low. Once SYNC is low, the *Binary* data on the D<sub>IN</sub> line is clocked into the 16-bit serial input register on the falling edges of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. At this point the

SYNC line may be kept low or brought high. In either case, it must be brought high for the minimum specified time before the next write sequence as a falling edge of SYNC will initiate the next write cycle.

Since the SYNC and D<sub>IN</sub> buffers draw more current when they are high, they should be idled low between write sequences to minimize power consumption.

Please refer to the DAC124S085 datasheet for more information.

### 4.2 DAC Reference Circuitry

The reference voltage for the DAC124S085 is selected by JP2. (See Table 1 for details.) The reference can either be selected as a fixed 2.5 volts, or as the supply voltage. In the latter case, the analog output range of the DAC124S085 can be scaled by adjusting the supply voltage (V<sub>A</sub>). This voltage can be set anywhere from +2.7V to +5.5V.

### 4.3 Analog Output

The analog output of this Eval board is available DC coupled at the header J6. An AC coupled output is not provided, however SMA footprints are available at J2 and J4. These footprints can be used along with the prototype field to design another output circuit, should it be desired.

### 4.4 Power Supply Connections

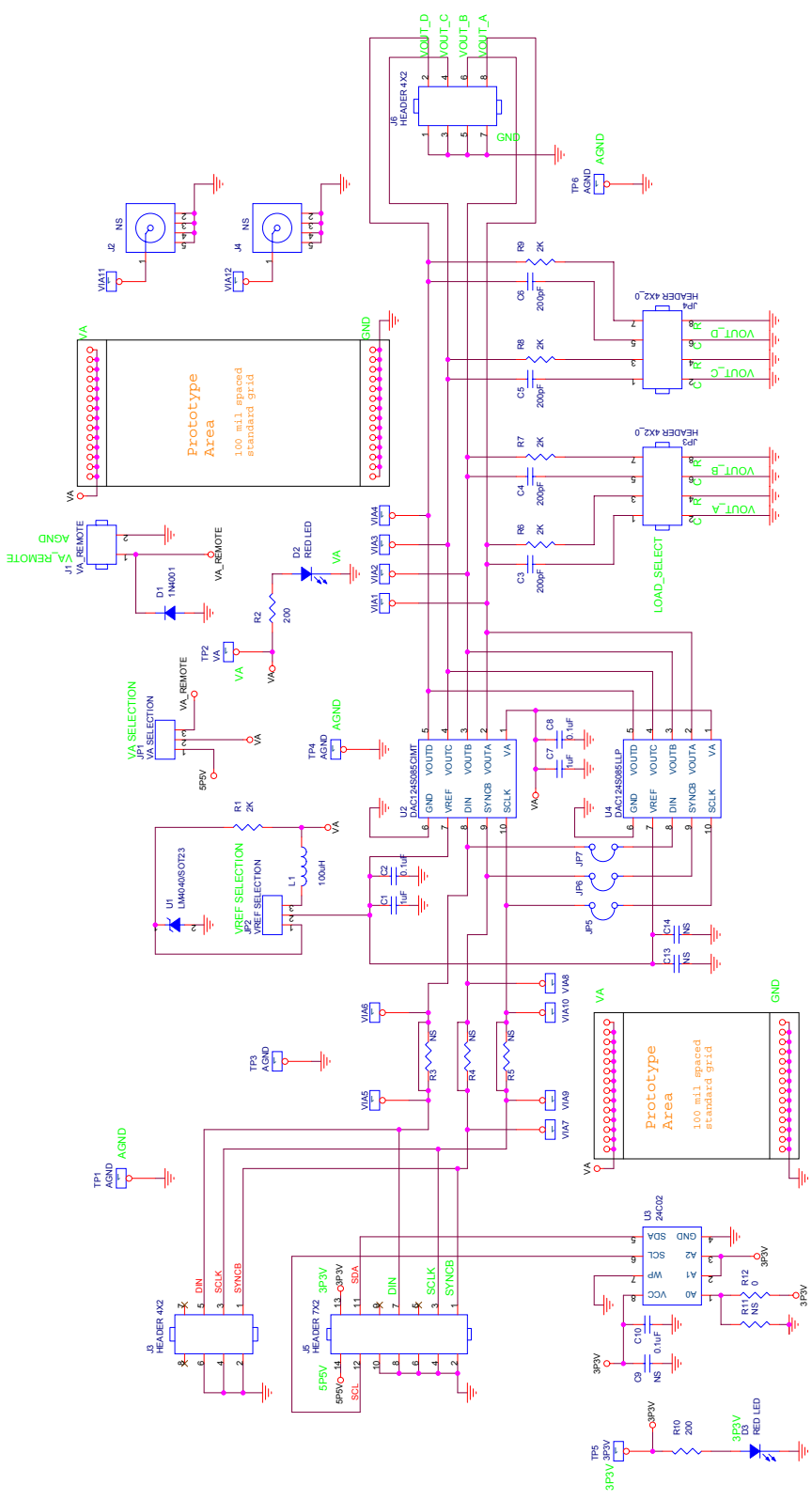
In Stand-alone mode, the DAC124S085 board must be powered by an external supply.

Connect a DC voltage supply to connector J1 and place a jumper across pins 2 and 3 of JP1 to select V<sub>A\_REMOTE</sub>. This voltage (V<sub>A</sub>) can be set anywhere from +2.7V to +5.5V.

If the supply voltage (V<sub>A</sub>) serves as the reference for the DAC124S085, ensure a clean power supply is used.

## 6.0 Evaluation Board Specifications

|                      |                                    |                  |
|----------------------|------------------------------------|------------------|
| Board Size:          | 3.70" x 3.15" (9.4 cm x 8 cm)      |                  |
| Power Requirements   | Min: +2.7V, 3mA                    | Max: +5.5V, 5 mA |
| Max Clock Frequency: | 40 MHz                             |                  |
| Analog Output        |                                    |                  |
| Impedance:           | User Selectable: 2KΩ, 200pF, or ∞. |                  |





# APPENDIX

## A1.0 Summary Tables of Test Points, Jumpers, and Connectors

### Test Points on the DAC124S085 Evaluation Board

|           |                                                                    |
|-----------|--------------------------------------------------------------------|
| TP1: AGND | Ground. Located at the lower left of the board.                    |
| TP2: VA   | V <sub>A</sub> Test Point. Located in the lower left of the board. |
| TP3: AGND | Ground. Located at the lower right of the board.                   |
| TP4: AGND | Ground. Located in the center of the board                         |
| TP5: 3P3V | 3.3V test point. Located at the lower right edge of the board.     |
| TP6: AGND | Ground. Located in the center of the board.                        |

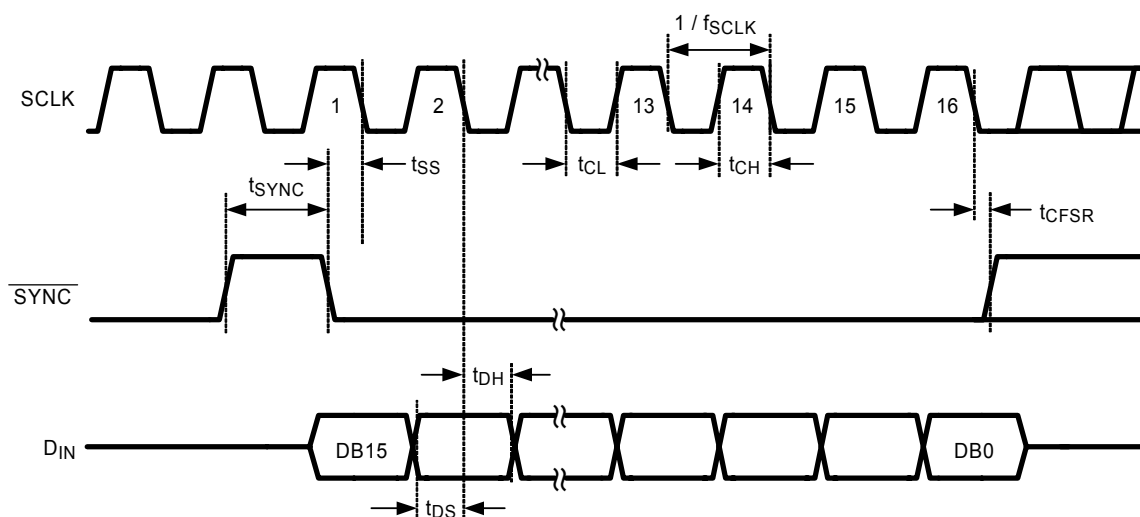
### Connectors on the DAC124S085 Evaluation Board

|                             |                                                                                            |
|-----------------------------|--------------------------------------------------------------------------------------------|
| J1: Terminal Block          | VA_REMOTE. External power supply connector.                                                |
| J2: SMA Footprint           | Not Used                                                                                   |
| J3: Serial Interface Header | Serial Interface connector. Logic Input. (Refer to <i>Figure 3</i> for a pin-out diagram.) |
| J4: SMA Footprint           | Not Used                                                                                   |
| J5: WV4.1 Connector         | WaveVision 4.1 connector (for future use)                                                  |
| J6: Output Header           | DC Coupled output for channels A-D                                                         |

### Selection Jumpers on the DAC124S085 Evaluation Board (Refer to *Table 1* in Section 4.0 for configuration details)

|                   |                                               |
|-------------------|-----------------------------------------------|
| JP1: VA_SELECTION | Selects source of V <sub>A</sub> .            |
| JP2: VREF_SELECT  | Selects V <sub>REF</sub> Level                |
| JP3: LOAD SELECT  | Configures the output load for channels A & B |
| JP4: LOAD SELECT  | Configures the output load for channels C & D |

## A2.0 Enlarged Timing Diagram



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