

# The RF MOSFET Line

## RF Power Field Effect Transistors

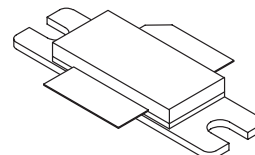
### N-Channel Enhancement-Mode Lateral MOSFETs

**MRF18060A**  
**MRF18060AS**

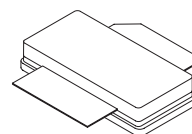
Designed for PCN and PCS base station applications from frequencies up to 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for PCN-PCS/cellular radio and WLL applications. Specified for GSM1805 – 1880 MHz.

- Typical GSM Performance, Full Frequency Band (1805 – 1880 MHz)  
Power Gain — 13 dB (Typ) @ 60 Watts  
Efficiency — 45% (Typ) @ 60 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts (CW) Output Power
- Excellent Thermal Stability

**60 W, 1.80 – 1.88 GHz, 26 V**  
**LATERAL N-CHANNEL**  
**BROADBAND**  
**RF POWER MOSFETs**



**CASE 465-04, STYLE 1**  
**(MRF18060A)**



**CASE 465A-04, STYLE 1**  
**(MRF18060AS)**

#### MAXIMUM RATINGS

| Rating                                                                                    | Symbol    | Value       | Unit                         |
|-------------------------------------------------------------------------------------------|-----------|-------------|------------------------------|
| Drain-Source Voltage                                                                      | $V_{DSS}$ | 65          | Vdc                          |
| Gate-Source Voltage                                                                       | $V_{GS}$  | +15, -0.5   | Vdc                          |
| Total Device Dissipation @ $T_C \geq 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$     | 180<br>1.03 | Watts<br>W/ $^\circ\text{C}$ |
| Storage Temperature Range                                                                 | $T_{stg}$ | -65 to +150 | $^\circ\text{C}$             |
| Operating Junction Temperature                                                            | $T_J$     | 200         | $^\circ\text{C}$             |

#### ESD PROTECTION CHARACTERISTICS

| Test Conditions  | Class        |
|------------------|--------------|
| Human Body Model | 2 (Typical)  |
| Machine Model    | M3 (Typical) |

#### THERMAL CHARACTERISTICS

| Characteristic                       | Symbol          | Max  | Unit               |
|--------------------------------------|-----------------|------|--------------------|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 0.97 | $^\circ\text{C/W}$ |

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

**OFF CHARACTERISTICS**

|                                                                                                 |               |    |   |   |                 |
|-------------------------------------------------------------------------------------------------|---------------|----|---|---|-----------------|
| Drain–Source Breakdown Voltage<br>( $V_{GS} = 0\text{ Vdc}$ , $I_D = 10\text{ }\mu\text{Adc}$ ) | $V_{(BR)DSS}$ | 65 | — | — | Vdc             |
| Zero Gate Voltage Drain Current<br>( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0$ )                  | $I_{DSS}$     | —  | — | 6 | $\mu\text{Adc}$ |
| Gate–Source Leakage Current<br>( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0$ )                       | $I_{GSS}$     | —  | — | 1 | $\mu\text{Adc}$ |

**ON CHARACTERISTICS**

|                                                                                           |              |     |      |     |     |
|-------------------------------------------------------------------------------------------|--------------|-----|------|-----|-----|
| Gate Threshold Voltage<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 300\text{ }\mu\text{Adc}$ ) | $V_{GS(th)}$ | 2   | —    | 4   | Vdc |
| Gate Quiescent Voltage<br>( $V_{DS} = 26\text{ Vdc}$ , $I_D = 500\text{ mAdc}$ )          | $V_{GS(Q)}$  | 2.5 | 3.9  | 4.5 | Vdc |
| Drain–Source On–Voltage<br>( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2\text{ Adc}$ )            | $V_{DS(on)}$ | —   | 0.27 | —   | Vdc |
| Forward Transconductance<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 2\text{ Adc}$ )           | $g_{fs}$     | —   | 4.7  | —   | S   |

**DYNAMIC CHARACTERISTICS**

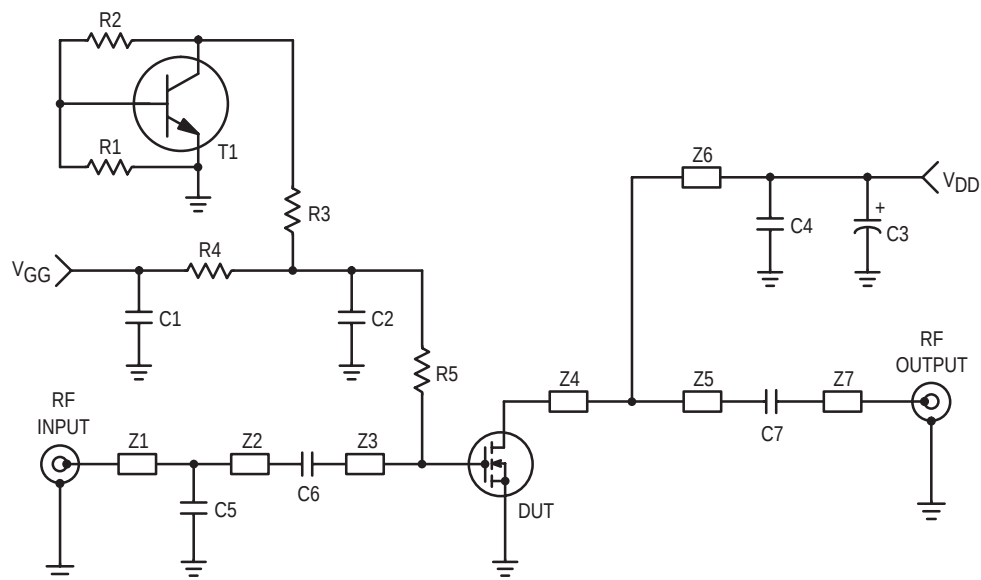
|                                                                                                                                           |           |   |     |   |    |
|-------------------------------------------------------------------------------------------------------------------------------------------|-----------|---|-----|---|----|
| Input Capacitance (Including Input Matching Capacitor in Package) (1)<br>( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ ) | $C_{iss}$ | — | 160 | — | pF |
| Output Capacitance (1)<br>( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )                                                | $C_{oss}$ | — | 740 | — | pF |
| Reverse Transfer Capacitance<br>( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$ )                                          | $C_{rss}$ | — | 2.7 | — | pF |

**FUNCTIONAL TESTS** (In Motorola Test Fixture)

|                                                                                                                                                                      |          |                                                         |    |   |    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|---------------------------------------------------------|----|---|----|
| Common–Source Amplifier Power Gain @ 60 W (2)<br>( $V_{DD} = 26\text{ Vdc}$ , $I_{DQ} = 500\text{ mA}$ , $f = 1805 - 1880\text{ MHz}$ )                              | $G_{ps}$ | 11.5                                                    | 13 | — | dB |
| Drain Efficiency @ 60 W (2)<br>( $V_{DD} = 26\text{ Vdc}$ , $I_{DQ} = 500\text{ mA}$ , $f = 1805 - 1880\text{ MHz}$ )                                                | $\eta$   | 43                                                      | 45 | — | %  |
| Input Return Loss (2)<br>( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 60\text{ W CW}$ , $I_{DQ} = 500\text{ mA}$ ,<br>$f = 1805 - 1880\text{ MHz}$ )                      | IRL      | 10                                                      | —  | — | dB |
| Output Mismatch Stress<br>( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 60\text{ W CW}$ , $I_{DQ} = 500\text{ mA}$ VSWR = 10:1,<br>All Phase Angles at Frequency of Tests) | $\Psi$   | No Degradation In Output Power<br>Before and After Test |    |   |    |

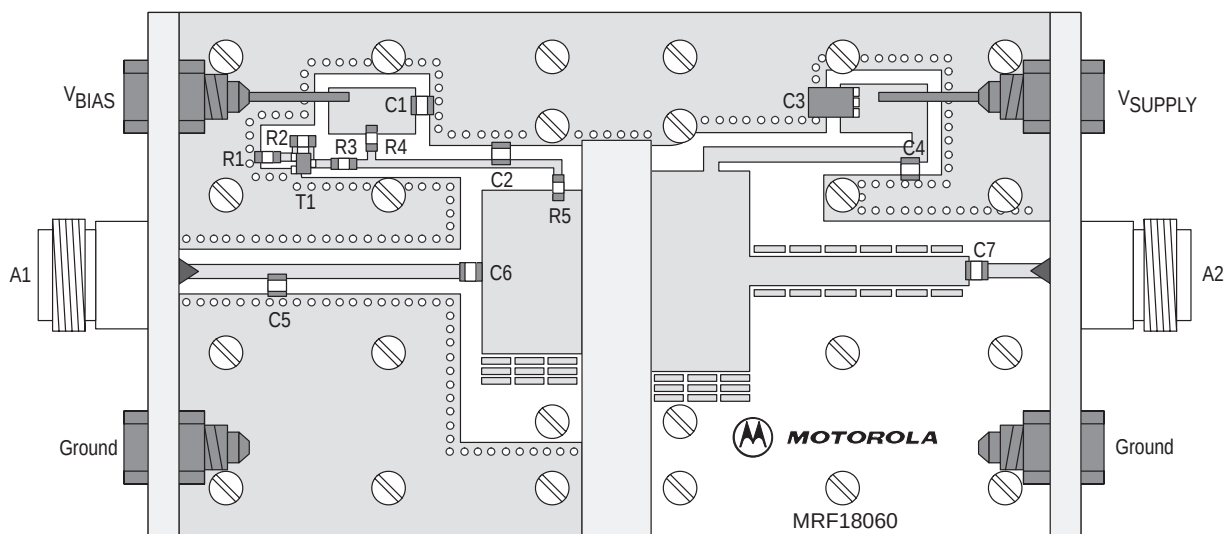
(1) Part is internally matched both on input and output.

(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.



|            |                                             |          |                               |
|------------|---------------------------------------------|----------|-------------------------------|
| C1         | 100 nF, Chip Capacitor 1203                 | R1, R3   | 2.2 kΩ, Chip Resistor 0805    |
| C2, C4, C7 | 10 pF, Chip Capacitor                       | R2, R4   | 2.7 kΩ, Chip Resistor 0805    |
| C3         | 10 μF, 35 V Electrolytic Tantalum Capacitor | R5       | 1.1 kΩ, Chip Resistor 0805    |
| C5         | 1.2 pF, Chip Capacitor                      | T1       | BC847 Transistor SOT-23       |
| C6         | 1.0 pF, Chip Capacitor                      | Z1 to Z7 | Microstrip Transmission Lines |

**Figure 1. 1805 – 1880 MHz Test Fixture Schematic**



**Figure 2. 1805 – 1880 MHz Test Fixture Component Layout**

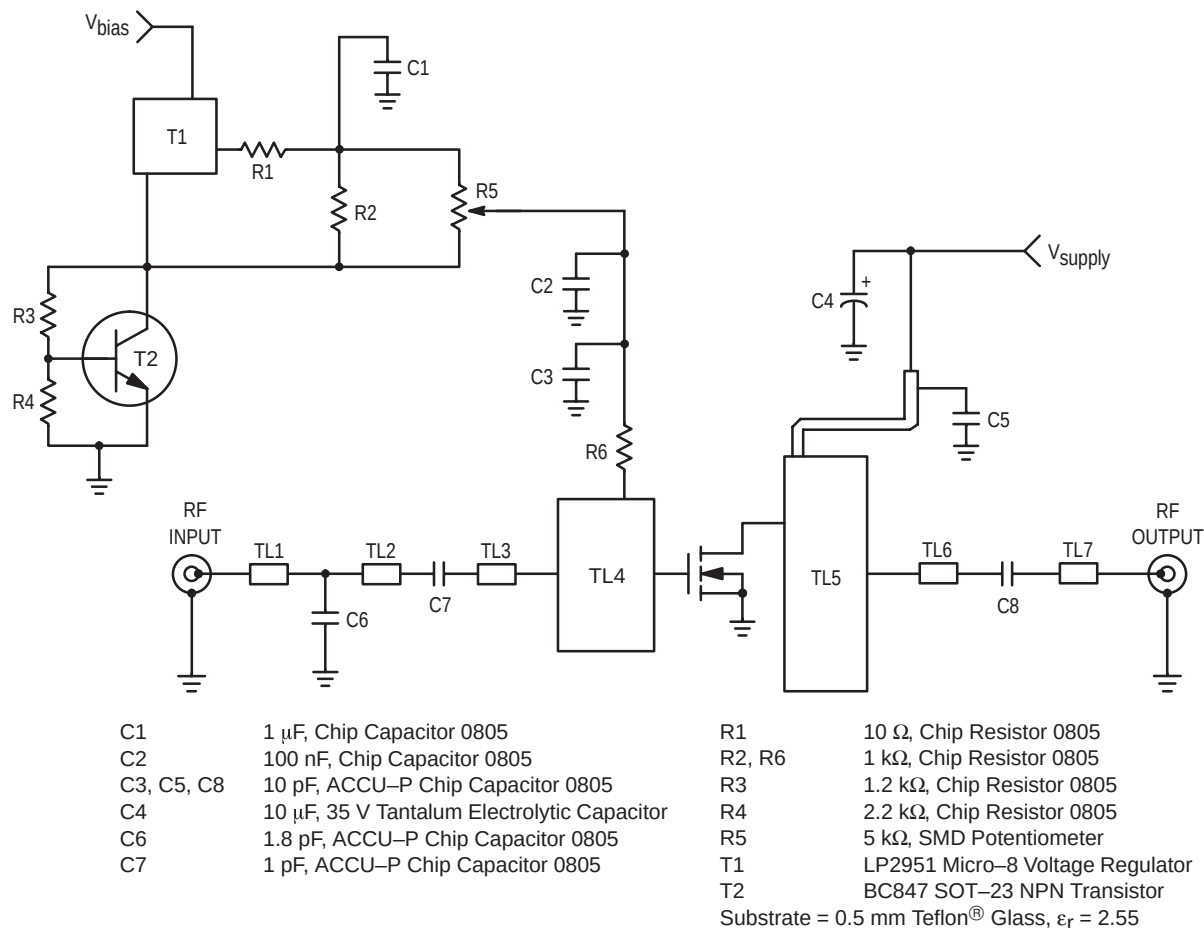


Figure 3. 1800 – 2000 MHz Demo Board Schematic

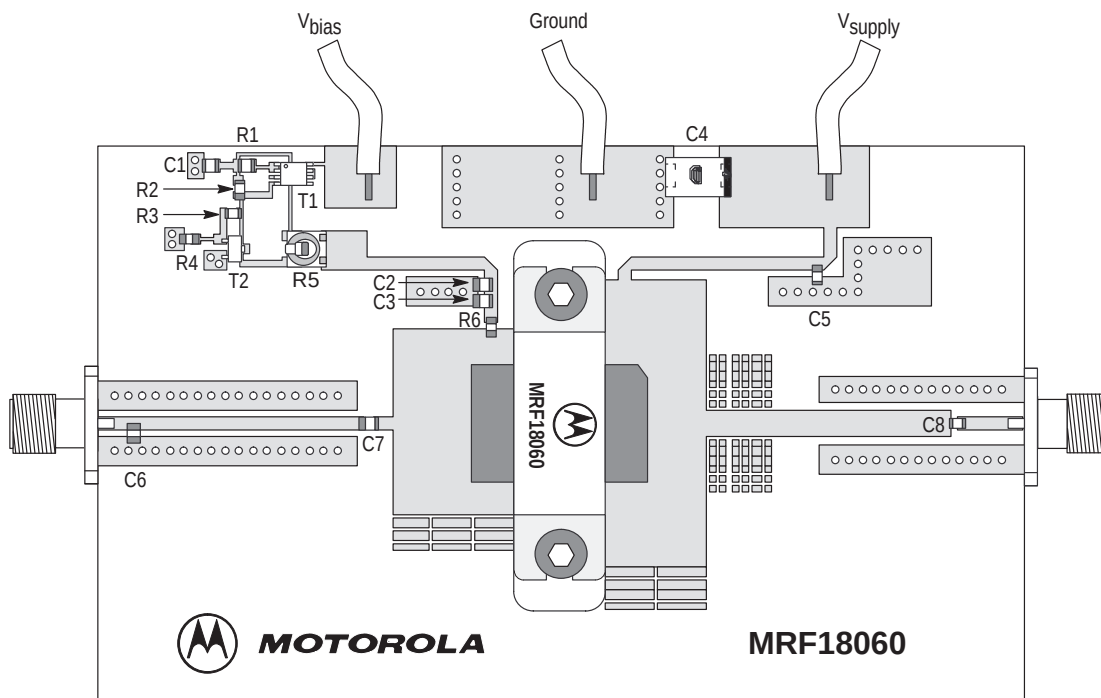


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

$V_{DD} = 26 \text{ V}$ ,  $I_{DQ} = 500 \text{ mA}$ ,  $P_{out} = 60 \text{ Watts (CW)}$

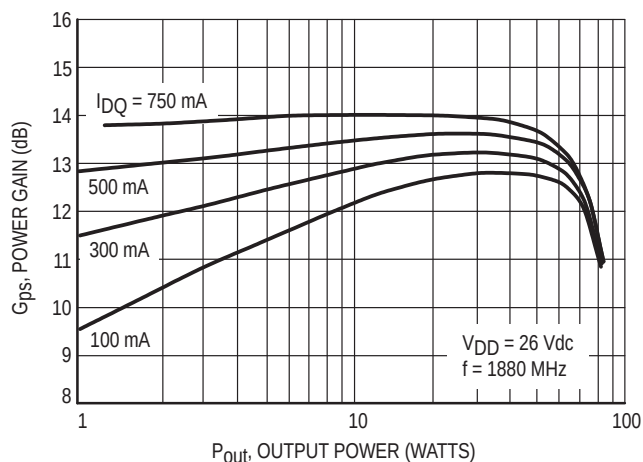
| <b>f<br/>MHz</b> | <b><math>Z_{in}</math><br/><math>\Omega</math></b> | <b><math>Z_{OL}^*</math><br/><math>\Omega</math></b> |
|------------------|----------------------------------------------------|------------------------------------------------------|
| 1700             | $0.60 + j2.53$                                     | $2.27 + j3.44$                                       |
| 1800             | $0.80 + j3.20$                                     | $2.05 + j3.05$                                       |
| 1900             | $0.92 + j3.42$                                     | $1.90 + j2.90$                                       |
| 2000             | $1.07 + j3.59$                                     | $1.64 + j2.88$                                       |
| 2100             | $1.31 + j4.00$                                     | $1.29 + j2.99$                                       |

$Z_{in}$  = Complex conjugate of source impedance.

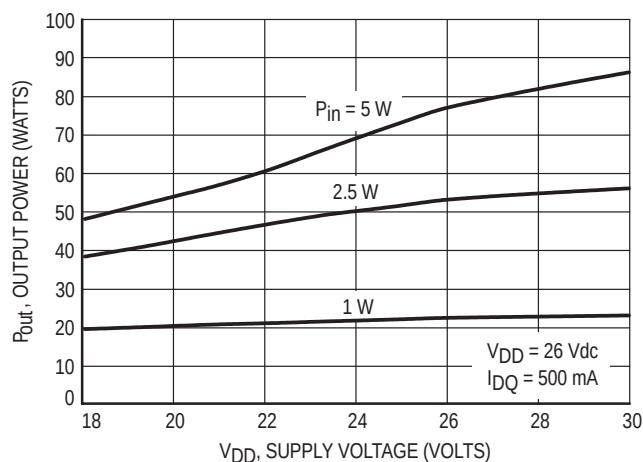
$Z_{OL}^*$  = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

**Table 1. Series Equivalent Input and Output Impedance**

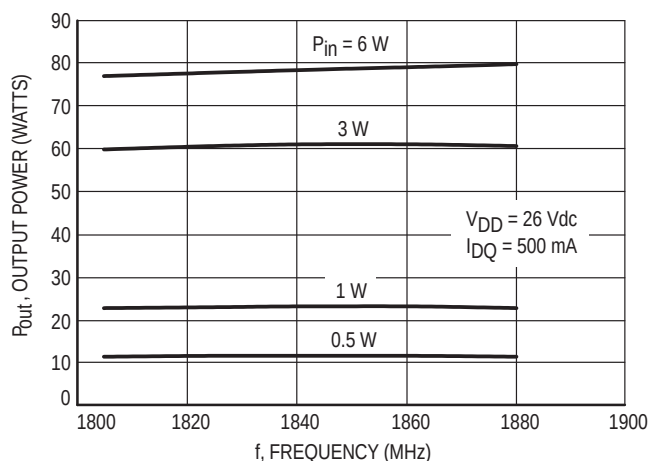
# TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)



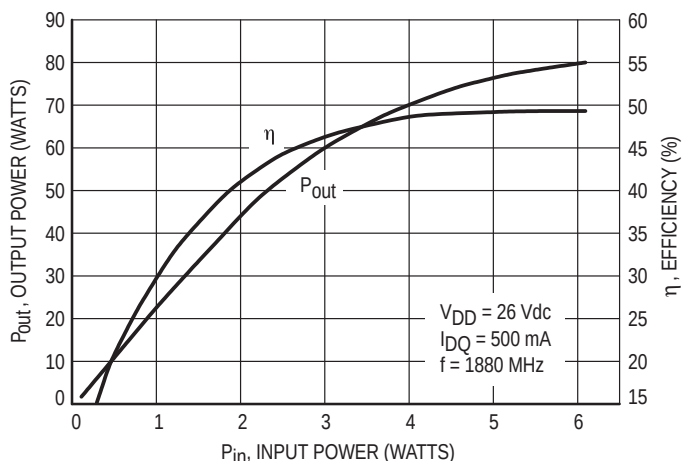
**Figure 5. Power Gain versus Output Power**



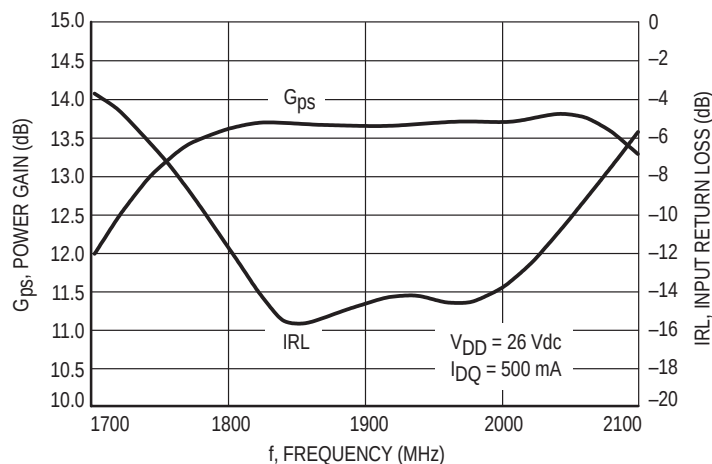
**Figure 6. Output Power versus Supply Voltage**



**Figure 7. Output Power versus Frequency**

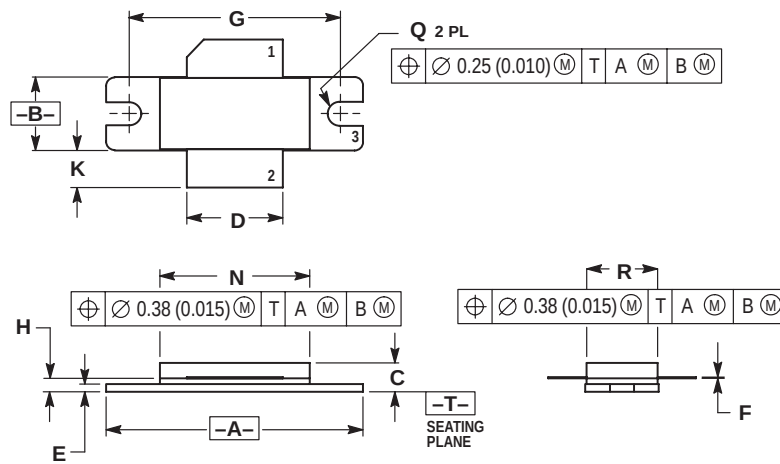


**Figure 8. Output Power and Efficiency versus Input Power**



**Figure 9. Wideband Gain and IRL (at Small Signal)**

## PACKAGE DIMENSIONS

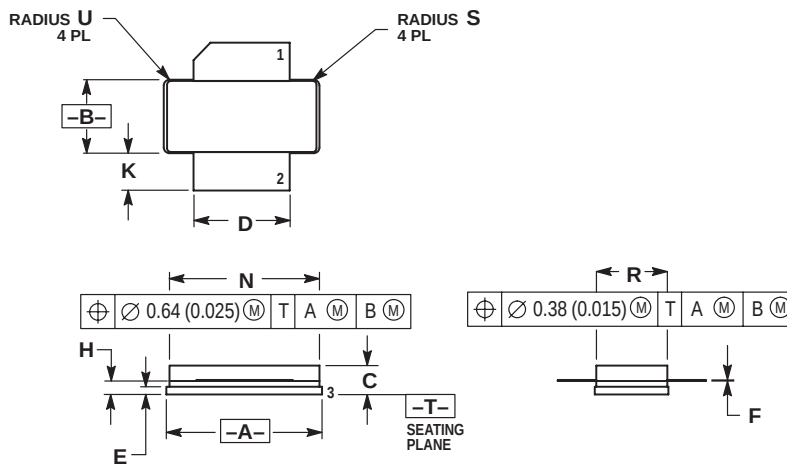


**CASE 465-04  
ISSUE D  
(MRF18060A)**

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 465-01, -02 AND -03 OBSOLETE, NEW STANDARD 465-04.
  4. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.335     | 1.345 | 33.91       | 34.16 |
| B   | 0.380     | 0.390 | 9.65        | 9.91  |
| C   | 0.125     | 0.170 | 3.18        | 4.32  |
| D   | 0.495     | 0.505 | 12.57       | 12.83 |
| E   | 0.035     | 0.045 | 0.89        | 1.14  |
| F   | 0.003     | 0.006 | 0.08        | 0.15  |
| G   | 1.100 BSC |       | 27.94 BSC   |       |
| H   | 0.055     | 0.065 | 1.40        | 1.65  |
| K   | 0.170     | 0.210 | 4.32        | 5.33  |
| N   | 0.772     | 0.788 | 19.60       | 20.00 |
| Q   | 0.118     | 0.138 | 3.00        | 3.51  |
| R   | 0.365     | 0.375 | 9.27        | 9.53  |

- STYLE 1:
- PIN 1. DRAIN
  - GATE
  - SOURCE



**CASE 465A-04  
ISSUE D  
(MRF18060AS)**

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.805     | 0.815 | 20.45       | 20.70 |
| B   | 0.380     | 0.390 | 9.65        | 9.91  |
| C   | 0.125     | 0.170 | 3.18        | 4.32  |
| D   | 0.495     | 0.505 | 12.57       | 12.83 |
| E   | 0.035     | 0.045 | 0.89        | 1.14  |
| F   | 0.003     | 0.006 | 0.08        | 0.15  |
| H   | 0.055     | 0.065 | 1.40        | 1.65  |
| K   | 0.170     | 0.210 | 4.32        | 5.33  |
| N   | 0.775     | 0.785 | 19.69       | 19.94 |
| R   | 0.365     | 0.375 | 9.27        | 9.53  |
| S   | 0.020 REF |       | 0.51 REF    |       |
| U   | 0.030 REF |       | 0.76 REF    |       |

- STYLE 1:
- PIN 1. DRAIN
  - GATE
  - SOURCE

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