

74HC374; 74HCT374

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 6 — 5 August 2024

Product data sheet

1. General description

The 74HC374; 74HCT374 is an octal positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable (\overline{OE}) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
 - For 74HC374: CMOS level
 - For 74HCT374: TTL level
- Octal bus interface
- Non-inverting 3-state outputs
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Complies with JEDEC standards
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC374D 74HCT374D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC374PW 74HCT374PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

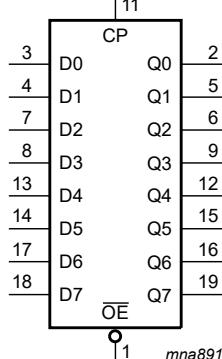


Fig. 1. Logic symbol

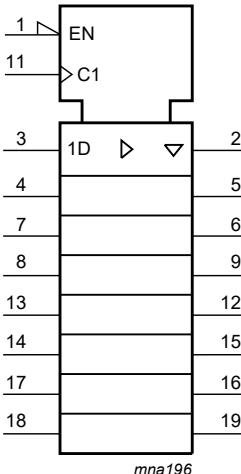


Fig. 2. IEC logic symbol

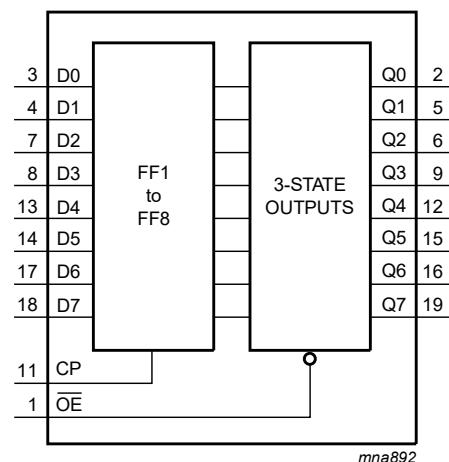


Fig. 3. Functional diagram

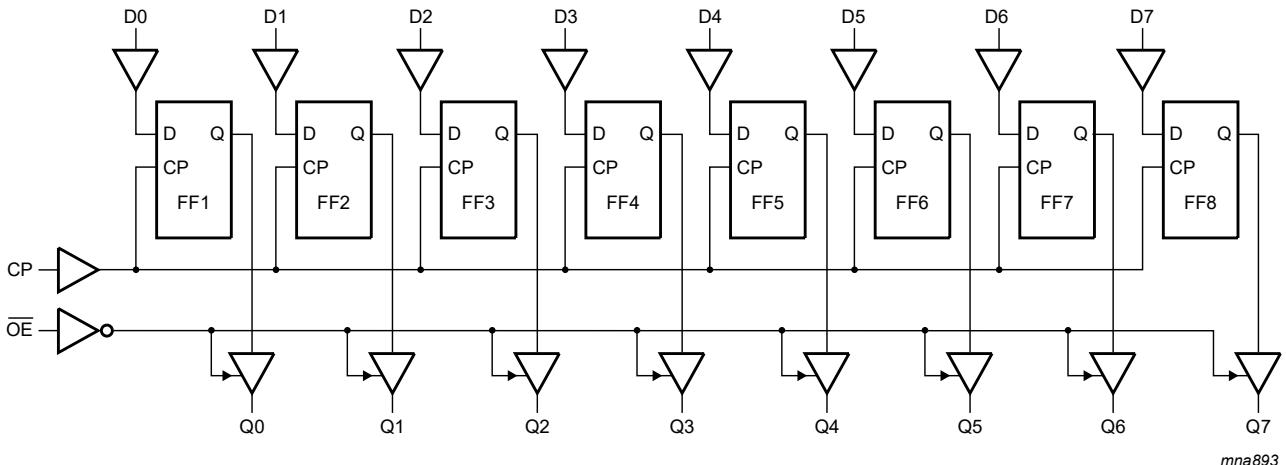
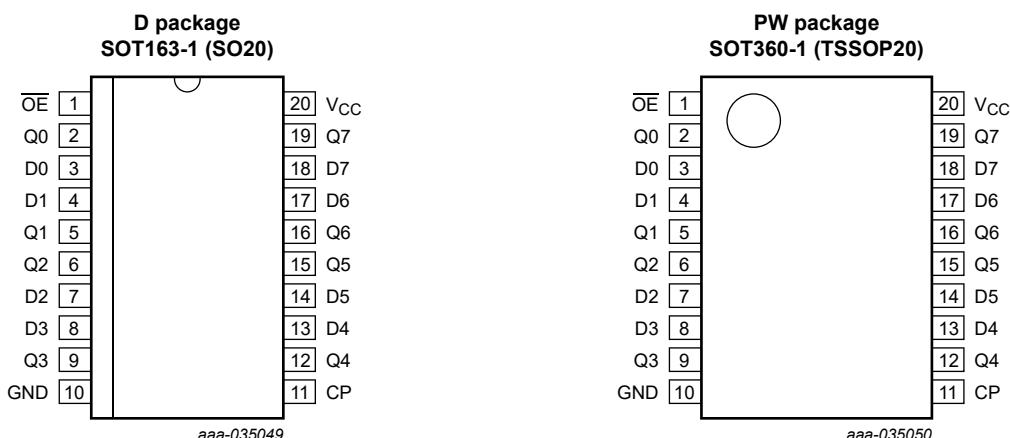


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data inputs
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	data outputs
OE	1	output enable input (active LOW)
CP	11	clock pulse input (active rising edge)
GND	10	ground (0 V)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

Z = high-impedance OFF-state; ↑ = LOW-to-HIGH clock transition.

Operating mode	Input			Internal flip-flops	Output
	OE	CP	D _n		Q _n
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
I_O	output current	$-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$	-	± 35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.

For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC374			74HCT374			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} (°C)						Unit	
			25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
74HC374										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0 V; V _O = V _{CC} or GND	-	-	±0.5	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	T _{amb} (°C)							Unit	
			25			-40 to +85		-40 to +125			
			Min	Typ	Max	Min	Max	Min	Max		
74HCT374											
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V	
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V									
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V	
		I _O = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V									
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V	
		I _O = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V	
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA	
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND	-	-	±0.5	-	±5.0	-	±10	µA	
I _{CC}	supply current	V _I = V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A	-	-	8.0	-	80	-	160	µA	
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A									
		OE input	-	125	450	-	563	-	613	µA	
		CP input	-	90	324	-	405	-	441	µA	
		D _n inputs	-	35	126	-	158	-	172	µA	
C _I	input capacitance		-	3.5	-	-	-	-	-	pF	

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 7](#).

Symbol	Parameter	Conditions	T _{amb} (°C)						Unit	
			25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
74HC374										
t _{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		V _{CC} = 2.0 V	-	50	165	-	205	-	250	ns
		V _{CC} = 4.5 V	-	18	33	-	41	-	50	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	28	-	35	-	43	ns
t _{en}	enable time	OE to Qn; see Fig. 6 [2]								
		V _{CC} = 2.0 V	-	41	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V _{CC} = 6.0 V	-	12	26	-	33	-	38	ns
t _{dis}	disable time	OE to Qn; see Fig. 6 [3]								
		V _{CC} = 2.0 V	-	50	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	18	30	-	38	-	45	ns
		V _{CC} = 6.0 V	-	14	26	-	33	-	38	ns
t _t	transition time	Qn; see Fig. 5 [4]								
		V _{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V _{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V _{CC} = 6.0 V	-	4	10	-	13	-	15	ns
t _w	pulse width	CP; HIGH or LOW; see Fig. 5								
		V _{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _{su}	set-up time	Dn to CP; see Fig. 5								
		V _{CC} = 2.0 V	60	14	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	5	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	4	-	13	-	15	-	ns
t _h	hold time	Dn to CP; see Fig. 5								
		V _{CC} = 2.0 V	5	-6	-	5	-	5	-	ns
		V _{CC} = 4.5 V	5	-2	-	5	-	5	-	ns
		V _{CC} = 6.0 V	5	-2	-	5	-	5	-	ns
f _{max}	maximum frequency	CP; see Fig. 5								
		V _{CC} = 2.0 V	6.0	23	-	4.8	-	4.0	-	MHz
		V _{CC} = 4.5 V	30	70	-	24	-	20	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	77	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	83	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	per flip-flop; V _I = GND to V _{CC} [5]	-	17	-			-	-	pF

Symbol	Parameter	Conditions	T _{amb} (°C)						Unit	
			25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
74HCT374										
t _{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	16	32	-	40	-	48	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
t _{en}	enable time	OE to Qn; V _{CC} = 4.5 V; see Fig. 6 [2]	-	16	30	-	38	-	45	ns
t _{dis}	disable time	OE to Qn; V _{CC} = 4.5 V; see Fig. 6 [3]	-	18	28	-	35	-	42	ns
t _t	transition time	Qn; V _{CC} = 4.5 V; see Fig. 5 [4]	-	5	12	-	15	-	18	ns
t _w	pulse width	CP; HIGH or LOW; V _{CC} = 4.5 V; see Fig. 5	19	11	-	24	-	29	-	ns
t _{su}	set-up time	Dn to CP; V _{CC} = 4.5 V; see Fig. 5	12	7	-	15	-	18	-	ns
t _h	hold time	Dn to CP; V _{CC} = 4.5 V; see Fig. 5	5	-3	-	5	-	5	-	ns
f _{max}	maximum frequency	CP; V _{CC} = 4.5 V; see Fig. 5	26	44	-	21	-	17	-	MHz
		CP; V _{CC} = 5 V; C _L = 15 pF	-	48	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	per flip-flop; V _I = GND to V _{CC} - 1.5 V [5]	-	17	-			-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_{en} is the same as t_{PZH} and t_{PZL}.

[3] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

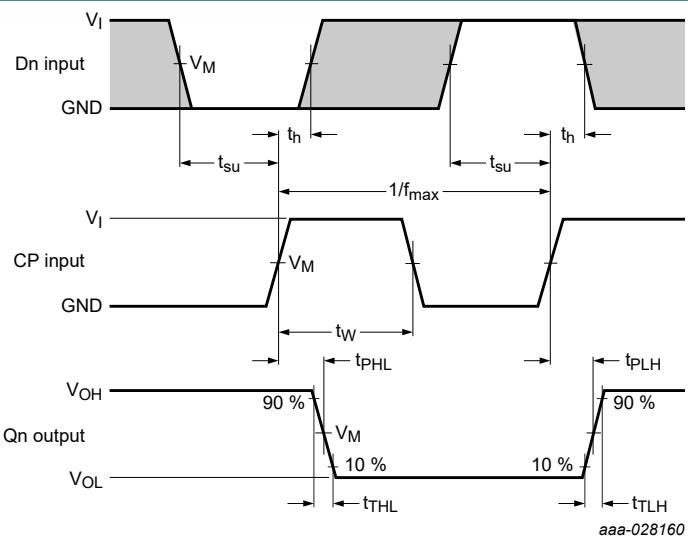
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

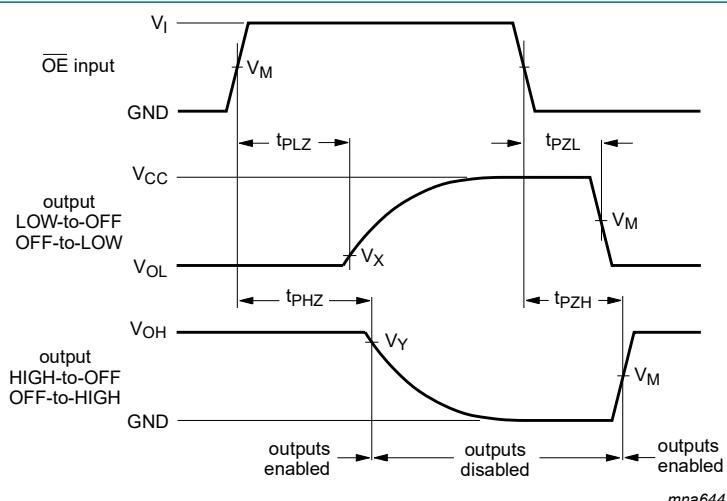


Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Clock input (CP) to output (Qn) propagation delay, clock pulse width, data (Dn) to clock (CP) set-up and hold times, output transition times (Qn) and maximum clock frequency



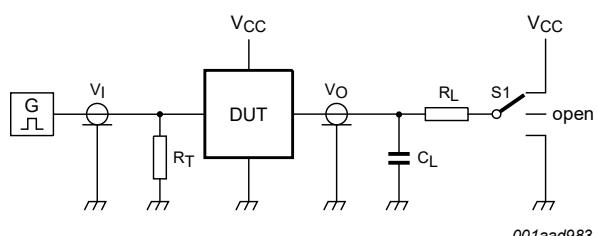
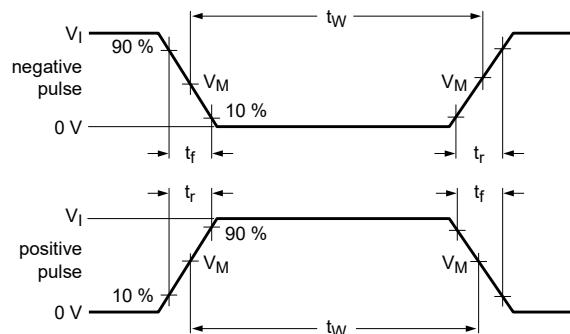
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. 3-state enable and disable times

Table 8. Measurement points

Type	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
74HC374	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$
74HCT374	GND to 3 V	1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

$S1$ = Test selection switch.

Fig. 7. Test circuit for measuring switching times

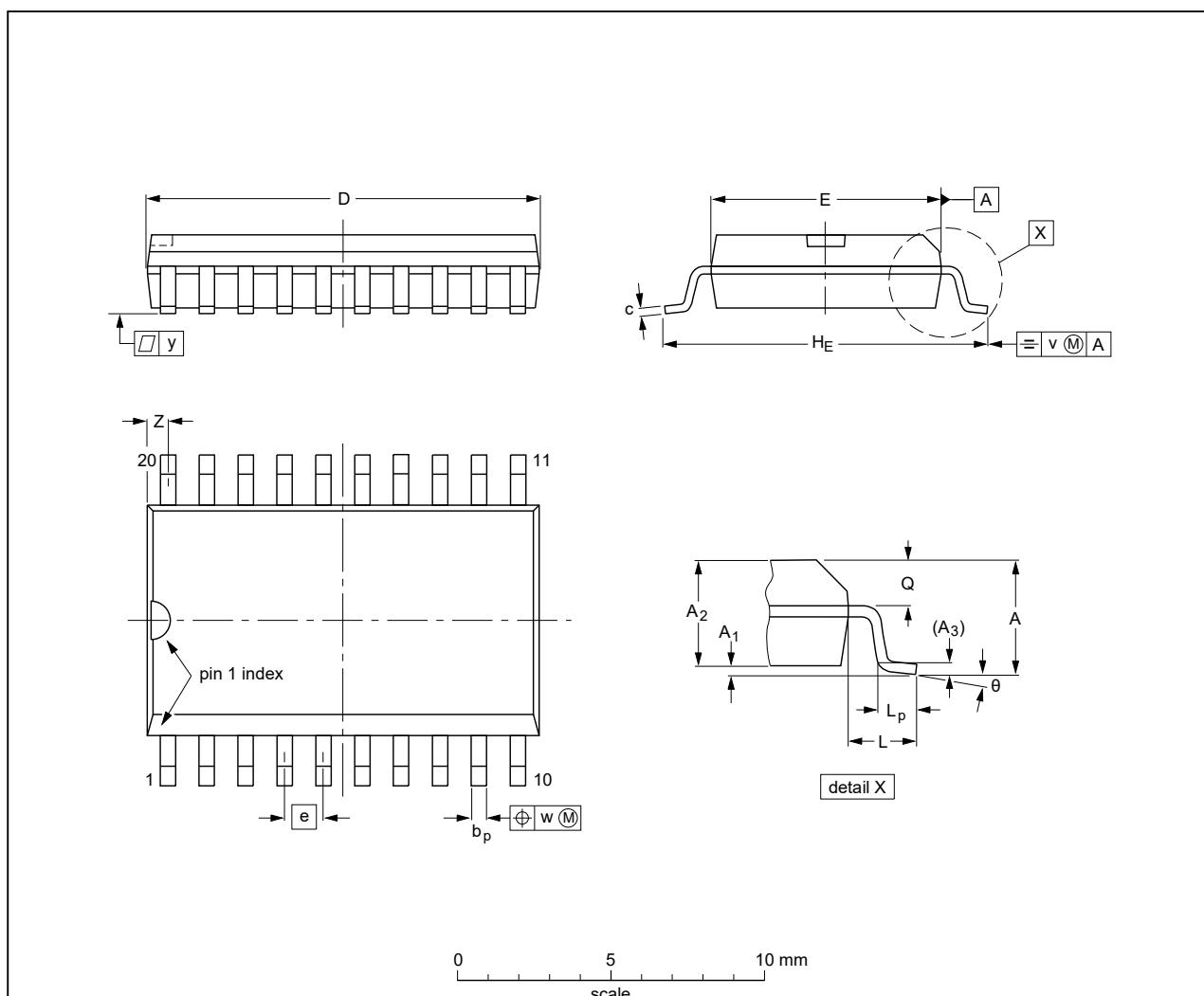
Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC374	GND to V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT374	GND to 3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ	
mm	2.65	0.3	2.45	0.25	0.49	0.32	13.0	7.6	1.27	10.65	1.4	1.1	1.1	0.25	0.25	0.1	0.9	8°	
inches	0.1	0.012	0.096	0.01	0.019	0.013	12.6	7.4	0.23	10.00	0.4	1.0	1.0	0.016	0.039	0.004	0.035	0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

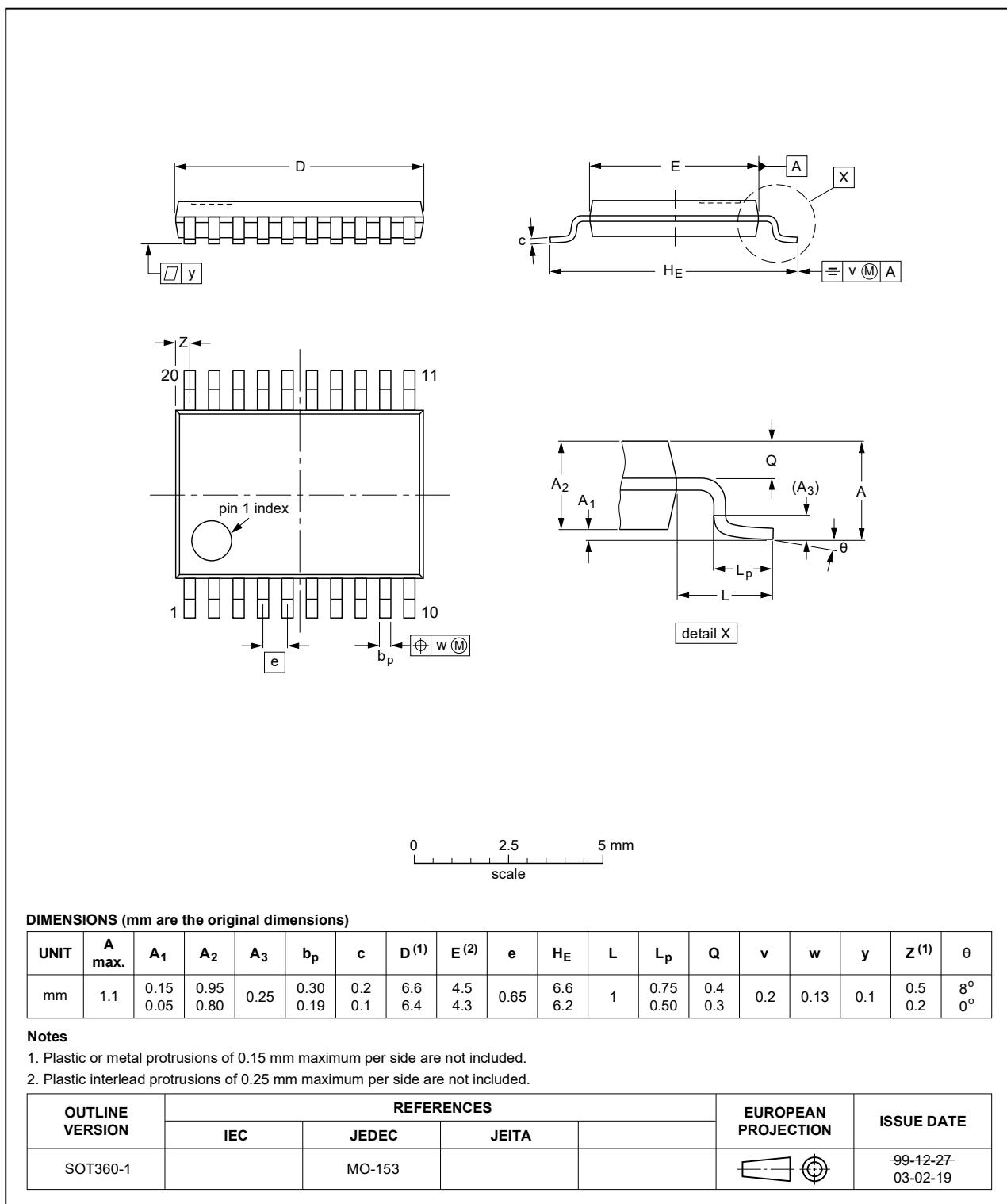


Fig. 9. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT374 v.6	20240805	Product data sheet	-	74HC_HCT374 v.5
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74HC_HCT374 v.5	20210907	Product data sheet	-	74HC_HCT374 v.4
Modifications:	<ul style="list-style-type: none"> Types 74HC374 and 74HCT374 (SOT339-1/SSOP20) removed 			
74HC_HCT374 v.4	20210302	Product data sheet	-	74HC_HCT374 v.3
Modifications:	<ul style="list-style-type: none"> Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT374 v.3	20180220	Product data sheet	-	74HC_HCT374 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT374 v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

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Octal D-type flip-flop; positive edge-trigger; 3-state

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