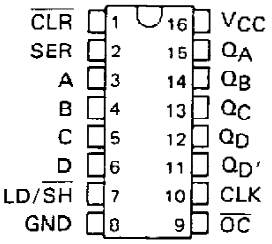
SN54LS395A, SN74LS395A
4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

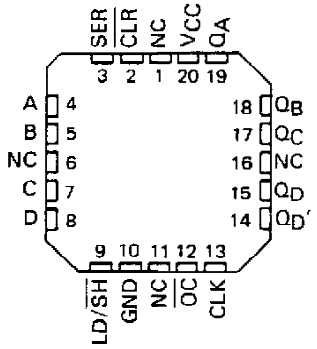
SDLS172 OCTOBER 1976 – REVISED MARCH 1988

- **Three-State, 4 Bit, Cascadable, Parallel-In, Parallel-Out Registers**
- **'LS395A Offers Three Times the Sink-Current Capability of 'LS395**
- **Low Power Dissipation . . . 75 mW Typical (Enabled)**
- **Applications:**
  N-Bit Serial-To-Parallel Converter
  N-Bit Parallel-To-Serial Converter
  N-Bit Storage Register

SN54LS395A . . . J OR W PACKAGE
SN74LS395A . . . D OR N PACKAGE
(TOP VIEW)



SN54LS395A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

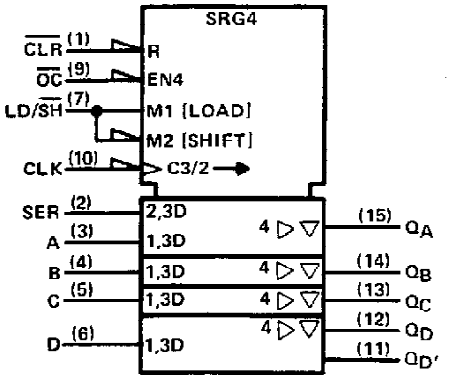
description

These 4-bit registers feature parallel inputs, parallel outputs, and clock (CLK), serial (SER), load shift (LD/$\overline{SH}$), output control ($\overline{OC}$) and direct overriding clear ($\overline{CLR}$) inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

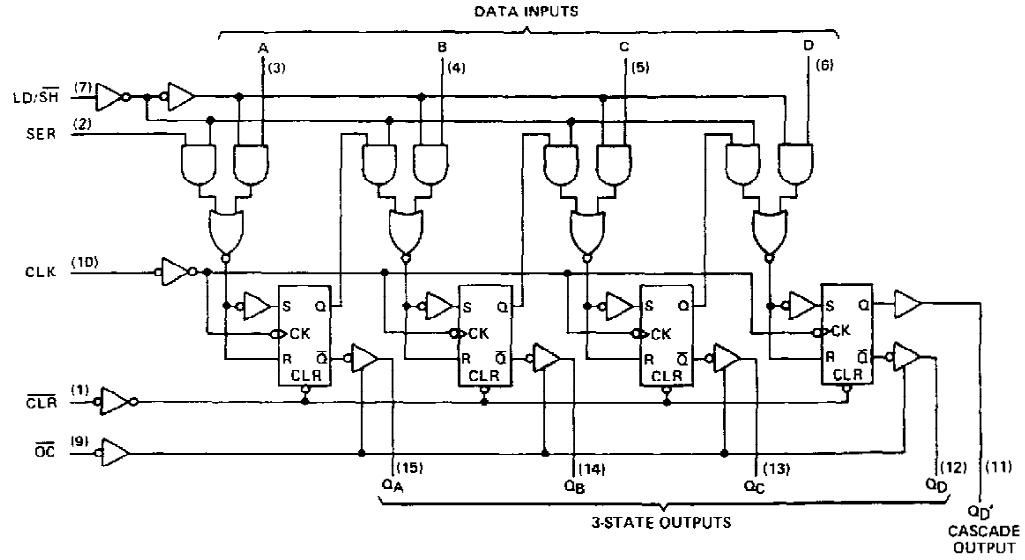
When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-impedance mode, the output at Q_D' is still available for cascading.

logic symbol†



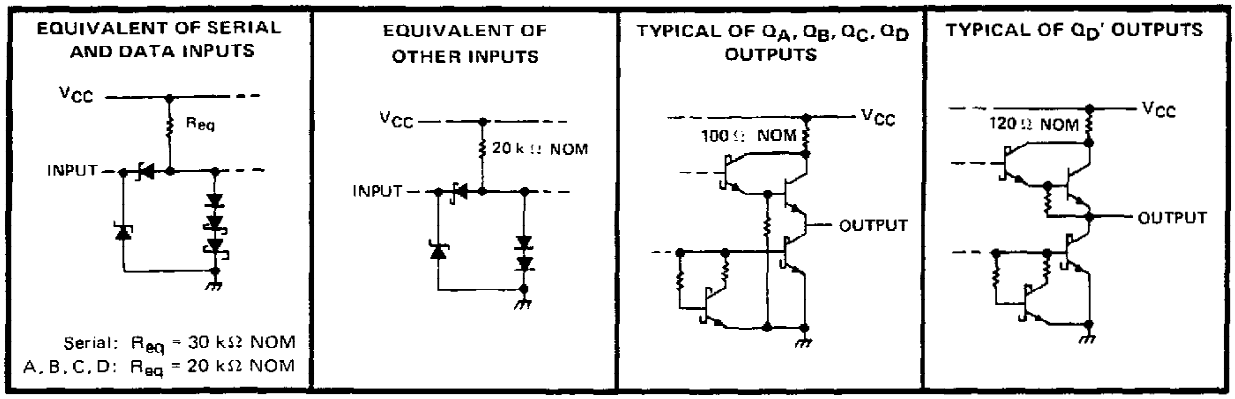
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



FUNCTION TABLE

INPUTS								3-STATE OUTPUTS				CASCADE OUTPUT
$\overline{CLR}$	LD/$\overline{SH}$	CLK	SER	PARALLEL A	B	C	D	Q_A	Q_B	Q_C	Q_D	Q_D'
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↑	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D' are not affected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS395A . . . . . −55°C to 125°C
SN74LS395A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS395A			SN74LS395A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A, Q_B, Q_C, Q_D			−1			−2.6	mA
	Q_D'			−400			−400	μA
Low-level output current, I_{OL}	Q_A, Q_B, Q_C, Q_D			12			24	mA
	Q_D'			4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$		16			16			ns
Setup time, high-level or low-level data, t_{su}	LD/$\overline{SH}$	40			40			ns
	All other inputs	20			20			
Hold time, high-level or low-level data, t_h		10			10			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS395A			SN74LS395A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	Q_A, Q_B, Q_C, Q_D	2.4	3.4		2.4	3.1		V
				Q_D'	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max, V_{IH} = 2 V	Q_A, Q_B, Q_C, Q_D	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
			Q_D'	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,	Q_A, Q_B, Q_C, Q_D			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,	Q_A, Q_B, Q_C, Q_D			−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		Q_A, Q_B, Q_C, Q_D	−30		−130	−30		−130	mA
				Q_D'	−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	Condition A		22	34		22	34	mA
				Condition B		21	31		21	31	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time,and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:
A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
B. Output control and clock input grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	See Note 3, Q_A, Q_B, Q_C, Q_D outputs: R_L = 667 Ω, C_L = 45 pF Q_D' output: R_L = 2 kΩ, C_L = 15 pF	30	45		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output			15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	30	ns
t_{PZH}	Output enable time to high level			15	25	ns
t_{PZL}	Output enable time to low level			17	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Note 3		11	17	ns
t_{PLZ}	Output disable time from low level			12	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
JM38510/30607B2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	Samples Not Available
JM38510/30607BEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
JM38510/30607BEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN54LS395AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN54LS395AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS395AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS395AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS395ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS395ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS395AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS395AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS395AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS395AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS395AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS395AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS395AW	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS395AW	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF SN54LS395A, SN74LS395A :

- Catalog: SN74LS395A
- Military: SN54LS395A

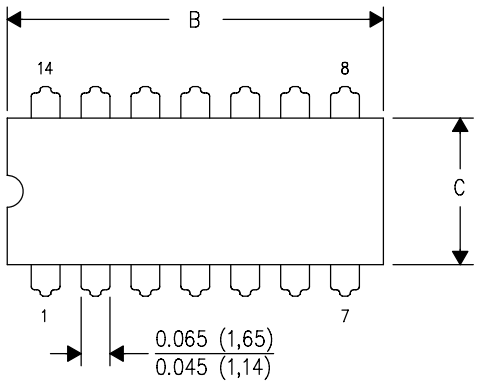
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

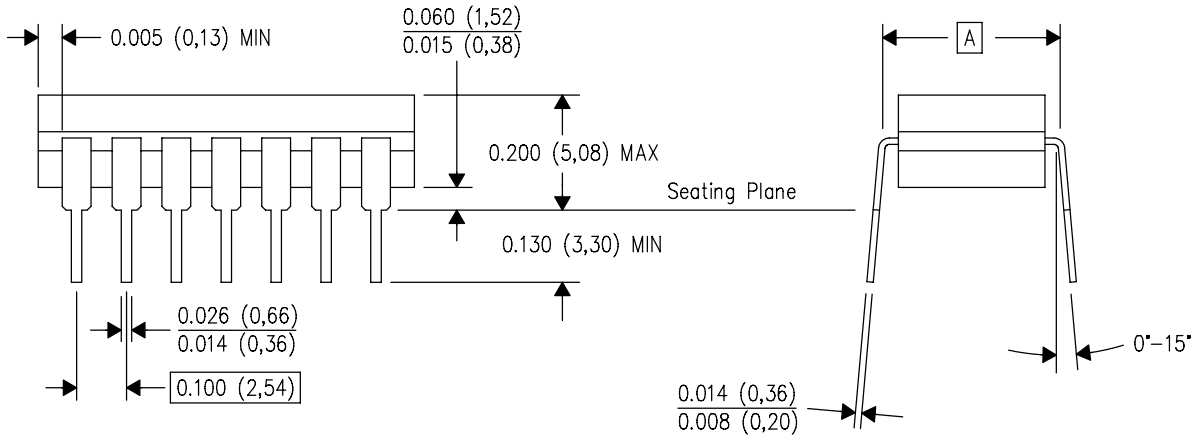
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



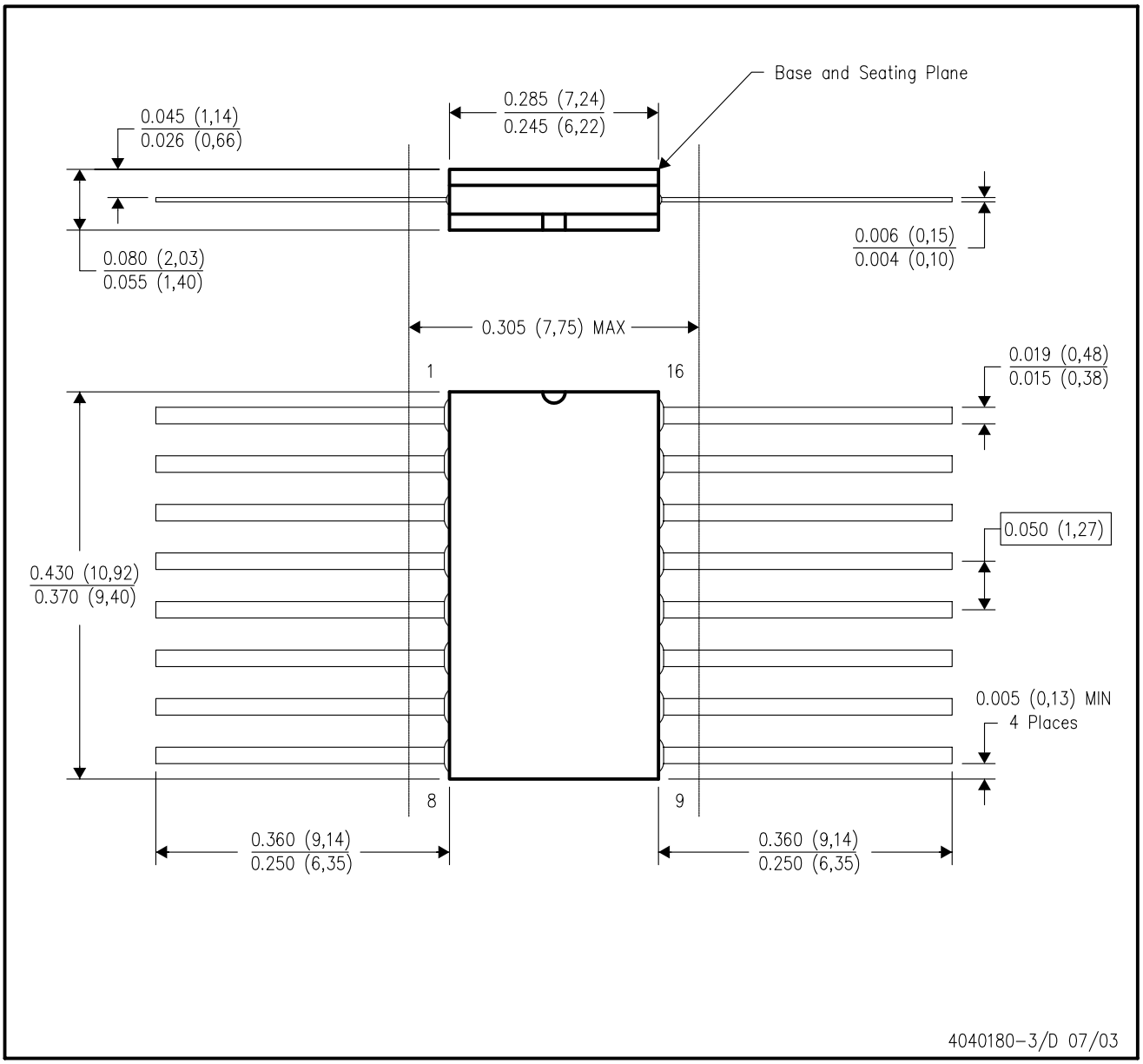
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

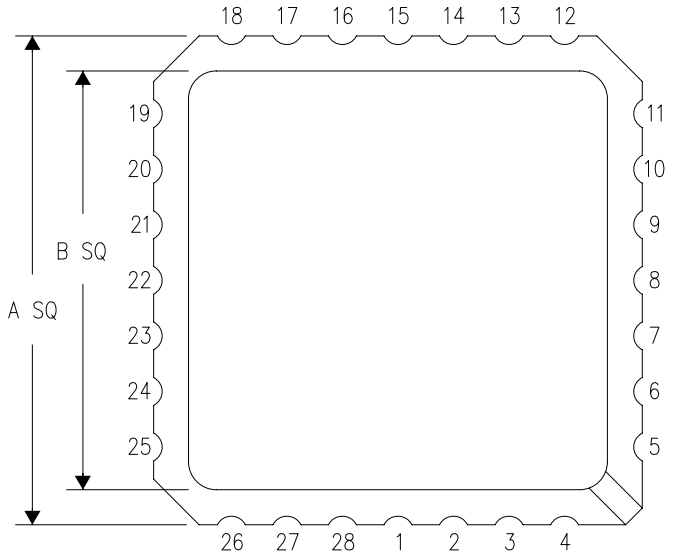
W (R–GDFP–F16) CERAMIC DUAL FLATPACK



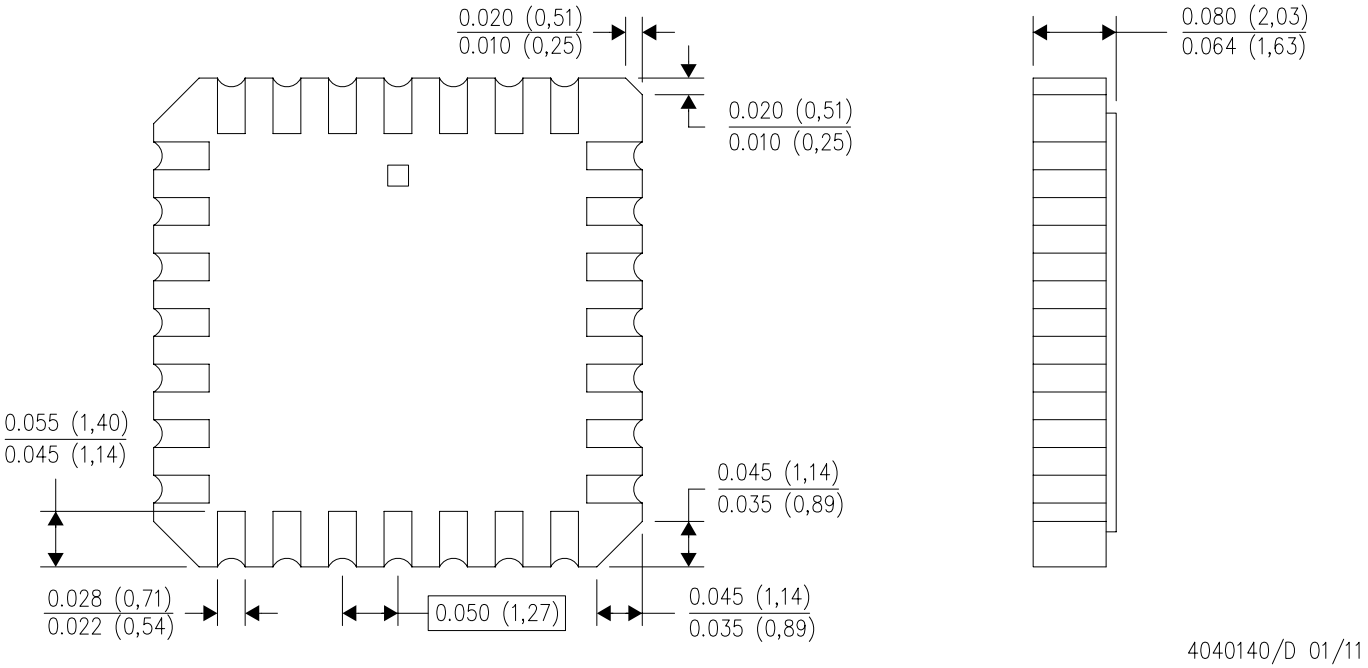
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



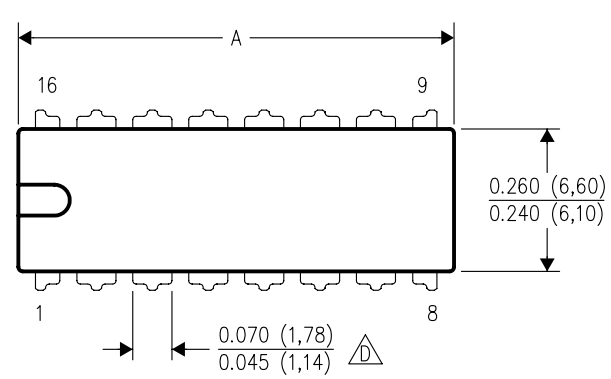
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

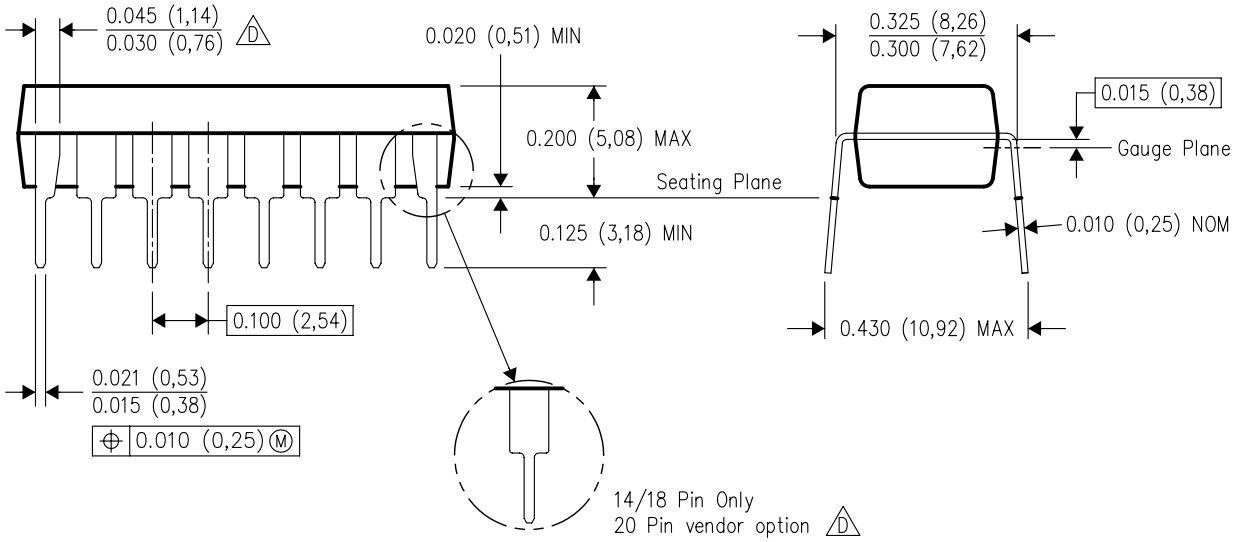
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



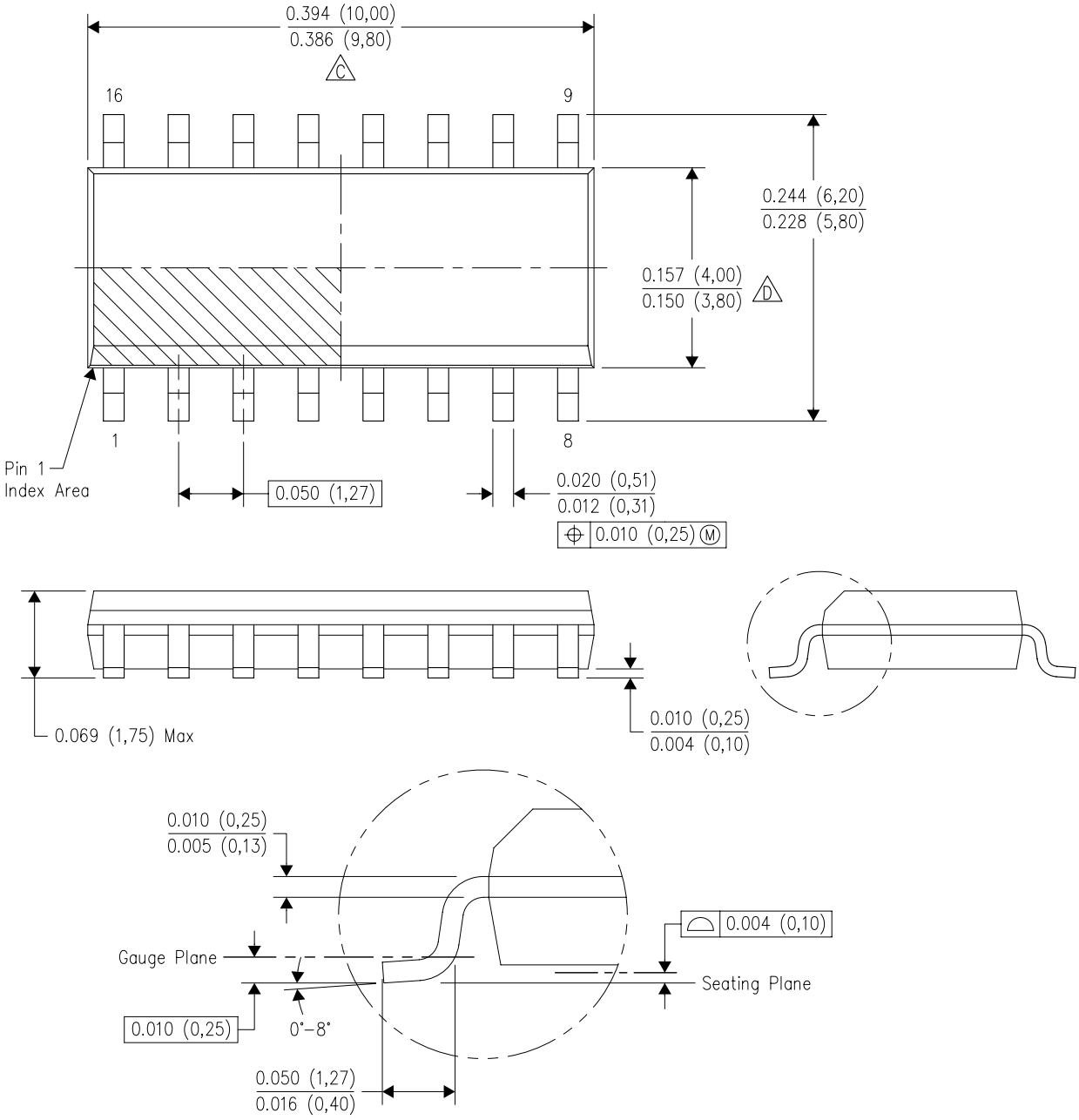
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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