



# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

MAX551/MAX552

## General Description

The MAX551/MAX552 are 12-bit, current-output, 4-quadrant multiplying digital-to-analog converters (DACs). These devices are capable of providing unipolar or bipolar outputs when operating from either a single +5V (MAX551) or +3V (MAX552) power supply. An internal power-on-reset circuit clears all DAC registers on power-up, setting the DAC output voltage to 0V.

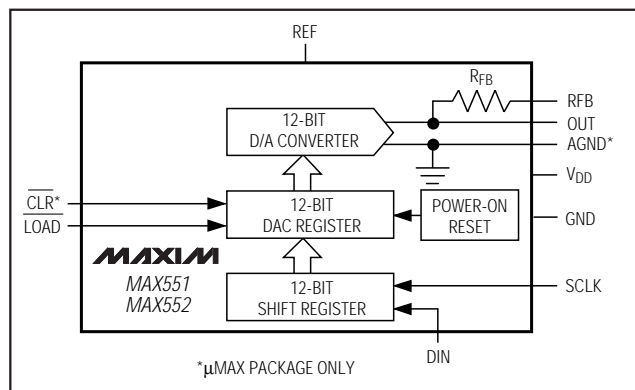
The SPI™/QSPI™ and Microwire™-compatible 3-wire serial interface saves board space and reduces power dissipation compared with parallel-interface devices. The MAX551/MAX552 feature double-buffered interface logic with a 12-bit input register and a 12-bit DAC register. Data in the DAC register sets the DAC output voltage. Data is loaded into the input register via the serial interface. The  $\overline{\text{LOAD}}$  input transfers data from the input register to the DAC register, updating the DAC output voltage.

The MAX551/MAX552 are available in an 8-pin DIP package or a space-saving 10-pin  $\mu$ MAX package. The  $\mu$ MAX package provides an asynchronous clear (CLR) input that clears all DAC registers when pulled to GND, setting the output voltage to 0V.

## Applications

Automatic Calibration  
Gain Adjustment  
Transducer Drivers  
Process-Control I/O Boards  
Digitally Controlled Filters  
Motion-Controlled Systems  
 $\mu$ P-Controlled Systems  
Programmable Amplifiers/Attenuators

## Functional Diagram



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## Features

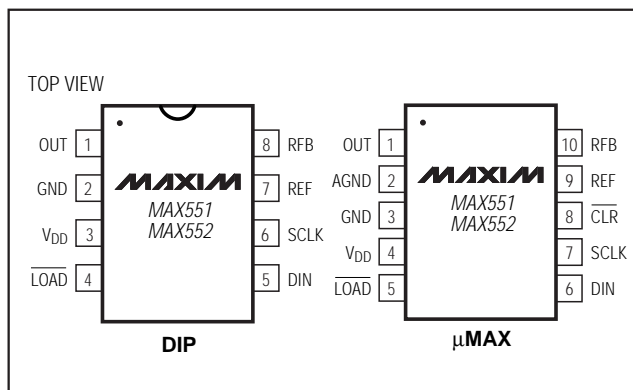
- ♦ **Single-Supply Operation:**  
+4.5V to +5.25V (MAX551)  
+2.7V to +3.6V (MAX552)
- ♦ **12.5MHz 3-Wire Serial Interface**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Power-On Reset Clears DAC Output to Zero**
- ♦ **Asynchronous Clear Input Clears DAC Output to Zero**
- ♦ **Voltage Mode or Bipolar Mode Operation with a Single Power Supply**
- ♦ **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**
- ♦ **0.4 $\mu$ A Supply Current**
- ♦ **10-Pin  $\mu$ MAX Package**

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSB)
MAX551ACPA	0°C to +70°C	8 Plastic DIP	$\pm 1/2$
MAX551BCPA	0°C to +70°C	8 Plastic DIP	$\pm 1$
MAX551ACUB	0°C to +70°C	10 $\mu$ MAX	$\pm 1/2$
MAX551BCUB	0°C to +70°C	10 $\mu$ MAX	$\pm 1$
MAX551AEPA	-40°C to +85°C	8 Plastic DIP	$\pm 1/2$
MAX551BEPA	-40°C to +85°C	8 Plastic DIP	$\pm 1$
MAX551AEUB	-40°C to +85°C	10 $\mu$ MAX	$\pm 1/2$
MAX551BEUB	-40°C to +85°C	10 $\mu$ MAX	$\pm 1$

Ordering Information continued at end of data sheet.

## Pin Configurations



# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$  to GND ..... 6V  
 $V_{REF}$ , RFB to GND .....  $\pm 12V$   
 Digital Inputs (SCLK, DIN,  $\overline{LOAD}$ ,  $\overline{CLR}$ )  
   to GND ..... -0.3V to 6V  
 OUT to GND ..... -0.3V to ( $V_{DD} + 0.3V$ )  
 $AGND$  to GND ..... -0.3V to ( $V_{DD} + 0.3V$ )  
 Continuous Power Dissipation ( $T_A = +70^\circ C$ )  
   Plastic DIP (derate 9.09mW/ $^\circ C$  above  $+70^\circ C$ ) ..... 727mW  
    $\mu$ MAX (derate 5.60mW/ $^\circ C$  above  $+70^\circ C$ ) ..... 444mW

### Operating Temperature Ranges

MAX55\_ \_C\_ .....  $0^\circ C$  to  $+70^\circ C$   
 MAX55\_ \_E\_ .....  $-40^\circ C$  to  $+85^\circ C$   
 Storage Temperature Range .....  $-65^\circ C$  to  $+150^\circ C$   
 Lead Temperature (soldering, 10sec) .....  $+300^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—MAX551

( $V_{DD} = +4.5V$  to  $+5.25V$ ,  $V_{REF} = 5V$ , OUT =  $AGND = GND$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE</b>						
Resolution	N		12			Bits
Integral Nonlinearity	INL				$\pm 1/2$	LSB
					$\pm 1$	
Differential Nonlinearity	DNL	Guaranteed monotonic over temperature			$\pm 1/2$	LSB
					$\pm 1$	
Gain Error		Using internal feedback resistor ( $R_{FB}$ )			$\pm 1$	LSB
					$\pm 2$	
Gain Tempco ( $\Delta Gain/\Delta Temp$ )		Using internal feedback resistor ( $R_{FB}$ ) (Note 2)		$\pm 0.2$	$\pm 1$	ppm/ $^\circ C$
Power-Supply Rejection	PSR	$\Delta V_{DD} = +5\%, -10\%$			2	ppm/%
<b>DYNAMIC PERFORMANCE</b> (Note 3)						
Current Settling Time	$t_S$	$T_A = +25^\circ C$ , to 1/2LSB, OUT load is $100\Omega    13pF$ , DAC register alternately loaded with 1s and 0s		0.08	1	$\mu s$
Digital-to-Analog Glitch		$V_{REF} = 0V$ , OUT load is $100\Omega    13pF$ , DAC register alternately loaded with 1s and 0s		0.65	20	nV-s
AC Feedthrough at OUT		$V_{REF} = 5V_{p-p}$ at 10kHz, DAC register loaded with all 0s		0.3	1	mVp-p
Total Harmonic Distortion	THD	$V_{REF} = 6V_{RMS}$ at 1kHz, DAC register loaded with all 1s		-85		dB
Output Noise-Voltage Density		10Hz to 100kHz, measured between RFB and OUT		13	15	$nV/\sqrt{Hz}$

# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

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## ELECTRICAL CHARACTERISTICS—MAX551 (continued)

( $V_{DD}$  = +4.5V to +5.25V,  $V_{REF}$  = 5V, OUT = AGND = GND,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A$  = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT							
Input Resistance	R <sub>REF</sub>	Measured between REF and OUT		7	11	15	kΩ
Input Resistance Tempco				6.5			ppm/°C
Reference -3dB Bandwidth	BW	V <sub>OUT</sub> = 0.31V <sub>p-p</sub> , R <sub>L</sub> = 50Ω, code = full-scale		725			kHz
ANALOG OUTPUT							
OUT Leakage Current		DAC register loaded with all 0s	T <sub>A</sub> = +25°C	±0.15		±5	nA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	±25			
OUT Capacitance	C <sub>OUT</sub>	Code = zero scale (Note 2)		14		20	pF
		Code = full scale (Note 2)		20		30	
DIGITAL INPUTS							
Input High Voltage	V <sub>IH</sub>			2.4			V
Input Low Voltage	V <sub>IL</sub>					0.8	V
Input Hysteresis	HYST	LOAD, CLR, DIN, and SCLK, V <sub>DD</sub> = 5V		156			mV
Input Leakage Current	I <sub>IN</sub>	CLR	VCLR = V <sub>DD</sub>	±1			μA
			VCLR = 0V	18		100	
		SCLK, LOAD, DIN	Inputs at 0V or V <sub>DD</sub>		±1		
Input Capacitance	C <sub>IN</sub>	Inputs at 0V or V <sub>DD</sub> (Note 2)		8			pF
SWITCHING CHARACTERISTICS							
SCLK Pulse Width High	t <sub>CH</sub>			25			ns
SCLK Pulse Width Low	t <sub>CL</sub>			25			ns
DIN Data to SCLK Setup	t <sub>DS</sub>			15			ns
DIN Data to SCLK Hold	t <sub>DH</sub>			15			ns
LOAD Pulse Width	t <sub>LD</sub>			20			ns
LSB SCLK to LOAD	t <sub>SL</sub>			0			ns
LOAD High to SCLK	t <sub>LC</sub>			15			ns
CLR Pulse Width	t <sub>CLR</sub>			20			ns
POWER SUPPLY							
Supply Voltage	V <sub>DD</sub>			4.50		5.25	V
Supply Current	I <sub>DD</sub>	All digital inputs at V <sub>IL</sub> or V <sub>IH</sub> , CLR = V <sub>DD</sub>		0.5		1.5	mA
		All digital inputs at 0V or V <sub>DD</sub> , CLR = V <sub>DD</sub>		0.4		5	μA

# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

## ELECTRICAL CHARACTERISTICS —MAX552

( $V_{DD}$  = +2.7V to +3.6V,  $V_{REF}$  = 2.5V, OUT = AGND = GND,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A$  = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE</b>						
Resolution	N		12			Bits
Integral Nonlinearity	INL				$\pm 1/2$	LSB
					$\pm 1$	
Differential Nonlinearity	DNL	Guaranteed monotonic over temperature			$\pm 1/2$	LSB
					$\pm 1$	
Gain Error		Using internal feedback resistor ( $R_{FB}$ )			$\pm 1$	LSB
					$\pm 2$	
Gain Tempco ( $\Delta$ Gain/ $\Delta$ Temp)		Using internal feedback resistor ( $R_{FB}$ ) (Note 2)		$\pm 0.3$	$\pm 1$	ppm/ $^{\circ}$ C
Power-Supply Rejection	PSR	$\Delta V_{DD}$ = +20%, -10%			1	ppm/%
<b>DYNAMIC PERFORMANCE</b> (Note 3)						
Current Settling Time	$t_S$	$T_A$ = +25 $^{\circ}$ C, to 1/2LSB, OUT load is 100 $\Omega$   13pF, DAC register alternately loaded with 1s and 0s		0.12	1	$\mu$ s
Digital-to-Analog Glitch		$V_{REF}$ = 0V, OUT load is 100 $\Omega$   13pF, DAC register alternately loaded with 1s and 0s		0.6	20	nV-s
AC Feedthrough at OUT		$V_{REF}$ = 3Vp-p at 10kHz, DAC register loaded with all 0s		0.2	0.6	mVp-p
Total Harmonic Distortion	THD	$V_{REF}$ = 6V <sub>RMS</sub> at 1kHz, DAC register loaded with all 1s		-85		dB
Output Noise-Voltage Density		10Hz to 100kHz, measured between RFB and OUT		13	15	nV/ $\sqrt{Hz}$
<b>REFERENCE INPUT</b>						
Input Resistance	$R_{REF}$	Measured between REF and OUT	7	11	15	k $\Omega$
Input Resistance Tempco				7.5		ppm/ $^{\circ}$ C
Reference -3dB Bandwidth	BW	$V_{OUT}$ = 0.31Vp-p, $R_L$ = 50 $\Omega$ , code = full-scale		725		kHz
<b>ANALOG OUTPUT</b>						
OUT Leakage Current		DAC register loaded with all 0s	$T_A$ = +25 $^{\circ}$ C	$\pm 0.13$	$\pm 5$	nA
			$T_A$ = $T_{MIN}$ to $T_{MAX}$		$\pm 25$	
OUT Capacitance	$C_{OUT}$	Code = zero code (Note 2)		14	20	pF
		Code = full scale (Note 2)		20	30	

# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

MAX551/MAX552

## ELECTRICAL CHARACTERISTICS —MAX552 (continued)

( $V_{DD} = +2.7V$  to  $+3.6V$ ,  $V_{REF} = 2.5V$ ,  $V_{OUT} = AGND = GND$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL INPUTS</b>						
Input High Voltage	$V_{IH}$		2.1			V
Input Low Voltage	$V_{IL}$				0.6	V
Input Hysteresis	HYST	$\overline{LOAD}$ , $\overline{CLR}$ , DIN, and SCLK, $V_{DD} = 3V$		135		mV
Input Leakage Current	$I_{IN}$	$\overline{CLR}$			$\pm 1$	$\mu A$
		$V_{CLR} = V_{DD}$				
		$V_{CLR} = 0V$		12	75	
		SCLK, $\overline{LOAD}$ , DIN			$\pm 1$	
		Inputs at 0V or $V_{DD}$				
Input Capacitance	$C_{IN}$	Inputs at 0V or $V_{DD}$ (Note 2)			8	pF
<b>SWITCHING CHARACTERISTICS</b>						
SCLK Pulse Width High	$t_{CH}$		40			ns
SCLK Pulse Width Low	$t_{CL}$		40			ns
DIN Data to SCLK Setup	$t_{DS}$		15			ns
DIN Data to SCLK Hold	$t_{DH}$		15			ns
$\overline{LOAD}$ Pulse Width	$t_{LD}$		30			ns
LSB SCLK to $\overline{LOAD}$	$t_{SL}$		0			ns
$\overline{LOAD}$ High to SCLK	$t_{LC}$		15			ns
$\overline{CLR}$ Pulse Width	$t_{CLR}$		30			ns
<b>POWER SUPPLY</b>						
Supply Voltage	$V_{DD}$		2.7		3.6	V
Supply Current	$I_{DD}$	All digital inputs at $V_{IL}$ or $V_{IH}$ , $\overline{CLR} = V_{DD}$		0.1	0.5	mA
		All digital inputs at 0V or $V_{DD}$ , $\overline{CLR} = V_{DD}$		0.07	5	$\mu A$

**Note 1:** AGND and  $\overline{CLR}$  are for  $\mu$ MAX only.

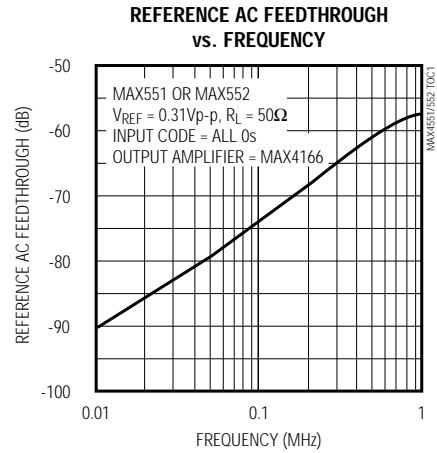
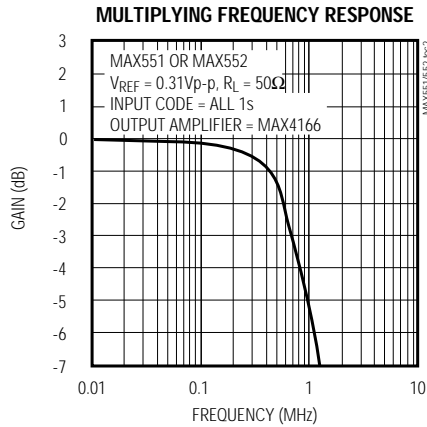
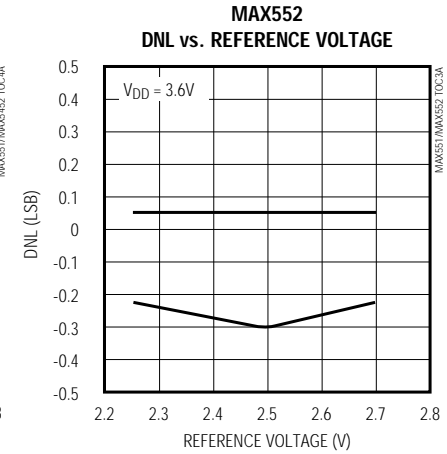
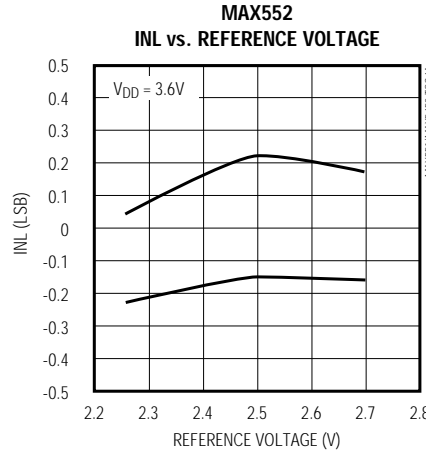
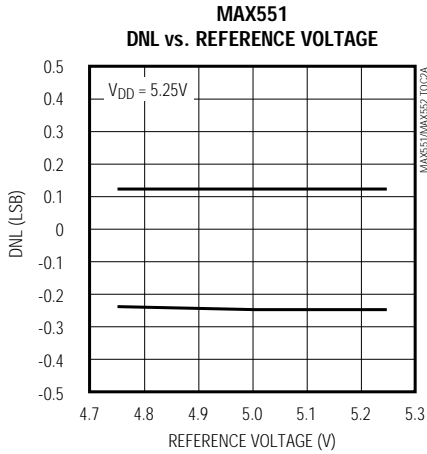
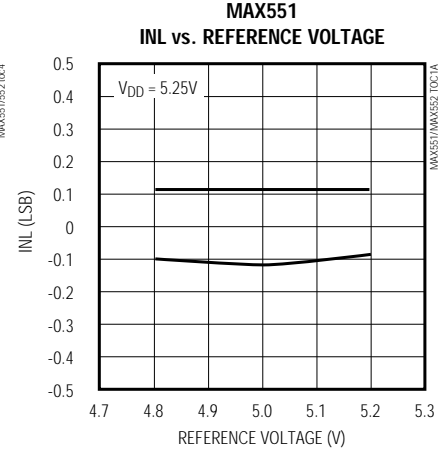
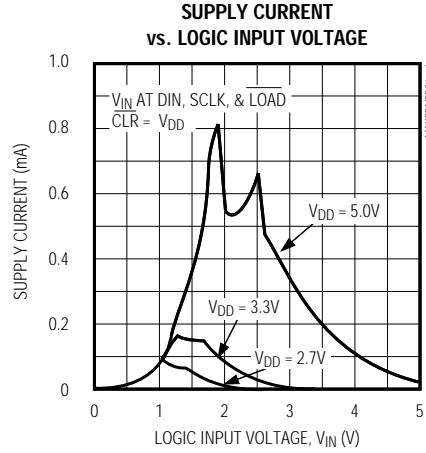
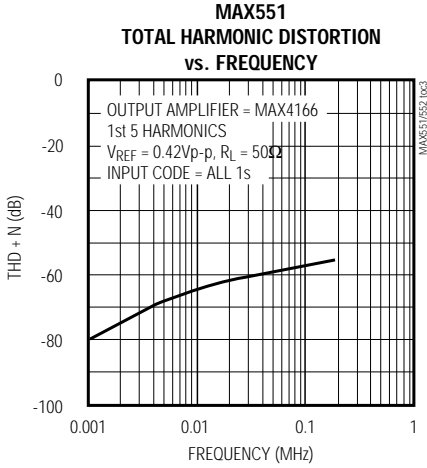
**Note 2:** Guaranteed by design. Not subject to production testing.

**Note 3:** Parametric limits are provided for design guidance, and are not production tested.

# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

## Pin Description

PIN		NAME	FUNCTION
DIP	$\mu$ MAX		
1	1	OUT	DAC Current Output
—	2	AGND	Analog Ground
2	3	GND	Digital Ground. Also Analog Ground for DIP package.
3	4	V <sub>DD</sub>	Supply Voltage
4	5	$\overline{\text{LOAD}}$	Active-Low Load DAC Input. Driving this asynchronous input low transfers the contents of the input register to the DAC register.
5	6	DIN	Serial-Data Input
6	7	SCLK	Serial-Clock Input. The serial input data is clocked in on SCLK's rising edge.
—	8	$\overline{\text{CLR}}$	Clear DAC Input. Clears the DAC register. Tie to V <sub>DD</sub> or float if not used.
7	9	REF	Reference Input
8	10	RFB	Feedback Resistor

MAX551/MAX552

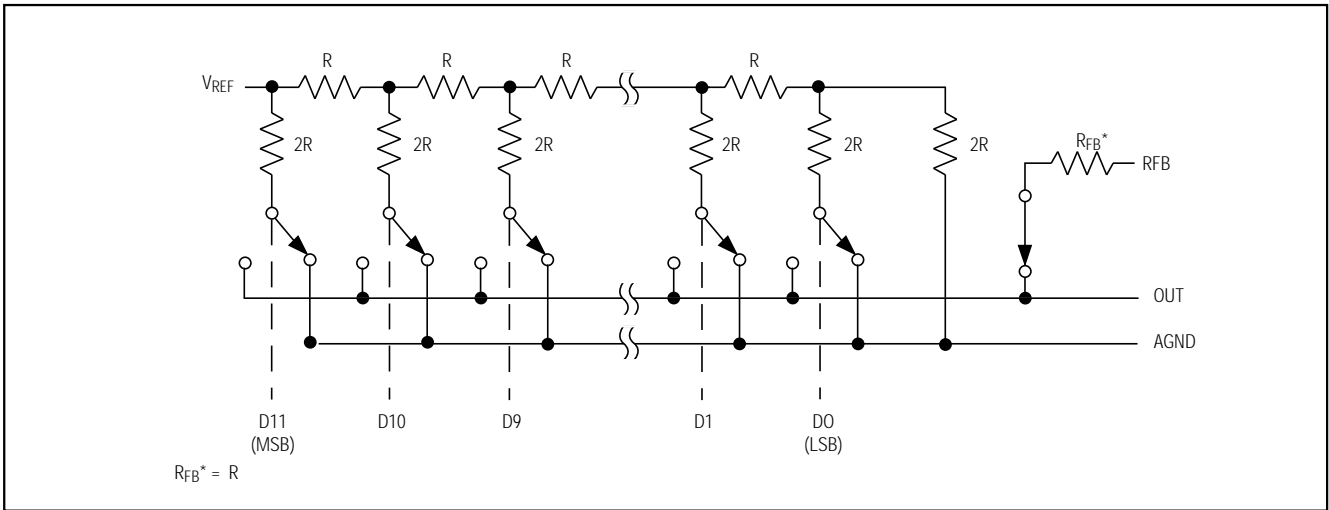


Figure 1. MAX551/MAX552 Simplified Circuit

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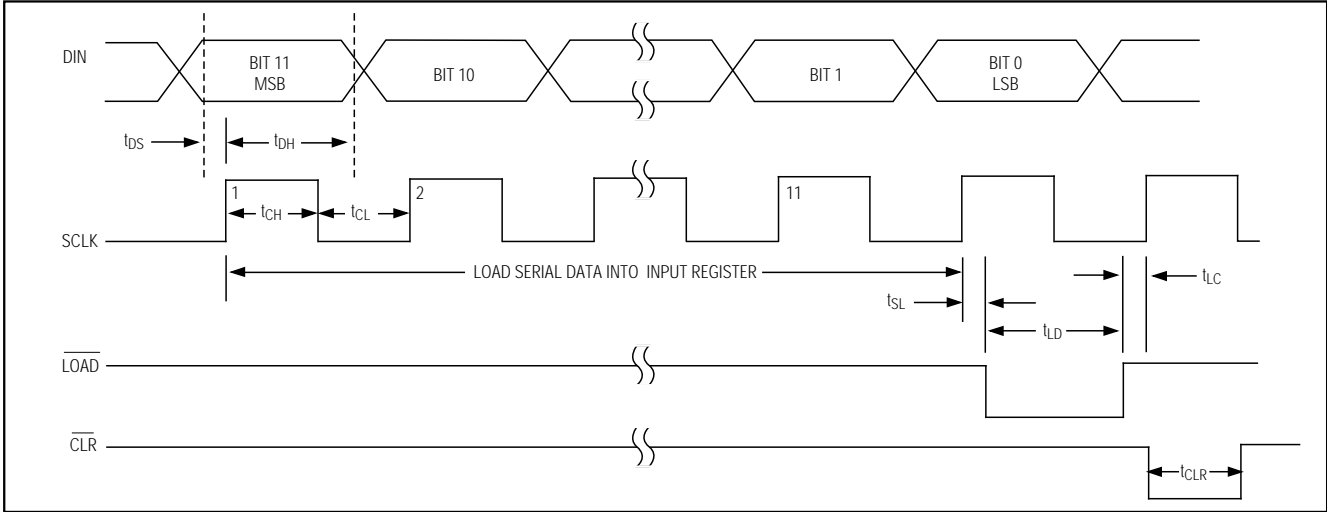


Figure 2. Write-Cycle Timing Diagram

## Detailed Description

The MAX551/MAX552 digital-to-analog converter (DAC) circuits consist of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches (Figure 1). Binary-weighted currents are switched to either OUT or AGND, depending on the status of each input data bit. Although the currents at OUT and AGND depend on the digital input code, the sum of the two output currents is always equal to the input current at REF.

The output current ( $I_{OUT}$ ) can be converted into a voltage by adding an external output amplifier (Figure 3). The REF input accepts a wide range of signals, including fixed and time-varying voltage or current inputs. If a current source is used at the reference input, use a low-tempco, external feedback resistor in place of the

internal feedback resistor ( $R_{FB}$ ) to minimize gain variation with temperature.

The internal feedback resistor ( $R_{FB}$ ) is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array, resulting in excellent supply rejection and gain-temperature coefficient.

The OUT pin output capacitance ( $C_{OUT}$ ) is code dependent.  $C_{OUT}$  is typically 14pF at 000hex and 20pF at FFFhex.

## Serial Interface

The MAX551/MAX552 serial interface is compatible with the SPI/QSPI and Microwire serial-interface standards. These devices accept serial clocks up to 12.5MHz (50% duty cycle). If the SCLK input is not

Table 1. Unipolar Binary-Code Table for Circuit of Figure 3

DIGITAL INPUT			ANALOG OUTPUT
MSB	LSB		
1111	1111	1111	$-V_{REF} \left( \frac{4095}{4096} \right)$
1000	0000	0000	$-V_{REF} \left( \frac{2048}{4096} \right) = -\frac{V_{REF}}{2}$
0000	0000	0001	$-V_{REF} \left( \frac{1}{4096} \right)$
0000	0000	0000	0

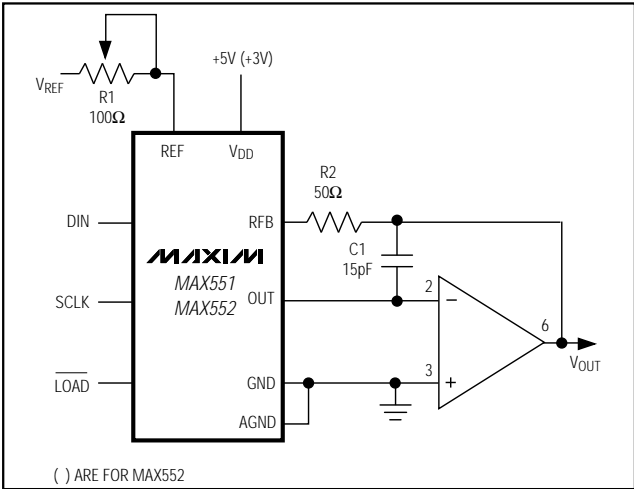


Figure 3. Unipolar Operation



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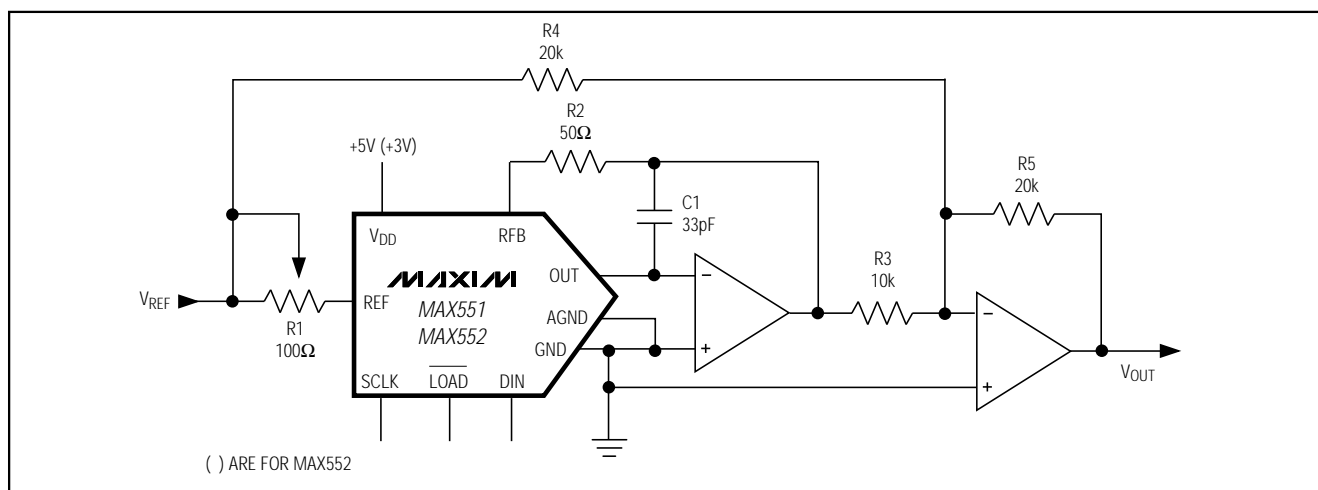


Figure 4. Bipolar Operation

**Table 2. Offset Binary-Code Table  
for Circuit of Figure 4**

DIGITAL INPUT			ANALOG OUTPUT
MSB		LSB	
1111	1111	1111	$+V_{REF} \left( \frac{2047}{2048} \right)$
1000	0000	0001	$+V_{REF} \left( \frac{1}{2048} \right)$
1000	0000	0000	0
0111	1111	1111	$-V_{REF} \left( \frac{1}{2048} \right)$
0000	0000	0000	$-V_{REF} \left( \frac{2048}{2048} \right)$

symmetrical, then the clock signal used must meet the  $t_{CH}$  and  $t_{CL}$  requirements given in the *Electrical Characteristics*.

Figure 2 shows the MAX551/MAX552 timing diagram. The most significant bit (MSB) is always loaded first on SCLK's rising edge. When all data is shifted into the input register, the DAC register is loaded by driving the  $\overline{LOAD}$  signal low. The DAC register is transparent when  $\overline{LOAD}$  is low and latched when  $\overline{LOAD}$  is high. The MAX551/MAX552 digital inputs are compatible with CMOS logic levels. The MAX551's inputs are also compatible with TTL logic.

## Unipolar Operation

Figure 3 shows the MAX551/MAX552's basic application. This circuit is used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 1. Note that the output's polarity is the opposite of the reference voltage polarity.

In many applications the gain accuracy is sufficient and gain adjustment is not necessary. In these cases, resistors R1 and R2 in Figure 3 can be omitted. If the gain is trimmed and the DAC is operated over a wide temperature range, use low-tempco ( $<300\text{ppm}/^{\circ}\text{C}$ ) resistors for R1 and R2. Capacitor C1 provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the DAC's output.

## Bipolar Operation

Figure 4 shows the MAX551/MAX552 operating in bipolar (or 4-quadrant multiplying) mode. Matched resistors R3, R4, and R5 must be of the same material (preferably metal film or wire-wound) for good temperature-tracking characteristics ( $<15\text{ppm}/^{\circ}\text{C}$ ) and should match to 0.01% for 12-bit performance. The output code is offset binary, as listed in Table 2.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is needed to adjust the ratio of R3 and R4 for 0V out. Trim full scale by loading the DAC with all 0s or 1s and adjusting the  $V_{REF}$  amplitude or varying R5 until the desired positive or negative output is obtained. In applications where gain trim is not required, omit resistors R1 and R2. If gain trim is desired and the DAC is operated over a wide tempera-

# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

ture range, then low-tempco ( $<300\text{ppm}/^\circ\text{C}$ ) resistors should be used.

## Applications Information

### Output Amplifier

For best linearity, terminate OUT and GND at exactly 0V. In most applications, OUT is connected to an inverting op amp's summing junction. The amplifier's input offset voltage can degrade the DAC's linearity by causing OUT to be terminated to a nonzero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS} (1 + R_{FB} / R_O)$$

where  $V_{OS}$  = is the op amp's offset and  $R_O$  is the DAC's output resistance, which is code dependent. The maximum error voltage ( $R_O = R_{FB}$ ) is  $2V_{OS}$ ; the minimum error voltage ( $R_O = \infty$ ) is  $V_{OS}$ . To minimize this error, use a low-offset amplifier such as the MAX4166 (unipolar output) or the MAX427 (bipolar output). Otherwise, the amplifier offset must be trimmed to zero. A good guide rule is that  $V_{OS}$  should be no more than 1/10LSB.

The output amplifier's input bias current ( $I_B$ ) can also limit performance, since  $I_B \times R_{FB}$  generates an offset error. Choose an op amp with an  $I_B$  much less than (e.g., one-tenth) the DAC's 1LSB output current (typically 111nA when  $V_{REF} = 5\text{V}$ , and 55.5nA when  $V_{REF} = 2.5\text{V}$ ). Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a bias-current compensation resistor. This resistor adds to the offset at this pin and thus should not be used. For best performance, connect the noninverting input directly to ground.

In static or DC applications, the output amplifier's characteristics are not critical. In higher speed applications in which either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the output op amp's AC parameters must be considered.

A compensation capacitor,  $C_1$ , may be required when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance,  $C_{OUT}$ , and the

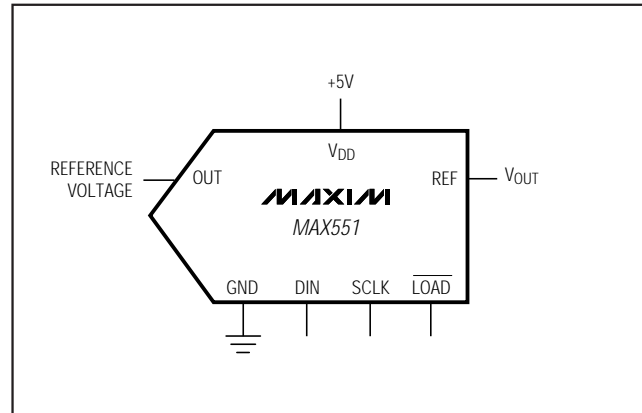


Figure 5. Single-Supply, Voltage Mode Operation

internal feedback resistor,  $R_{FB}$ . Its value depends on the type of op amp used but typically ranges from 14pF to 30pF. Too small a value causes output ringing, while excess capacitance overdamps the output.  $C_1$ 's size can be minimized and the output voltage settling time improved by keeping the circuit-board trace short and stray capacitance at OUT as low as possible.

## Single-Supply Operation

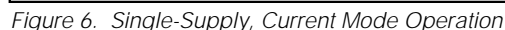
### Reference Voltage

The MAX551/MAX552 are true 4-quadrant DACs, making them ideal for multiplying applications. The reference input accepts both AC and DC signals within a voltage range of  $\pm 6\text{V}$ . The R-2R ladder is implemented with thin-film resistors, enabling the use of unipolar or bipolar reference voltages with only a single power supply for the DAC. The voltage at the  $V_{REF}$  input sets the DAC's full-scale output voltage.

If the reference is too noisy, it should be bypassed to GND (AGND on the 10-pin  $\mu$ MAX package) with a 0.1 $\mu\text{F}$  ceramic capacitor located as close to the REF pin as possible.

### Voltage Mode (MAX551)

The MAX551 can be conveniently used in voltage mode, single-supply operation with OUT biased at any voltage between GND and  $V_{DD}$ . OUT must not be allowed to go 0.3V lower than GND or 0.3V higher than  $V_{DD}$ . Otherwise, internal diodes will turn on, causing a high current flow that could damage the device.

$$\text{MAX551/MAX552}$$


An advantage of voltage mode operation is that a negative reference is not required for a positive output. Note that the reference input (OUT) must always be positive and is limited to no more than 2V when  $V_{DD}$  is 5V. The unipolar and bipolar circuits in Figures 3 and 4 can be converted to voltage mode.

Figure 6 shows the MAX551/MAX552 in a current output configuration in which the output amplifier is powered from a single supply, and AGND is biased to 1.23V. With 0V applied to the REF input, the output can be programmed from 1.23V (zero code) to 2.46V (full



The MAX4166 op amp that drives AGND maintains the 1.23V bias as AGND's impedance changes with the DAC's digital code, from high impedance (zero code) to 7k $\Omega$  minimum (full scale).

In applications where reference voltage has AC signal components, the MAX551/MAX552 have multiplying capability within the reference input range of  $\pm 6V$ . If the DAC and the output amplifier are operated with a single supply voltage, then an AC reference input can be offset with the circuit shown in Figure 7 to prevent the DAC output voltage from exceeding the output amplifier's negative output rail. The reference input's typical -3dB bandwidth is greater than 700kHz, as shown in the *Typical Operating Characteristics* graphs.

The MAX551/MAX552 provide separate AGND and GND inputs in the  $\mu$ MAX package. With this package, AGND can be biased above GND to provide an arbitrary nonzero output voltage for a “0” input code (Figure 8).

Bypass VDD with a 0.1µF capacitor, located as close to VDD and GND as possible. The ground pins (AGND and GND) should be connected in a star configuration to the highest quality ground available, which should be located as close to the MAX551/MAX552 as possible.

**MAXIM**

# +3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin $\mu$ MAX Package

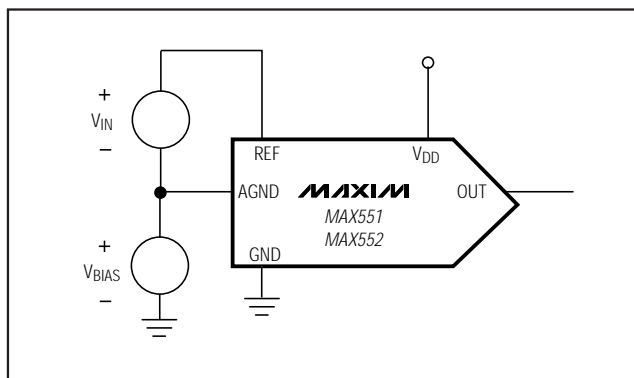


Figure 8. AGND Bias Current

grounded should be connected directly to a single-point ground through a separate, low-resistance (less than  $0.2\Omega$ ) connection. The current at OUT and AGND varies with input code, creating a code-dependent error if these terminals are connected to ground (or virtual ground) through a resistive path.

Parasitic coupling of the signal from REF to OUT is an error source in dynamic applications. This coupling is normally a function of board layout and pin-to-pin package capacitance. Minimize digital feedthrough with guard traces between digital inputs, REF, and OUT pins.

The MAX551/MAX552 have high-impedance digital inputs. To minimize noise pick-up, tie them to either  $V_{DD}$  or GND when they are not in use. As a good prac-

tice, connect active inputs to  $V_{DD}$  or GND through high-value resistors ( $1M\Omega$ ) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected.

The  $\overline{CLR}$  input on the  $\mu$ MAX device has an internal pull-up resistor with a typical value of  $125k\Omega$ . If the  $\overline{CLR}$  input is not used, tie it to  $V_{DD}$  to minimize supply current.

## Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSB)
MAX552ACPA	0°C to +70°C	8 Plastic DIP	$\pm 1/2$
MAX552BCPA	0°C to +70°C	8 Plastic DIP	$\pm 1$
MAX552ACUB	0°C to +70°C	10 $\mu$ MAX	$\pm 1/2$
MAX552BCUB	0°C to +70°C	10 $\mu$ MAX	$\pm 1$
MAX552AEPA	-40°C to +85°C	8 Plastic DIP	$\pm 1/2$
MAX552BEPA	-40°C to +85°C	8 Plastic DIP	$\pm 1$
MAX552AEUB	-40°C to +85°C	10 $\mu$ MAX	$\pm 1/2$
MAX552BEUB	-40°C to +85°C	10 $\mu$ MAX	$\pm 1$

## Chip Information

TRANSISTOR COUNT: 887

SUBSTRATE CONNECTED TO  $V_{DD}$

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

12 Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

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