# SiT8009B

High Frequency, Low Power Oscillator

## Features

- 100% pin-to-pin drop-in replacement to quartz-based XO
- Excellent total frequency stability as low as ±20 ppm
- Operating temperature from -40°C to 85°C. For 125°C and/ or -55°C options, refer to SiT8919 and SiT8921
- Low power consumption of 4.9 mA typical at 1.8V
- Standby mode for longer battery life
- Fast startup time of 5 ms
- LVCMOS/HCMOS compatible output
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- Instant samples with Time Machine II and Field Programmable Oscillators
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free
- For AEC-Q100 oscillators, refer to SiT8924 and SiT8925

## Applications

- Ideal for GPON/EPON, network switches, routers, servers, embedded systems
- Ideal for Ethernet, PCI-E, DDR, etc.

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## Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

### Table 1. Electrical Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Range** | | | | | | |
| **Output Frequency Range** | f | 115 | – | 137 | MHz | |
| **Frequency Stability and Aging** | | | | | | |
| **Frequency Stability** | F_stab | -20 | – | +20 | ppm | Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load. |
| | | -25 | – | +25 | ppm | |
| | | -50 | – | +50 | ppm | |
| **Operating Temperature Range** | | | | | | |
| **Operating Temperature Range** | T_use | -20 | – | +70 | °C | Extended Commercial |
| | | -40 | – | +85 | °C | Industrial |
| **Supply Voltage and Current Consumption** | | | | | | |
| **Supply Voltage** | Vdd | 1.62 | 1.8 | 1.98 | V | Contact SiTime for 1.5V support |
| | | 2.25 | 2.5 | 2.75 | V | |
| | | 2.52 | 2.8 | 3.08 | V | |
| | | 2.7 | 3.0 | 3.3 | V | |
| | | 2.97 | 3.3 | 3.63 | V | |
| | | 2.25 | – | 3.63 | V | |
| **Current Consumption** | Idd | – | 6.2 | 7.5 | mA | No load condition, f = 125 MHz, Vdd = 2.8V, 3.0V, 3.3V or 2.25 to 3.63V |
| | | – | 5.5 | 6.4 | mA | No load condition, f = 125 MHz, Vdd = 2.5V |
| | | – | 4.9 | 5.6 | mA | No load condition, f = 125 MHz, Vdd = 1.8V |
| **OE Disable Current** | I_OD | – | – | 4.2 | mA | Vdd = 2.5V to 3.3V, OE = GND, Output in high-Z state |
| | | – | – | 4.0 | mA | Vdd = 1.8V, OE = GND, Output in high-Z state |
| **Standby Current** | I_std | – | 2.6 | 4.3 | µA | $\overline{ST}$ = GND, Vdd = 2.8V to 3.3V, Output is weakly pulled down |
| | | – | 1.4 | 2.5 | µA | $\overline{ST}$ = GND, Vdd = 2.5V, Output is weakly pulled down |
| | | – | 0.6 | 1.3 | µA | $\overline{ST}$ = GND, Vdd = 1.8V, Output is weakly pulled down |
| **LVCMOS Output Characteristics** | | | | | | |
| **Duty Cycle** | DC | 45 | – | 55 | % | All Vdds |
| **Rise/Fall Time** | Tr, Tf | – | 1 | 2 | ns | Vdd = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80% |
| | | – | 1.3 | 2.5 | ns | Vdd =1.8V, 20% - 80% |
| | | – | 0.8 | 2 | ns | Vdd = 2.25V - 3.63V, 20% - 80% |
| **Output High Voltage** | VOH | 90% | – | – | Vdd | IOH = -4 mA (Vdd = 3.0V or 3.3V) |
| **Output Low Voltage** | VOL | – | – | 10% | Vdd | IOL = 4 mA (Vdd = 3.0V or 3.3V) |

## Table 1. Electrical Characteristics (continued)

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Input Characteristics** | | | | | | |
| **Input High Voltage** | VIH | 70% | – | – | Vdd | Pin 1, OE or $\overline{ST}$ |
| **Input Low Voltage** | VIL | – | – | 30% | Vdd | Pin 1, OE or $\overline{ST}$ |
| **Input Pull-up Impedance** | Z_in | 50 | 87 | 150 | kΩ | Pin 1, OE logic high or logic low, or ST logic high |
| | | 2 | – | – | MΩ | Pin 1, $\overline{ST}$ logic low |
| **Startup and Resume Timing** | | | | | | |
| **Startup Time** | T_start | – | – | 5 | ms | Measured from the time Vdd reaches its rated minimum value |
| **Enable/Disable Time** | T_oe | – | – | 122 | ns | f = 137 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles |
| **Resume Time** | T_resume | – | – | 5 | ms | Measured from the time $\overline{ST}$ pin crosses 50% threshold |
| **Jitter** | | | | | | |
| **RMS Period Jitter** | T_jitt | – | 1.9 | 3 | ps | f = 125 MHz, Vdd = 2.5V, 2.8V, 3.0V or 3.3V |
| | | – | 1.8 | 4 | ps | f = 125 MHz, Vdd = 1.8V |
| **Peak-to-peak Period Jitter** | T_pk | – | 12 | 25 | ps | f = 125 MHz, Vdd = 2.5V, 2.8V, 3.0V or 3.3V |
| | | – | 14 | 30 | ps | f = 125 MHz, Vdd = 1.8V |
| **RMS Phase Jitter (random)** | T_phj | – | 0.5 | 0.9 | ps | Integration bandwidth = 900 kHz to 7.5 MHz |
| | | – | 1.3 | 2 | ps | Integration bandwidth = 12 kHz to 20 MHz |

## Table 2. Pin Description

| Pin | Symbol | | Functionality |
|---|---|---|---|
| 1 | OE/$\overline{ST}$/NC | Output Enable | H[1]: specified frequency output<br>L: output is high impedance. Only output driver is disabled. |
| | | Standby | H[1]: specified frequency output<br>L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std. |
| | | No Connect | Any voltage between 0 and Vdd or Open[1]: Specified frequency output. Pin 1 has no function. |
| 2 | GND | Power | Electrical ground |
| 3 | OUT | Output | Oscillator output |
| 4 | VDD | Power | Power supply voltage[2] |

**Top View**

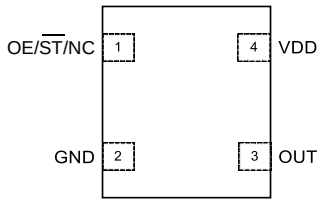



**Figure 1. Pin Assignments**

**Notes:**

1. In OE or $\overline{ST}$ mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
2. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

## Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| **Storage Temperature** | -65 | 150 | °C |
| **Vdd** | -0.5 | 4 | V |
| **Electrostatic Discharge** | – | 2000 | V |
| **Soldering Temperature (follow standard Pb free soldering guidelines)** | – | 260 | °C |
| **Junction Temperature[3]** | – | 150 | °C |

**Note:**

3. Exceeding this temperature for extended period of time may damage the device.

## Table 4. Thermal Consideration[4]

| Package | θJA, 4 Layer Board (°C/W) | θJA, 2 Layer Board (°C/W) | θJC, Bottom (°C/W) |
|---|---|---|---|
| 7050 | 142 | 273 | 30 |
| 5032 | 97 | 199 | 24 |
| 3225 | 109 | 212 | 27 |
| 2520 | 117 | 222 | 26 |
| 2016 | 152 | 252 | 36 |

**Note:**

4. Refer to JESD51 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

## Table 5. Maximum Operating Junction Temperature[5]

| Max Operating Temperature (ambient) | Maximum Operating Junction Temperature |
|---|---|
| 70°C | 80°C |
| 85°C | 95°C |

**Note:**

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

## Table 6. Environmental Compliance

| Parameter | Condition/Test Method |
|---|---|
| **Mechanical Shock** | **MIL-STD-883F, Method 2002** |
| **Mechanical Vibration** | **MIL-STD-883F, Method 2007** |
| **Temperature Cycle** | **JESD22, Method A104** |
| **Solderability** | **MIL-STD-883F, Method 2003** |
| **Moisture Sensitivity Level** | **MSL1 @ 260°C** |

## Test Circuit and Waveform[6]

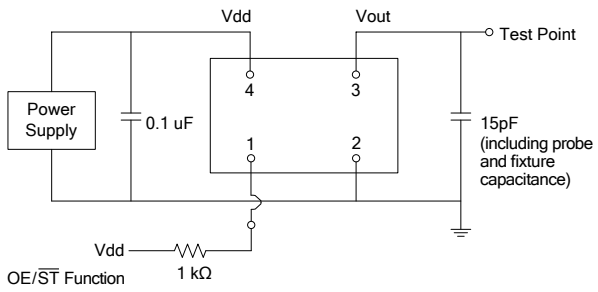



**Figure 2. Test Circuit**

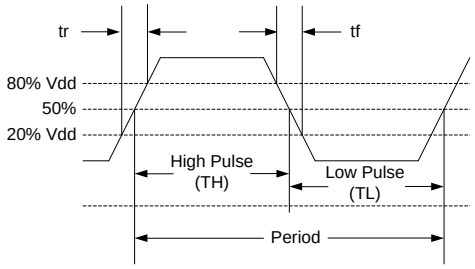



**Figure 3. Waveform**

**Note:**

6. Duty Cycle is computed as Duty Cycle = TH/Period.

## Timing Diagrams

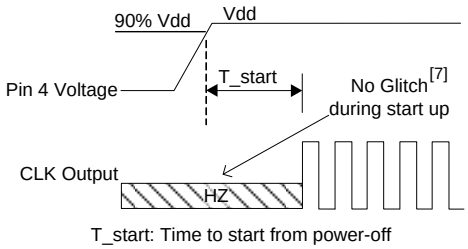



**Figure 4. Startup Timing (OE/ $\overline{ST}$ Mode)**

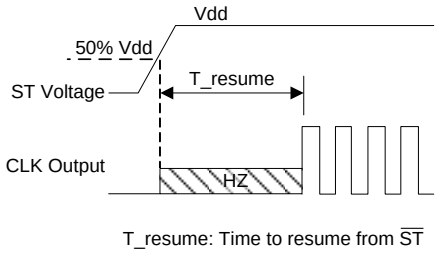



**Figure 5. Standby Resume Timing ( $\overline{ST}$ Mode Only)**

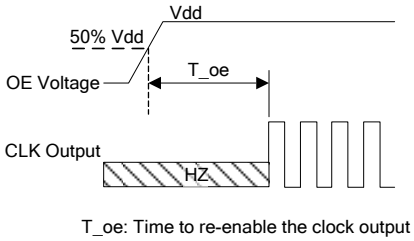



**Figure 6. OE Enable Timing (OE Mode Only)**

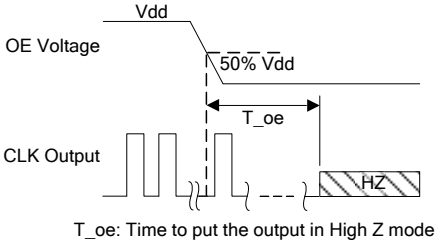



**Figure 7. OE Disable Timing (OE Mode Only)**

**Note:**

7. SiT8009 has “no runt” pulses and “no glitch” output during startup or resume.

## Performance Plots[8]

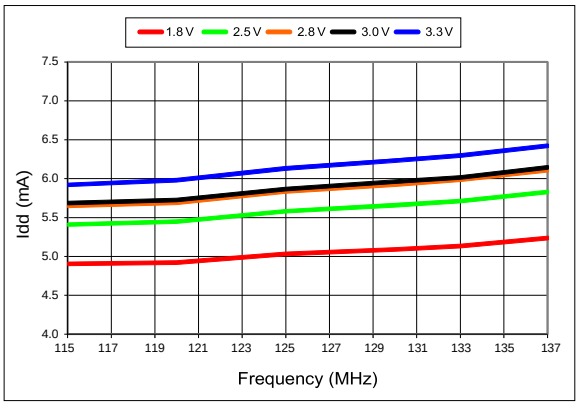



**Figure 8. Idd vs Frequency**

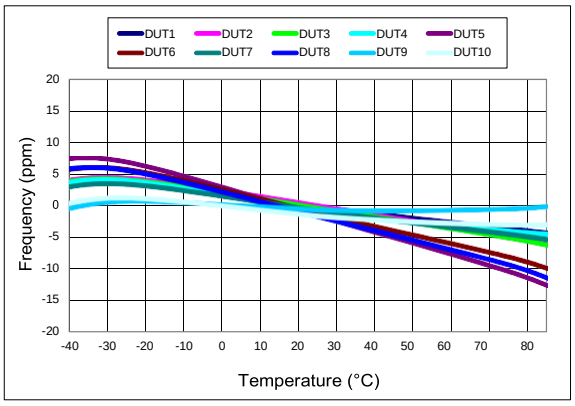



**Figure 9. Frequency vs Temperature, 1.8V**

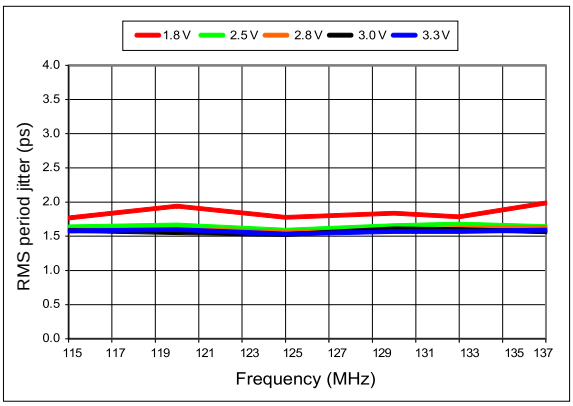



**Figure 10. RMS Period Jitter vs Frequency**

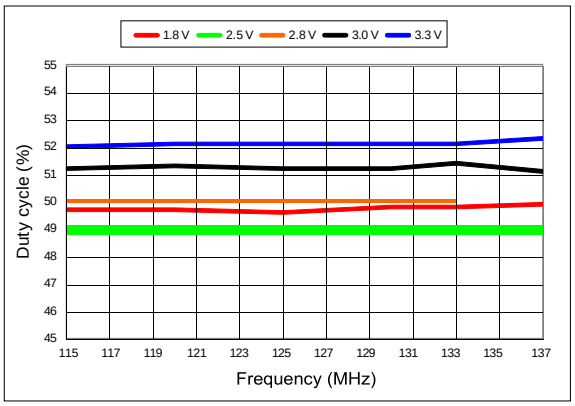



**Figure 11. Duty Cycle vs Frequency**

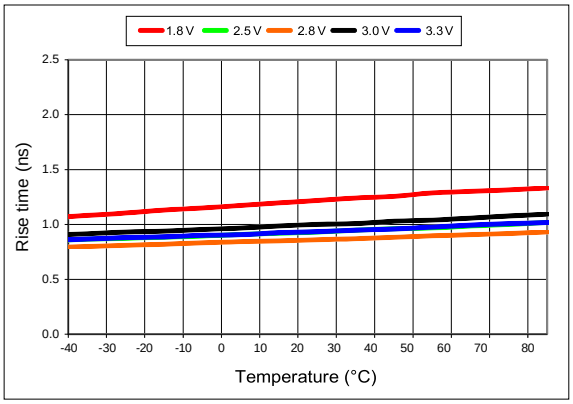



**Figure 12. 20%-80% Rise Time vs Temperature**

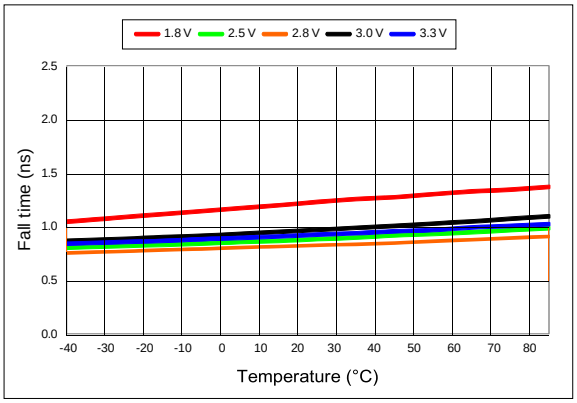



**Figure 13. 20%-80% Fall Time vs Temperature**

## Performance Plots[8]

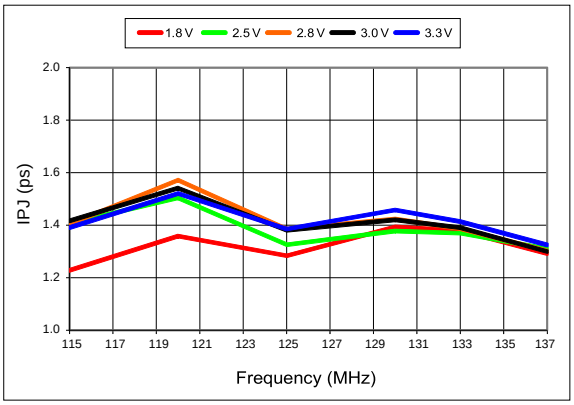



**Figure 14. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency[9]**

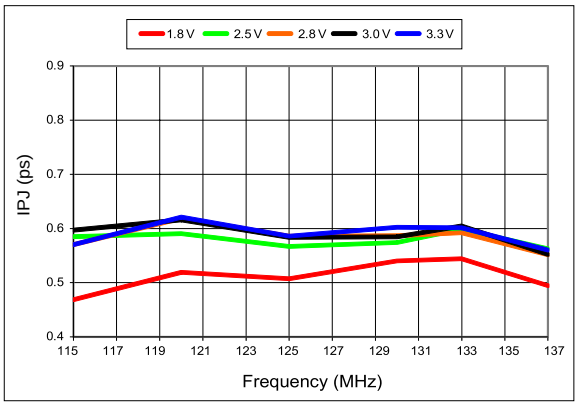



**Figure 15. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency[9]**

**Notes:**

8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
9. Phase noise plots are measured with Agilent E5052B signal source analyzer. Integration range is up to 5 MHz for carrier frequencies below 40 MHz.

## Programmable Drive Strength

The SiT8009 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Application Notes section.

### EMI Reduction by Slowing Rise/Fall Time

Figure 16 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11$^{th}$ clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

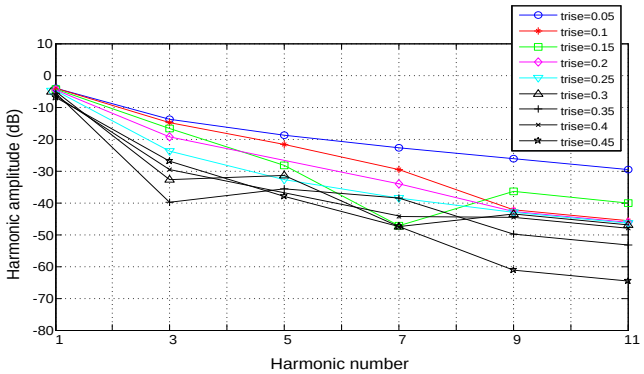



**Figure 16. Harmonic EMI reduction as a Function of Slower Rise/Fall Time**

### Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

### High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V SiT8009 device with default drive strength setting, the typical rise/fall time is 0.46 ns for 5 pF output load. The typical rise/fall time slows down to 1 ns when the output load increases to 15 pF. One can choose to speed up the rise/fall time to 0.72 ns by then increasing the driven strength setting on the SiT8009 to "F".

The SiT8009 can support up to 30 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Fall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

### SiT8009 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT8009 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

### Calculating Maximum Frequency

Based on the rise and fall time data given in Table 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf_20/80}}$$

where Trf_20/80 is the typical value for 20%-80% rise/fall time.

### Example 1

Calculate $f_{MAX}$ for the following condition:

- Vdd = 3.3V (Table 11)
- Capacitive Load: 30 pF
- Desired Tr/f time = 1.46 ns
  (rise/fall time part number code = U)

Part number for the above example:

SiT8009BI**U**12-33E-136.986300

Drive strength code is inserted here. Default setting is "-"

## Rise/Fall Time (20% to 80%) vs $C_{LOAD}$ Tables

### Table 7. Vdd = 1.8V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | |
|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF |
| T | 0.93 | n/ | n/a |
| E | 0.78 | n/ | n/a |
| U | 0.70 | 1.4 | n/a |
| F or "-": default | 0.65 | 1.3 | n/a |

### Table 8. Vdd = 2.5V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | |
|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF |
| R | 1.45 | n/a | n/a |
| B | 1.09 | n/a | n/a |
| T | 0.62 | 1.28 | n/a |
| E | 0.54 | 1.00 | n/a |
| U or "-": default | 0.43 | 0.96 | n/a |
| F | 0.34 | 0.88 | n/a |

### Table 9. Vdd = 2.8V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | |
|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF |
| R | 1.29 | n/a | n/a |
| B | 0.97 | n/a | n/a |
| T | 0.55 | 1.12 | n/a |
| E | 0.44 | 1.00 | n/a |
| U or "-": default | 0.34 | 0.88 | n/a |
| F | 0.29 | 0.81 | 1.48 |

### Table 10. Vdd = 3.0V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | |
|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF |
| R | 1.22 | n/a | n/a |
| B | 0.89 | n/a | n/a |
| T or "-": default | 0.51 | 1.00 | n/a |
| E | 0.38 | 0.92 | n/a |
| U | 0.30 | 0.83 | n/a |
| F | 0.27 | 0.76 | 1.39 |

### Table 11. Vdd = 3.3V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | |
|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF |
| R | 1.16 | n/a | n/a |
| B | 0.81 | n/a | n/a |
| T or "-": default | 0.46 | 1.00 | n/a |
| E | 0.33 | 0.87 | n/a |
| U | 0.28 | 0.79 | 1.46 |
| F | 0.25 | 0.72 | 1.31 |

**Note:**

10. "n/a" in Table 7 to Table 11 indicates that the resulting rise/fall time from the respective combination of the drive strength and output load does not provide rail-to-rail swing and is not available.

## Pin 1 Configuration Options (OE, $\overline{ST}$, or NC)

Pin 1 of the SiT8009 can be factory-programmed to support three modes: Output Enable (OE), standby ($\overline{ST}$) or No Connect (NC). These modes can also be programmed with the Time Machine using field programmable devices.

### Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1µs.

### Standby ($\overline{ST}$) Mode

In the $\overline{ST}$ mode, a device enters into the standby mode when Pin 1 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few µA. When $\overline{ST}$ is pulled High, the device goes through the "resume" process, which can take up to 5 ms.

### No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 1.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE, $\overline{ST}$, or NC mode.

### Table 12. OE vs. $\overline{ST}$ vs. NC

| | OE | $\overline{ST}$ | NC |
|---|---|---|---|
| Active current 125 MHz (max, 1.8V) | 5.6 mA | 5.6 mA | 5.6 mA |
| OE disable current (max. 1.8V) | 4.0 mA | N/A | N/A |
| Standby current (typical 1.8V) | N/A | 0.6 uA | N/A |
| OE enable time at 125 MHz (max) | 124 ns | N/A | N/A |
| Resume time from standby (max, all frequency) | N/A | 5 ms | N/A |
| Output driver in OE disable/standby mode | High Z | weak pull-down | N/A |

### Output on Startup and Resume

The SiT8009 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.

In addition, the SiT8009 has NO RUNT, NO GLITCH output during startup or resume as shown in the waveform captures in Figure 17 and Figure 18.

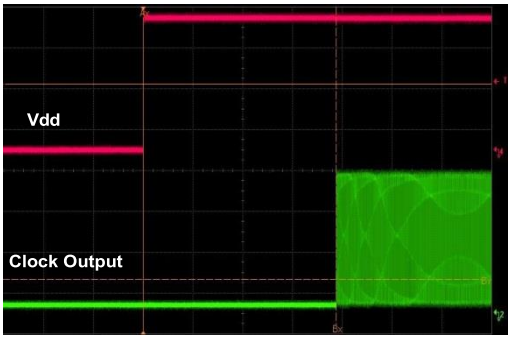



**Figure 17. Startup Waveform vs. Vdd**

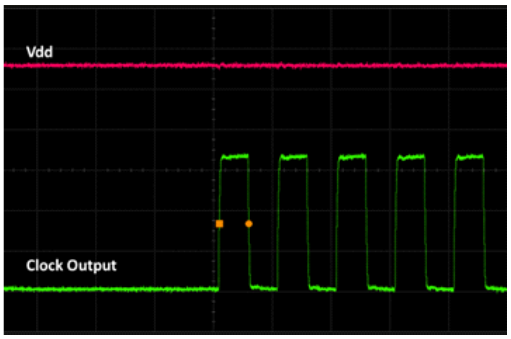



**Figure 18. Startup Waveform vs. Vdd (Zoomed-in View of Figure 17)**

## Instant Samples with Time Machine and Field Programmable Oscillators

SiTime supports a field programmable version of the SiT8009 high frequency, high temperature oscillator for fast prototyping and real time customization of features. The field programmable devices (FP devices) are available for all five standard SiT8009 package sizes and can be configured to one's exact specification using the Time Machine II, an USB powered MEMS oscillator programmer.

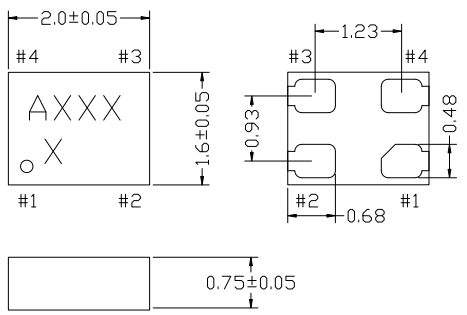
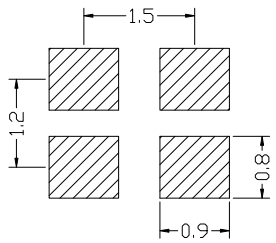
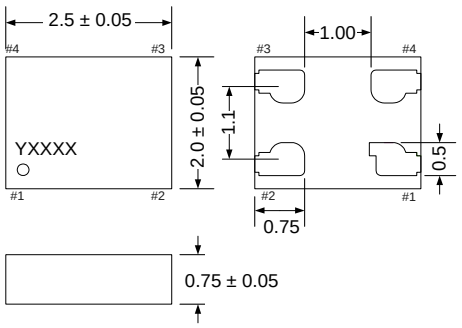
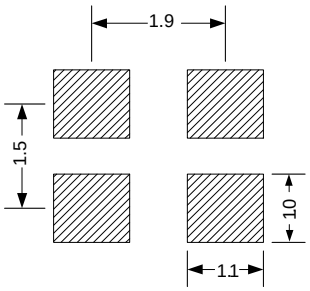
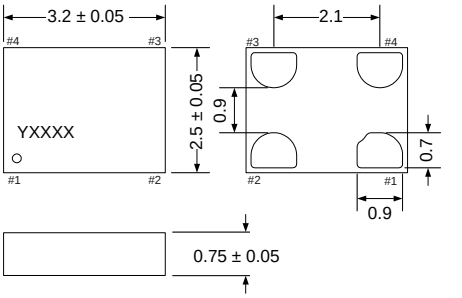
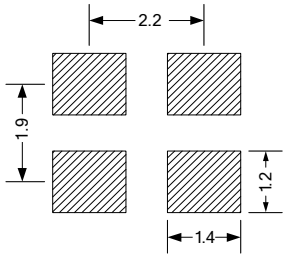
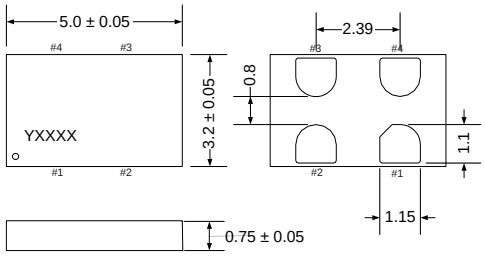
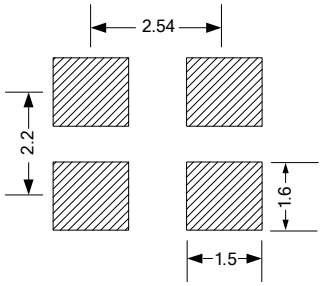
**Customizable Features of the SiT8009 FP Devices Include**

- Frequencies between 115 MHz – 137 MHz
- Three frequency stability options, ±20 ppm, ±25 ppm, ±50 ppm
- Two operating temperatures, -20 to 70°C or -40 to 85°C
- Six supply voltage options, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V and 2.25 to 3.63V continuous
- Output drive strength
- OE, $\overline{ST}$, or NC mode

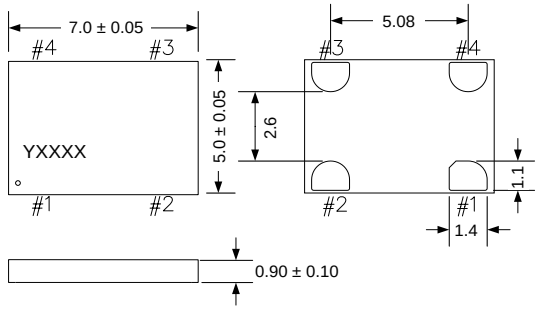
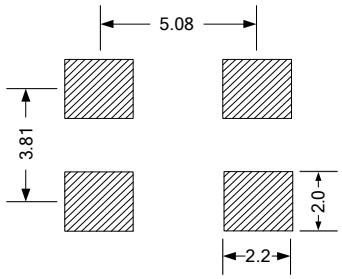
For more information regarding SiTime's field programmable solutions, see Time Machine II and Field Programmable Oscillators.

SiT8009 is factory-programmed per customer ordering codes for volume delivery.

## Dimensions and Patterns

| Package Size – Dimensions (Unit: mm)[11] | Recommended Land Pattern (Unit: mm)[12] |
|---|---|
| **2.0 x 1.6 x 0.75 mm**<br>  |  |
| **2.5 x 2.0 x 0.75 mm**<br>  |  |
| **3.2 x 2.5 x 0.75 mm**<br>  |  |
| **5.0 x 3.2 x 0.75 mm**<br>  |  |

## Dimensions and Patterns

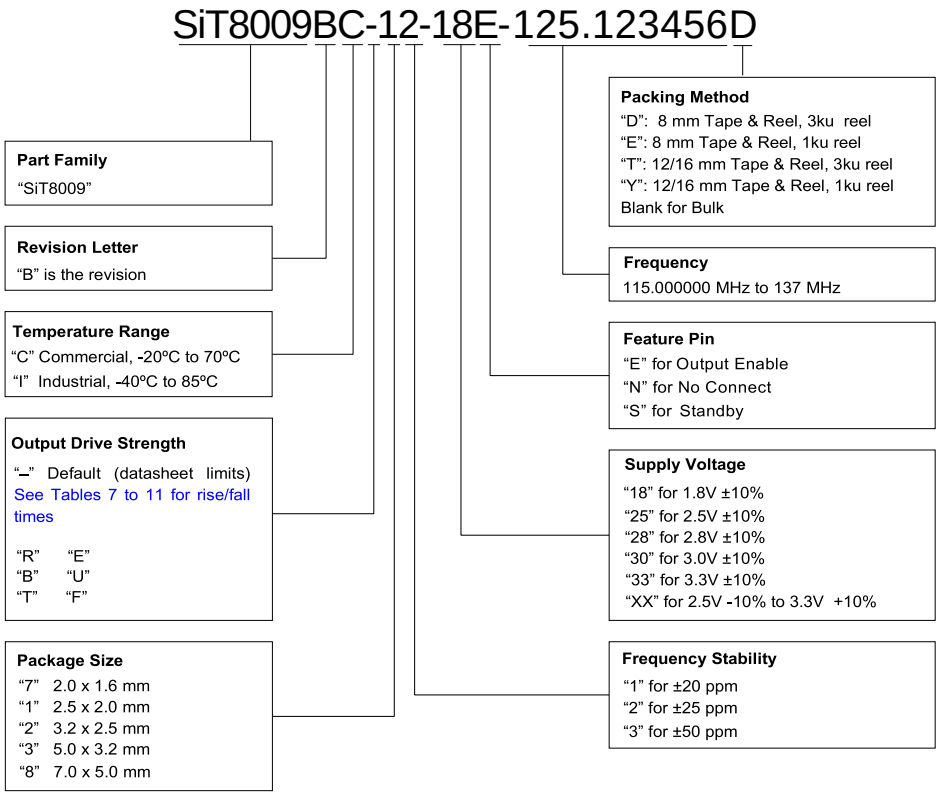
| Package Size – Dimensions (Unit: mm)[11] | Recommended Land Pattern (Unit: mm)[12] |
|---|---|
| **7.0 x 5.0 x 0.90 mm**<br>  <br> |  <br> |

**Notes:**

11. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
12. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

## Ordering Information

**The Part No. Guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator.**




### Table 13. Ordering Codes for Supported Tape & Reel Packing Method

| Device Size (mm x mm) | 16 mm T&R (3ku) | 16 mm T&R (1ku) | 12 mm T&R (3ku) | 12 mm T&R (1ku) | 8 mm T&R (3ku) | 8 mm T&R (1ku) |
|---|---|---|---|---|---|---|
| 2.0 x 1.6 | – | – | – | – | D | E |
| 2.5 x 2.0 | – | – | – | – | D | E |
| 3.2 x 2.5 | – | – | – | – | D | E |
| 5.0 x 3.2 | – | – | T | Y | – | – |
| 7.0 x 5.0 | T | Y | – | – | – | – |

## Table 14. Additional Information

| Document | Description | Download Link |
|---|---|---|
| **Time Machine II** | MEMS oscillator programmer | http://www.sitime.com/support/time-machine-oscillator-programmer |
| **Field Programmable Oscillators** | Devices that can be programmable in the field by Time Machine II | http://www.sitime.com/products/field-programmable-oscillators |
| **Manufacturing Notes** | Tape & Reel dimension, reflow profile and other manufacturing related info | http://www.sitime.com/manufacturing-notes |
| **Qualification Reports** | RoHS report, reliability reports, composition reports | http://www.sitime.com/support/quality-and-reliability |
| **Performance Reports** | Additional performance data such as phase noise, current consumption and jitter for selected frequencies | http://www.sitime.com/support/performance-measurement-report |
| **Termination Techniques** | Termination design recommendations | http://www.sitime.com/support/application-notes |
| **Layout Techniques** | Layout recommendations | http://www.sitime.com/support/application-notes |

## Table 15. Revision History

| Revision | Release Date | Change Summary |
|---|---|---|
| 1.0 | 06/10/2014 | Final production release |
| 1.01 | 05/07/2015 | Revised the Electrical Characteristics, Timing Diagrams and Performance Plots<br>Revised 2016 package diagram |
| 1.02 | 06/18/2015 | Added 16 mm T&R information to Table 13<br>Revised 12 mm T&R information to Table 13 |
| 1.03 | 08/30/2016 | Revised part number example in the ordering information |
| 1.04 | 01/30/2018 | Revised 2520 package land pattern<br>Updated logo and company address, other page layout changes |

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# Supplemental Information

The Supplemental Information section is not part of the datasheet and is for informational purposes only.

## Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, SiTime has in-house MEMS and analog CMOS expertise, which allows SiTime to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

### Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise

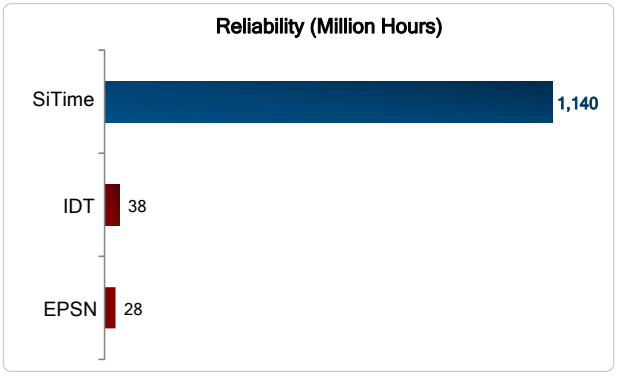


**Figure 1. Reliability Comparison[1]**

## Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new SiTime product specifies 10-year aging. A comparison is shown in Figure 2.

### Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

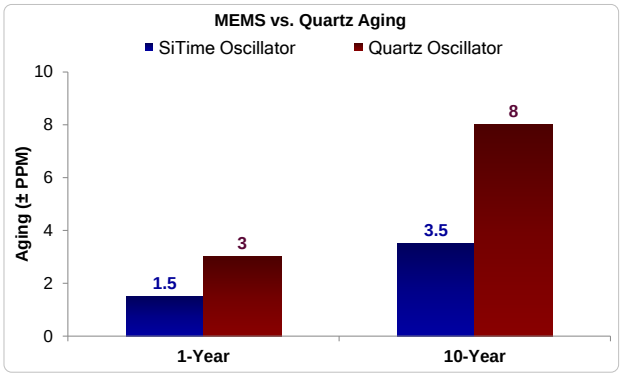


**Figure 2. Aging Comparison[2]**

## Best Electro Magnetic Susceptibility (EMS)

SiTime's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

### Why is SiTime Best in Class:

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

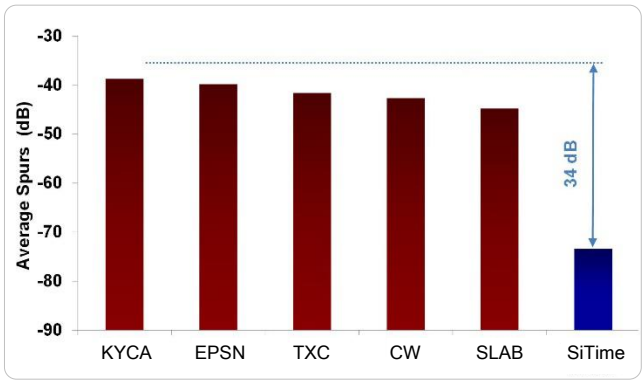


**Figure 3. Electro Magnetic Susceptibility (EMS)[3]**

## Best Power Supply Noise Rejection

SiTime's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

### Why is SiTime Best in Class:

- On-chip regulators and internal differential architecture for common mode noise rejection
- MEMS resonator is paired with advanced analog CMOS IC

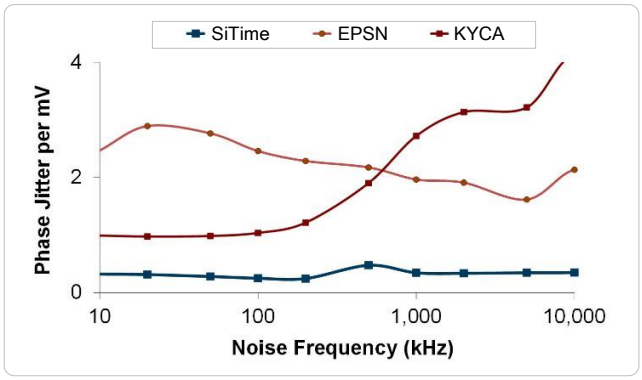


**Figure 4. Power Supply Noise Rejection[4]**

## Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

### Why is SiTime Best in Class:

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

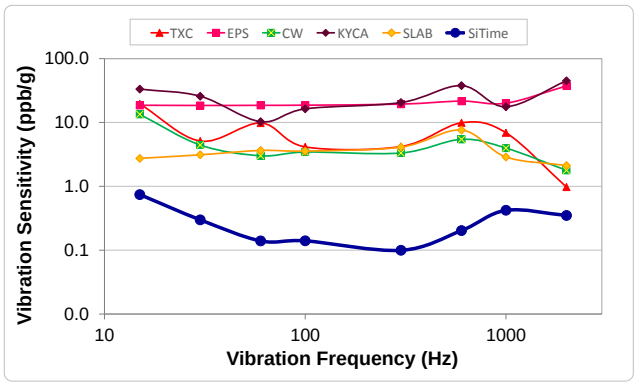


**Figure 5. Vibration Robustness[5]**

**Figure labels:**

- TXC = TXC
- Epson = EPSN
- Connor Winfield = CW
- Kyocera = KYCA
- SiLabs = SLAB
- SiTime = EpiSeal MEMS

## Best Shock Robustness

SiTime's oscillators can withstand at least 50,000 *g* shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

### Why is SiTime Best in Class:

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

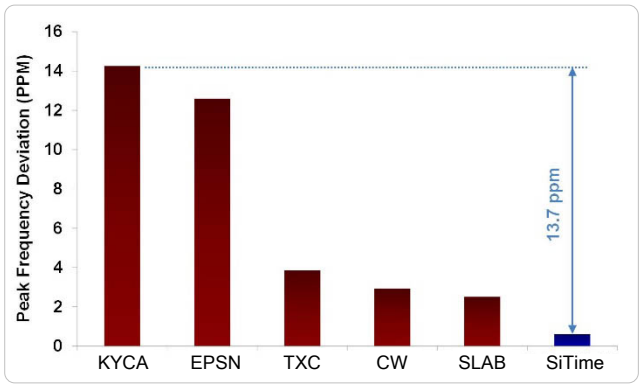


**Figure 6. Shock Robustness[6]**

**Notes:**

1. Data source: Reliability documents of named companies.
2. Data source: SiTime and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
   - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
   - Field strength: 3V/m
   - Radiated signal modulation: AM 1 kHz at 80% depth
   - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
   - Antenna polarization: Vertical
   - DUT position: Center aligned to antenna

   **Devices used in this test:**

| Label | Manufacturer | Part Number | Technology |
|---|---|---|---|
| EpiSeal MEMS | SiTime | SiT9120AC-1D2-33E156.250000 | MEMS + PLL |
| EPSN | Epson | EG-2102CA156.2500M-PHPAL3 | Quartz, SAW |
| TXC | TXC | BB-156.250MBE-T | Quartz, 3rd Overtone |
| CW | Conner Winfield | P123-156.25M | Quartz, 3rd Overtone |
| KYCA | AVX Kyocera | KC7050T156.250P30E00 | Quartz, SAW |
| SLAB | SiLab | 590AB-BDG | Quartz, 3rd Overtone + PLL |

4. 50 mV pk-pk Sinusoidal voltage.

   **Devices used in this test:**

| Label | Manufacturer | Part Number | Technology |
|---|---|---|---|
| EpiSeal MEMS | SiTime | SiT8208AI-33-33E-25.000000 | MEMS + PLL |
| NDK | NDK | NZ2523SB-25.6M | Quartz |
| KYCA | AVX Kyocera | KC2016B25M0C1GE00 | Quartz |
| EPSN | Epson | SG-310SCF-25M0-MB3 | Quartz |

5. Devices used in this test:
   same as EMS test stated in Note 3.
6. Test conditions for shock test:
   - MIL-STD-883F Method 2002
   - Condition A: half sine wave shock pulse, 500-g, 1ms
   - Continuous frequency measurement in 100 µs gate time for 10 seconds

   **Devices used in this test:**
   same as EMS test stated in Note 3.
7. Additional data, including setup and detailed results, is available upon request to qualified customer. Please contact productsupport@sitime.com.