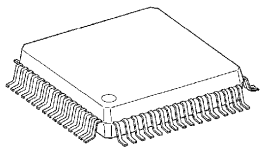
CMOS 8-Bit Microcontroller

TMP86CH72FG/TMP86CM72FG

TMP86CH72/CM72 is a low-power, high-speed and high-performance 8-bit single chip microcomputer, including large capacity ROM/RAM, input/output ports, multiple timer/counter, serial interface, 8-bit AD converter and VFT (Vacume Fluorescent Tube) driver.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CH72FG	16K × 8 bits	1 K × 8 bits	P-QFP64-1414-0.80C	TMP86PM72FG
TMP86CM72FG	32 K × 8 bits	1 K × 8 bits		

P-QFP64-1414-0.80C



TMP86CH72FG
TMP86CM72FG

Features

- 8-bit single chip microcomputer TLCS-870/C series
- Minimum instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 731 basic machine instructions: 132 types
- 19 interrupt sources (External: 6, Internal: 13)
- Input/output ports: 54 pins
- 16-bit timer counters: 1 channels
  - TC2: Timer, Event counter,Window modes
- 8-bit timer counters: 2 channels
  - TC3: Timer, Event counter, Capture modes (Pulse width/duty measurement).
  - TC4: Timer, Event counter, PWM (Pulse width modulation) Output , PDO (Programmable Divider Output)

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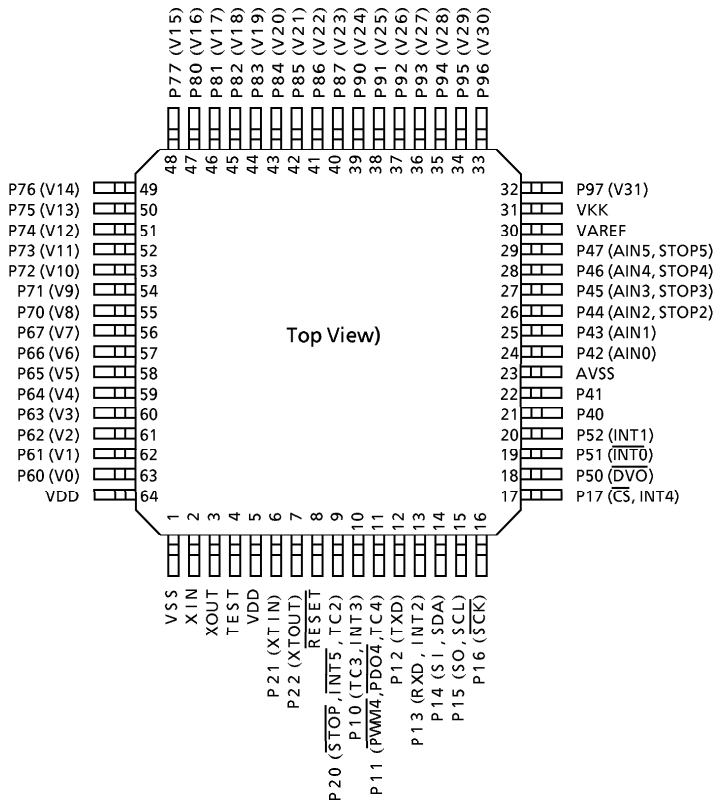
- Time base timer
- Watchdog timer
  - Interrupt source
- Divider output function
- 4 key-on wakeup pins
- Serial interface
  - 8-bit SIO: 1 channel (with 32 bytes buffer)
  - I^2C bus: 1 channel
  - 8-bit UART: 1 channel
- 8-bit successive approximation type AD converter
  - Analog input: 8 channels
- Vacume flouorescent tube driver (Automatic display)
  - Programmable grid scan
  - High breakdown voltage ports (Max 41 V × 32 bits)
- ROM corrective function
- Low-consumption power (9 modes)
  - STOP mode: Oscillation stop (Battery/capacitor back-up).
  - SLOW1 mode: Low consumption power operation by low-frequency clock (High-frequency clock stop.)
  - SLOW2 mode: Low consumption power operation by low-frequency clock (High-frequency clock oscillate.)
  - IDLE0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - IDLE1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE2 mode: CPU stops, and peripherals operate using high and low-frequency clock. Release by interrupts.
  - SLLEP0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - SLEEP1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP2 mode: CPU stops, and peripherals operate using high and low-frequency clock. Release by interrupts.
- Dual clock operation
  - Single/dual-clock mode
- Wide operating voltage: 4.5 V to 5.5 V at 16 MHz/32.768 kHz
  2.7 V to 5.5 V at 8 MHz/32.768 kHz

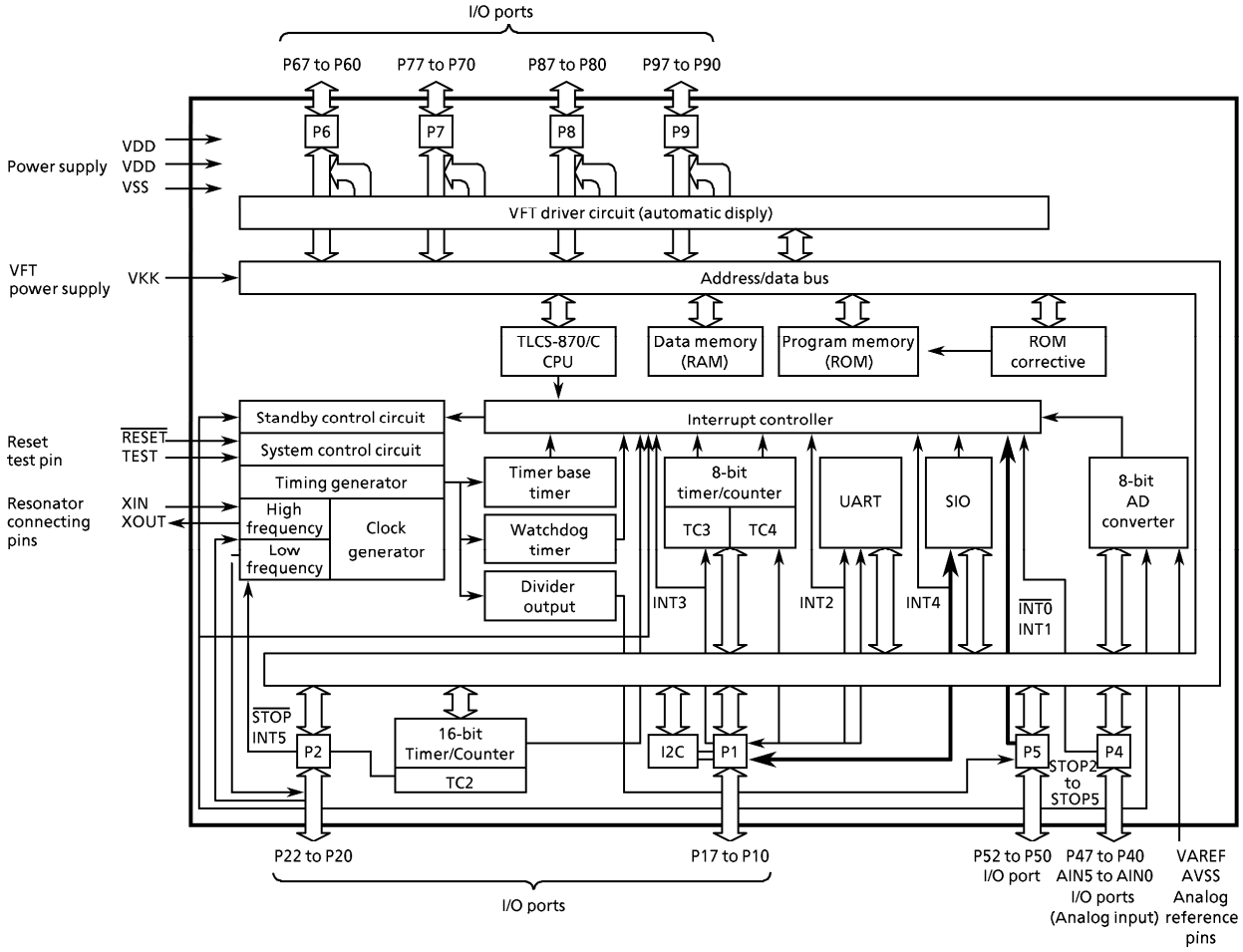
Pin Assignments (Top view)

P-QFP64-1414-0.80C



Note: All VDD terminals are connected externally.

Block Diagram



Pin Functions (1/2)

Pin Name	I/O	Functions	
P10(TC3/INT3)	I/O (Input)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control. When used as serial data input, external interrupt input, timer/counter input, the input mode is configured. When used as PWM output, PDO output , PPG output, serial data output, serial clock output, the latch must be set to "1" and the output mode is configured. When used as open-drain port, P1OUTCR set to "0". When used as CMOS port, P1OUTCR set to "1".	Timer/counter input External interrupt input
P11 (PWM4/PDO4/TC4)	I/O (Output/Output/Input)		PWM output PDO output Timer/counter input
P12 (TXD)	I/O (Output)		UART data output
P13 (RXD/INT2)	I/O (Input)		UART data input External interrupt input
P14 (SI/SDA)	I/O (Input)		SIO data input I^2C bus data
P15 (SO/SCL)	I/O (Output)		SIO data output I^2C bus clock
P16 ($\overline{SCK}$)	I/O (I/O)		SIO clock I/O
P17 ($\overline{CS}$/INT4)	I/O (Input)		SIO chip select input External interrupt input
P20 (STOP/INT5/TC2)	I/O (Input)	8-bit I/O port. When use as input port, external interrupt input, and STOP mode release signal input, the latch must be set to "1".	External interrupt input STOP mode release signal input Timer/counter input
P21 (XTIN)	I/O (Input)		Resonator connecting pins for low-frequency clock. For inputting external clock, XTIN is used and XTOUT is opened.
P22 (XTOUT)	I/O (Output)		
P40	I/O	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control. When use as analog input, then must be set to "1".	High current output
P41			
P42 (AIN0)	I/O (Input)		AD converter analog input
P43 (AIN1)			
P44 (AIN2/STOP2)	I/O (Input)		AD converter analog input STOP mode release signal Input
P45 (AIN3/STOP3)			
P46 (AIN4/STOP4)			
P47 (AIN5/STOP5)			
P50 (DVO)	I/O (Output)	3-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	Divider output
P51 (INT0)	I/O (Input)		External interrupt input
P52 (INT1)	I/O (Input)		External interrupt input
P60 (V0)	I/O (Output)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	Grid output
P61 (V1)			
P62 (V2)			
P63 (V3)			
P64 (V4)			
P65 (V5)			
P66 (V6)			
P67 (V7)			

Pin Functions (2/2)

Pin Name	I/O	Functions	
P70 (V8)	I/O (Output)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	Grid output
P71 (V9)			
P72 (V10)			
P73 (V11)			
P74 (V12)			
P75 (V13)			
P76 (V14)			
P77 (V15)			
P80 (V16)	I/O (Output)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	Segment output
P81 (V17)			
P82 (V18)			
P83 (V19)			
P84 (V20)			
P85 (V21)			
P86 (V22)			
P87 (V23)			
P90 (V24)	I/O (Output)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control.	Segment output
P91 (V25)			
P92 (V26)			
P93 (V27)			
P94 (V28)			
P95 (V29)			
P96 (V30)			
P97 (V31)			
TEST	Input	Test pin for out-going test. Be fixed to low.	
RESET	I/O	–	
XIN	Input	Resonator connecting pins for high-frequency clock. For inputting external clock, XTIN is used and XTOUT is opened.	
XOUT	Output		
VSS	Power Supply	0.0 [V] (GND)	
VDD		+ 5 [V]	
AVSS		GND0.0 [V]	
VAREF		Analog reference voltage input	
VKK		VFT driver power supply	

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The memory of TMP86CH72/CM72 consists of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64 Kbyte address space.Figure 1-1 shows the memory address map of TMP86CH72/CM72. The general-purpose registers are not assigned to the RAM address space.

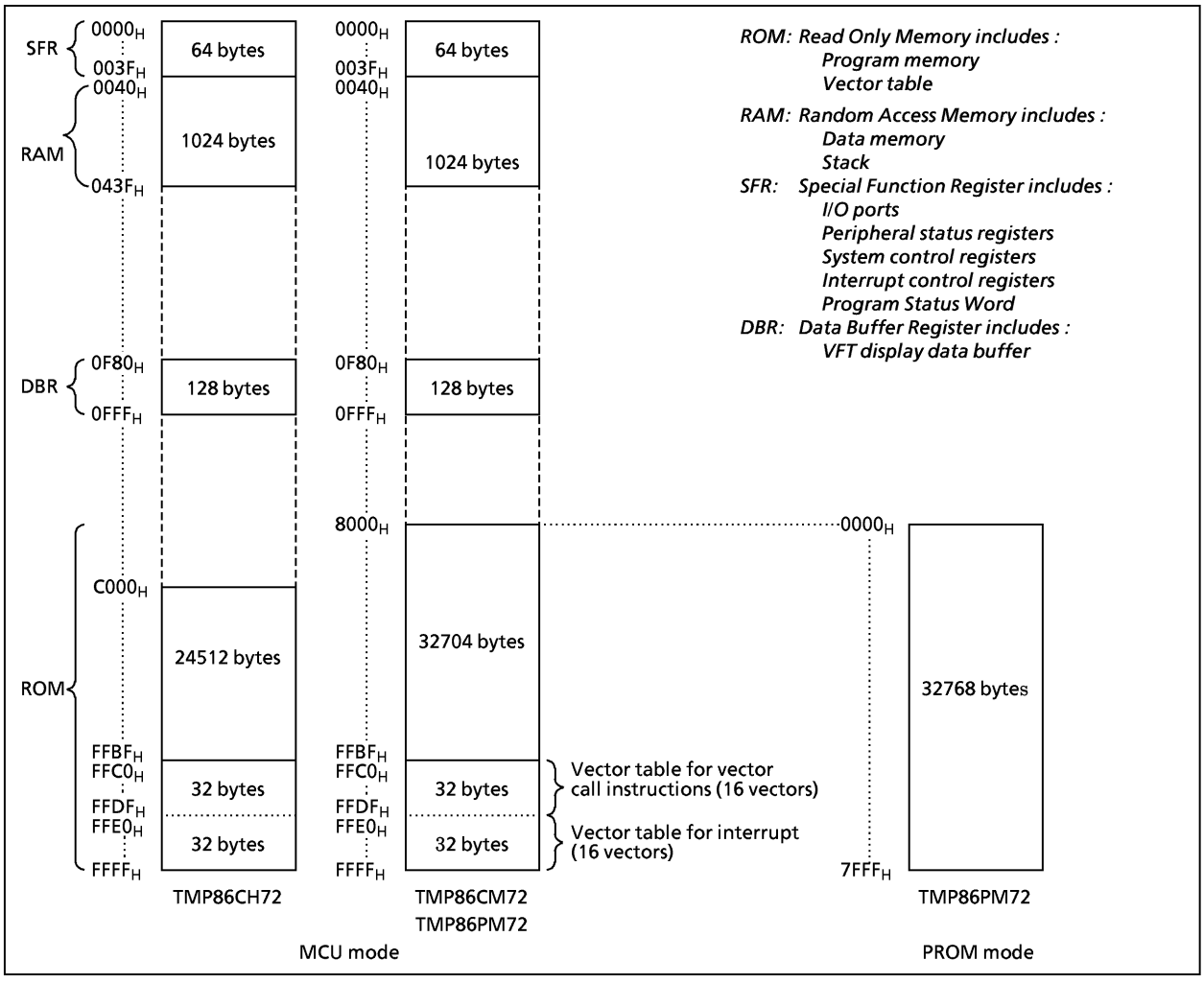


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86CH72 has an 16 K×8 bits (Address $C000_H$ to $FFFF_H$) of program memory, the TMP86CM72 has 32 K×8 bits (Address 8000_H to $FFFF_H$) of program memory (Mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

Electrical Characteristics

Absolute Maximum Ratings (VSS = 0 V)

Parameter		Symbol	Pins	Ratings	Unit
Supply voltage		V_{DD}		– 0.3 to 6.5	V
Program voltage		V_{PP}	TEST/VPP pin	– 0.3 to 13.0	
Input voltage		V_{IN}		– 0.3 to V_{DD} + 0.3	
Output voltage		V_{OUT1}		– 0.3 to V_{DD} + 0.3	
		V_{OUT2}	Source open drain port	V_{DD} – 41 to V_{DD} + 0.3	
Output current (Per 1 pin)	IOL	I_{OUT1}	P0, P01, P2, P4 (P43~P47), P5 ports	5	mA
		I_{OUT2}	P4 (P40, P41) port	40	
	IOH	I_{OUT3}	P1, P4, P5 ports	– 3	
		I_{OUT4}	P6, P7 ports	– 30	
		I_{OUT5}	P8, P9 ports	– 20	
Output current (Total)	IOL	ΣI_{OUT1}	P1, P2, P4, P5 ports	120	mA
	IOH	ΣI_{OUT4}	P6, P7, P8, P9 ports	– 120	
Power dissipation [Topr = 25°C]		PD		1200	mW
Soldering temperture (time)		Tsld		260 (10 s)	°C
Storage temperature		Tstg		– 55 to 125	
Operating temperature		Topr		– 30 to 70	

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum ratings is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products, which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: All VDDs should be connected externally for keeping the same voltage level.

Note 3: Power Dissipation (PD): For PD, it is necessary to decrease – 11.5 mW/°C.

How to Calculate Power Consumption

The share of VFT driver loss (VFT driver output loss + pull-down resistor (RK) loss) in power consumption Pmax of TMP86CH72/CM72 is high. When using a fluorescent display tube with a large number of segments, the maximum power consumption PD must not be exceeded.
Power consumption Pmax = Operating power consumption + Normal output port loss + VFT driver loss.

Where,

Operating power consumption: VDD × IDD
Normal output port loss : $\Sigma I_{OUT1} \times 0.4$
VFT driver loss : VFT driver output loss + pull-down resistor (RK) loss

Example :
When Ta = −10 to 50 °C (When using a fluorescent display tube with a conventional type which can use only one grid output at the same time.) and a fluorescent display tube with segment output = 3 mA, digit output = 12 mA, Vkk = −34.5 V is used.
Operating conditions ; VDD = 5 V ± 10%, fc = 8 MHz, VFT dimmer time (DIM) = (14/16) × tseg,

Power consumption Pmax = (1) + (2) + (3)
Where,
(1) Operating power consumption: $V_{DD} \times I_{DD} = 5.5\ V \times 10\ mA = 55\ mW$
(2) Normal output port loss : $\Sigma I_{OUT2} \times 0.4 = 60\ mA \times 0.4\ V = 24\ mW$
(3) VFT driver loss : Segment pin = 3 mA × 2 V × Number of segments X = 6 mW × X
Grid pin = 12 mA × 2 V × 14/16 (DIM) × Number of grids Y
= 21 mW × Y
Rk loss = $(5.5\ V + 34.5\ V)^2/50\ k\Omega$ × (Number of segments X + Number of grids Y) = 32 mW × (X + Y)

Therefore, Pmax = 55 mW + 24 mW + 6 mW × X + 21 mW × Y + 32 mW × (X + Y)
= 132 mW + 38 mWX···

Maximum power consumption PD when Ta = 50 °C is determined by the following equation;
PD = 1200 mW − (11.5 × 25) = 912.5 mW

The number of segments X that can be lit is:
PD > Pmax
912.5 mW > 132 + 38 X
20.53 > X

Thus, a fluorescent display tube with less than 20 segments can be used. If a fluorescent display tube with 20 segments or more is used, the number of segments to be lit must be kept to less than 20 by software.

Recommended Operating Conditions

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply voltage	V_{DD}		fc = 16 MHz	NORMAL1/2 modes	4.5	5.5	V
				IDLE1/2 modes			
			fc = 8 MHz	NORMAL1/2 modes	2.7		
				IDLE1/2 modes			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode			
Output voltage	V_{OUT3}	Source open drain pins			V_{DD} – 38	V_{DD}	
Input high voltage	V_{IH1}	Except hysteresis input			$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
Input low voltage	V_{IL1}	Except hysteresis input			0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
Clock frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.5 V		1.0	8.0	MHz
			V_{DD} = 4.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note : The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products, which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (V_{DD} = 5 V)

[Condition] V_{DD} = 5.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = − 30 to 70°C
(Typ. : V_{DD} = 5.0 V, Topr = 25°C, Vin = 5.0 V/0V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input			–	0.9	–	V
Input current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5V /0 V		–	–	± 2	μA
	I_{IN2}	Sink open-drain, Tri-st						
	I_{IN3}	RESET, STOP						
Input resistance	R_{IN}	RESET Pull-up			100	220	450	kΩ
Pull-down resistance (Note 4)	R_K	Source open drain	V_{DD} = 5.5 V, V_{KK} = − 30 V		50	80	120	
Output leakage current	I_{LO1}	Sink open-drain, Tri-st	V_{DD} = 5.5 V, V_{OUT} = 5.5 V		–	–	± 2	μA
	I_{LO2}	Source open-drain	V_{DD} = 5.5 V, V_{KK} = − 32 V		–	–	± 2	
Output high voltage	V_{OH}	Tri-st	V_{DD} = 4.5 V, I_{OH} = − 0.7 mA		4.1	–	–	V
Output low voltage	V_{OL1}	Except XOUT (P40, P41)	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		–	–	0.4	
Output high current	I_{OH1}	P6, P7	V_{DD} = 4.5 V, V_{OH} = 2.4 V		− 18	− 28	–	mA
	I_{OH2}	P8, P9, PD	V_{DD} = 4.5 V, V_{OH} = 2.4 V		− 9	− 14	–	
Output low current	I_{OL}	High-current (P40, P41)	V_{DD} = 4.5 V, V_{OL} = 1.0 V		–	20	–	
Supply current in NORMAL1/2 modes	I_{DD}		fc = 16.0 MHz fs = 32.768 KHz	AD converter Disable (IREF off)	–	12	18	
			fc = 8.0 MHz fs = 32.768 KHz		–	6	9	
Supply current in IDLE0/1/2 modes			fc = 16.0 MHz fs = 32.768 KHz		–	6	9	
			fc = 8.0 MHz fs = 32.768 KHz		–	3	4.5	
Supply current in NORMAL1/2 modes			fc = 16.0 MHz fs = 32.768 KHz	AD converter Enable	–	13	19	
			fc = 8.0 MHz fs = 32.768 KHz		–	7	10	
Supply current in STOP mode			T_{opr} = to 50 ℃	AD converter Disable	–	0.5	5	μA
			T_{opr} = to 70 ℃				10	

Note 1 : Typical values show those at T_{opr} = 25°C, V_{DD} = 5 V.
Note 2 : Input current (I_{IN1}, I_{IN3}): The current through pull-up or pull-down resistor is not included.
Note 3 : IDD does not include IREF current.
Note 4: T_{opr} = − 10°C to 70°C

DC Characteristics (V_{DD} = 3 V)

[Condition] V_{DD} = 3.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = − 30 to 70°C
(Typ. : V_{DD} = 3.0 V, Topr = 25°C, Vin = 3.0 V/0V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input			–	0.4	–	V
Input current	I_{IN1}	TEST	V_{DD} = 3.3 V, V_{IN} = 3.3 V/0 V		–	–	± 2	μA
	I_{IN2}	Sink open-drain, Tri-st						
	I_{IN3}	RESET, STOP						
Input resistance	R_{IN}	RESET Pull-up			100	220	450	kΩ
Pull-down resistance (Note 5)	R_K	Source open drain	V_{DD} = 3.3 V, V_{KK} = − 30 V		45	75	115	
Output leakage current	I_{LO1}	Sink open-drain, Tr-st	V_{DD} = 3.3 V, V_{OUT} = 3.3 V/0 V		–	–	± 2	μA
	I_{LO2}	Source open-drain	V_{DD} = 3.3 V, V_{KK} = − 32 V		–	–	± 2	
Output high voltage	V_{OH}	Tri-st	V_{DD} = 2.7 V, I_{OH} = − 0.6 mA		2.3	–	–	V
Output low voltage	V_{OL1}	Except XOUT (P40, P41)	V_{DD} = 2.7 V, I_{OL} = 0.9 mA		–	–	0.4	
Output high current	I_{OH1}	P6, P7	V_{DD} = 2.7 V, V_{OH} = 1.5 V		− 5.5	− 8	–	mA
	I_{OH2}	P8, P9, PD	V_{DD} = 2.7 V, V_{OH} = 1.5 V		− 3	− 4.5	–	
Output low current	I_{OL}	High-current (P40, P41)	V_{DD} = 2.7 V, V_{OL} = 1.0 V		–	6	–	
Supply current in NORMAL1/2 modes	I_{DD}		fc = 8.0 MHz fs = 32.768 KHz	AD converter Disable (IREF off)	–	3	4.5	
Supply current in IDLE0/1/2 modes			fc = 8.0 MHz fs = 32.768 KHz		–	2	2.5	
Supply current in NORMAL1/2 modes			fc = 8.0 MHz fs = 32.768 KHz	AD converter Enable	–	3.5	5	
Supply current in SLOW1/2 modes			fs = 32.768 KHz	AD converter Disable	–	3	60	μA
Supply current in SLEEP0/1/2 modes					–	15	30	
Supply current in STOP mode			T_{opr} = to 50 ℃		–	0.5	5	
			T_{opr} = to 70 ℃				10	

Note 1 : Typical values show those at T_{opr} = 25°C, V_{DD} = 3 V.
Note 2 : Input current (I_{IN1}, I_{IN3}) ; The current through pull-up or pull-down resistor is not included.
Note 3 : IDD does not include IREF current.
Note 4 : The supply currents of SLOW2 and SLEEP2 modes are equivalent to IDLE0, 1, 2.
Note 5: T_{opr} = − 10°C to 70°C

AD Characteristics

(V_{SS} = A_{VSS} = 0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = − 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		V_{DD} − 1.5	−	V_{DD}	V
Analog reerence voltage range	$\triangle V_{AREF}$		3.0	−	−	
Analog input voltage	V_{AIN}		0	−	V_{AREF}	V
Analog supply current	I_{REF}	V_{DD} = V_{AREF} = 5.5 V, V_{SS} = 0.0 V	−	0.6	1.0	mA
Non linearity error		V_{DD} = V_{AREF} = 4.5 to 5.5V, V_{SS} = 0 V	−	−	± 1	LSB
Zero point error			−	−	± 1	
Full scale error			−	−	± 1	
Total error			−	−	± 2	

(V_{SS} = A_{VSS} = 0 V, 2.7 V ≦ V_{DD} < 4.5 V, Topr = − 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		V_{DD} − 1.5	−	V_{DD}	V
Analog reerence voltage range	$\triangle V_{AREF}$		2.5	−	−	
Analog input voltage	V_{AIN}		0	−	V_{AREF}	V
Analog supply current	I_{REF}	V_{DD} = V_{AREF} = 4.5 V, V_{SS} = 0.0 V	−	0.5	0.8	mA
Non linearity error		V_{DD} = V_{AREF} = 2.7 to 4.5V, V_{SS} = 0 V	−	−	± 1	LSB
Zero point error			−	−	± 1	
Full scale error			−	−	± 1	
Total error			−	−	± 2	

Note 1 : Total errors includes all errors, except quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2 : Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.11.2 Register Configuration".

Note 3 : Please use input voltage to AIN input pin in limit of V_{AREF} − V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4 : Analog Reference Voltage Range: $\triangle V_{AREF}$ = V_{AREF} − V_{SS}

AC Characteristics

(V_{SS} = 0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine cycle time	tcyc	NORMAL1/2 modes	0.25	–	4	μs
		IDLE0/1/2 modes				
		SLOW1/2 modes	117.6	–	133.3	
		SLEEP0/1/2 modes				
High level clock pulse width	twcH	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

(V_{SS} = 0 V, 2.7 V ≦ V_{DD} ≦ 4.5 V, Topr = – 30 to 70°C)

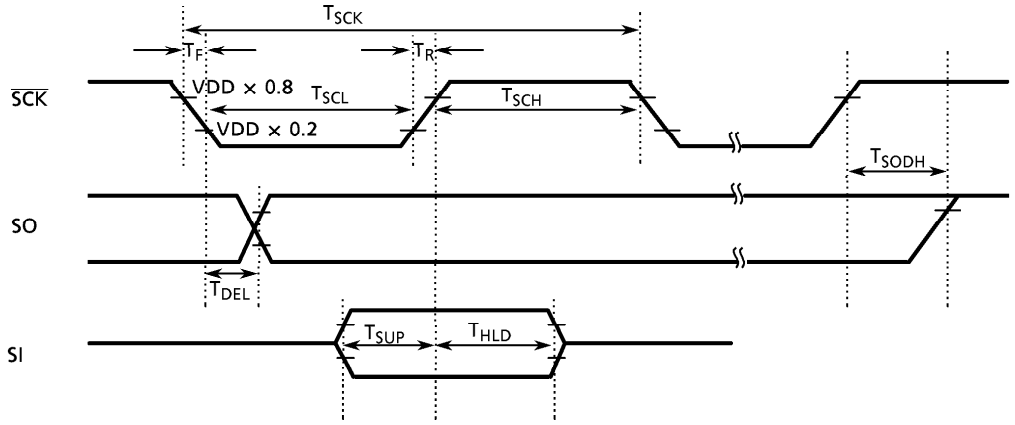
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine cycle time	tcyc	NORMAL1/2 mode	0.5	–	8	μs
		IDLE0/1/2 mode				
		SLOW1/2 mode	117.6	–	133.3	
		SLEEP0/1/2 mode				
High level clock pulse width	twcH	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

HSIO AC Characteristics (V_{SS} = 0 V, 2.7 V ≦ V_{DD} ≦ 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
$\overline{SCK}$ output period (internal clock)	T_{SCK1}	8 MHz < fc ≦ 16 MHz V_{DD} = 4.5 V to 5.5 V	16/fc	–	–	s
$\overline{SCK}$ output low width (internal clock)	T_{SCL1}		8/fc – 100ns	–	–	
$\overline{SCK}$ output high width (internal clock)	T_{SCH1}		8/fc – 100ns	–	–	
$\overline{SCK}$ output period (internal clock)	T_{SCK2}	4 MHz < fc ≦ 8 MHz V_{DD} = 2.7 V to 5.5 V	8/fc	–	–	
$\overline{SCK}$ output low width (internal clock)	T_{SCL2}		4/fc – 100ns	–	–	
$\overline{SCK}$ output high width (internal clock)	T_{SCH2}		4/fc – 100ns	–	–	
$\overline{SCK}$ output period (internal clock)	T_{SCK3}	fc ≦ 4 MHz V_{DD} = 2.7 V to 5.5 V	4/fc	–	–	
$\overline{SCK}$ output low width (internal clock)	T_{SCL3}		2/fc – 100ns	–	–	
$\overline{SCK}$ output high width (internal clock)	T_{SCH3}		2/fc – 100ns	–	–	
$\overline{SCK}$ input period (external clock)	T_{SCK4}	fc ≦ 8 MHz (V_{DD} = 2.7 V to 5.5 V) fc ≦ 16 MHz (V_{DD} = 4.4 V to 5.5 V)	800	–	–	ns
$\overline{SCK}$ input low width (external clock)	T_{SCL4}		300 (Note 1)	–	–	
$\overline{SCK}$ input low width (external clock)	T_{SCH4}		300 (Note 1)	–	–	
SI input setup time	T_{SUP}		150	–	–	
SI input hold time	T_{HLD}		150	–	–	
SO output delay time	T_{DEL}		–	–	200	
Rising time	T_R	V_{DD} = 3.0 V, CL = 50pF (Note 2)	–	–	100	
Falling time	T_F		–	–	100	
SO last bit hold time	T_{SODH}		16.5/fc	–	32.5/fc	

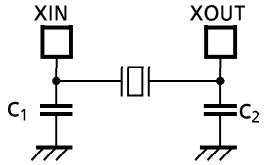
Note 1: T_{SCKL}, T_{SCKH} ≧ 2.5/fc (High-frequency clock mode), T_{SCKL}, T_{SCKH} ≧ 2.5/fc (Low-frequency clock mode)

Note 2: CL, external capacitance

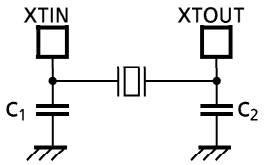


Recommended Oscillating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant	
					C_1	C_2
High-frequency Oscillation	Ceramic resonator	16 MHz	4.5 V to 5.5 V	MURATA CSA16.00MXZ040	10 pF	10 pF
		8 MHz	2.7 V to 5.5 V	MURATA CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	2.7 V to 5.5 V	MURATA CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency Oscillation	Crystal oscillator	32.768 kHz	2.7 V to 5.5 V	SII VT-200	6 pF	6 pF



(1) High-frequency oscillation



(2) Low-frequency oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note2: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html