

DATA SHEET

PDTA124T series
PNP resistor-equipped transistors;
R1 = 22 k Ω , R2 = open

Product specification
Supersedes data of 2004 May 05

2004 Aug 04

**PNP resistor-equipped transistors;
R1 = 22 kΩ, R2 = open**

PDTA124T series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	–	–50	V
I_o	output current (DC)	–	–100	mA
R1	bias resistor	22	–	kΩ
R2	open	–	–	–

DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA124TE	SOT416	SC-75	3R	PDTC124TE
PDTA124TEF	SOT490	SC-89	24	PDTC124TEF
PDTA124TK	SOT346	SC-59	59	PDTC124TK
PDTA124TM	SOT883	SC-101	DJ	PDTC124TM
PDTA124TS	SOT54 (TO-92)	SC-43	TA124T	PDTC124TS
PDTA124TT	SOT23	–	*AE ⁽¹⁾	PDTC124TT
PDTA124TU	SOT323	SC-70	*7B ⁽¹⁾	PDTC124TU

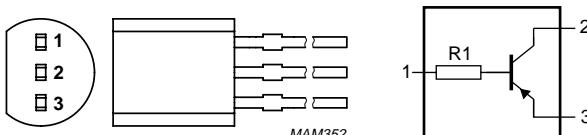
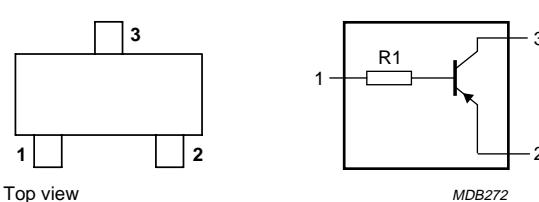
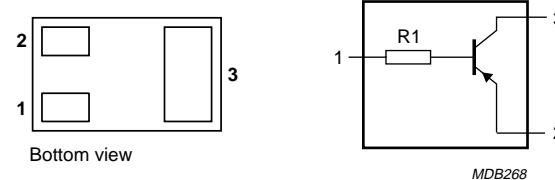
Note

1. * = p: Made in Hong Kong.
- * = t: Made in Malaysia.
- * = W: Made in China.

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA124TS		1 2 3	base collector emitter
PDTA124TE PDTA124TEF PDTA124TK PDTA124TT PDTA124TU		1 2 3	base emitter collector
PDTA124TM		1 2 3	base emitter collector

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTA124TE	–	plastic surface mounted package; 3 leads	SOT416
PDTA124TEF	–	plastic surface mounted package; 3 leads	SOT490
PDTA124TK	–	plastic surface mounted package; 3 leads	SOT346
PDTA124TM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTA124TS	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA124TT	–	plastic surface mounted package; 3 leads	SOT23
PDTA124TU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–50	V
V_{CEO}	collector-emitter voltage	open base	–	–50	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_o	output current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25^\circ\text{C}$			
	SOT23	note 1	–	250	mW
	SOT54	note 1	–	500	mW
	SOT323	note 1	–	200	mW
	SOT346	note 1	–	250	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 µm copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		note 1	500	K/W
		note 1	250	K/W
		note 1	625	K/W
		note 1	500	K/W
		note 1	833	K/W
		notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 µm copper strip line.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -50$ V; $I_E = 0$ A	–	–	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30$ V; $I_B = 0$ A	–	–	-1	µA
		$V_{CE} = -30$ V; $I_B = 0$ A; $T_j = 150$ °C	–	–	-50	µA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5$ V; $I_C = 0$ A	–	–	-100	nA
h_{FE}	DC current gain	$V_{CE} = -5$ V; $I_C = -1$ mA	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10$ mA; $I_B = -0.5$ mA	–	–	-150	mV
$R1$	input resistor		15.4	22	28.6	kΩ
C_c	collector capacitance	$I_E = i_e = 0$ A; $V_{CB} = -10$ V; $f = 1$ MHz	–	–	3	pF

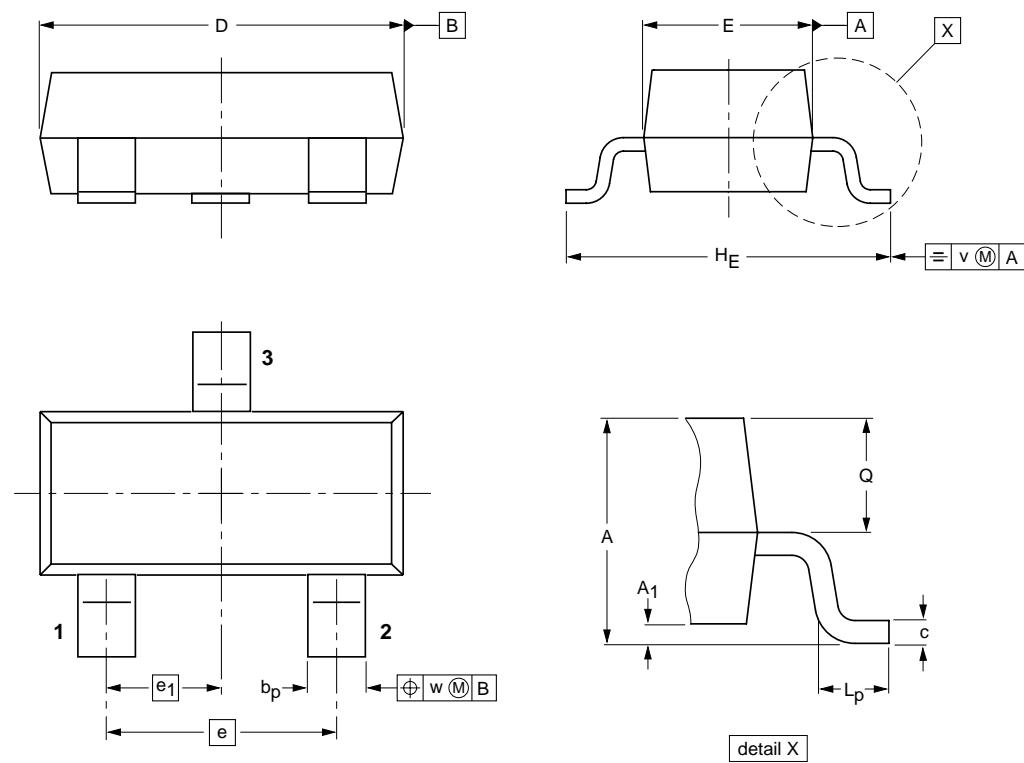
PNP resistor-equipped transistors;
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PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT23



0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	l_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

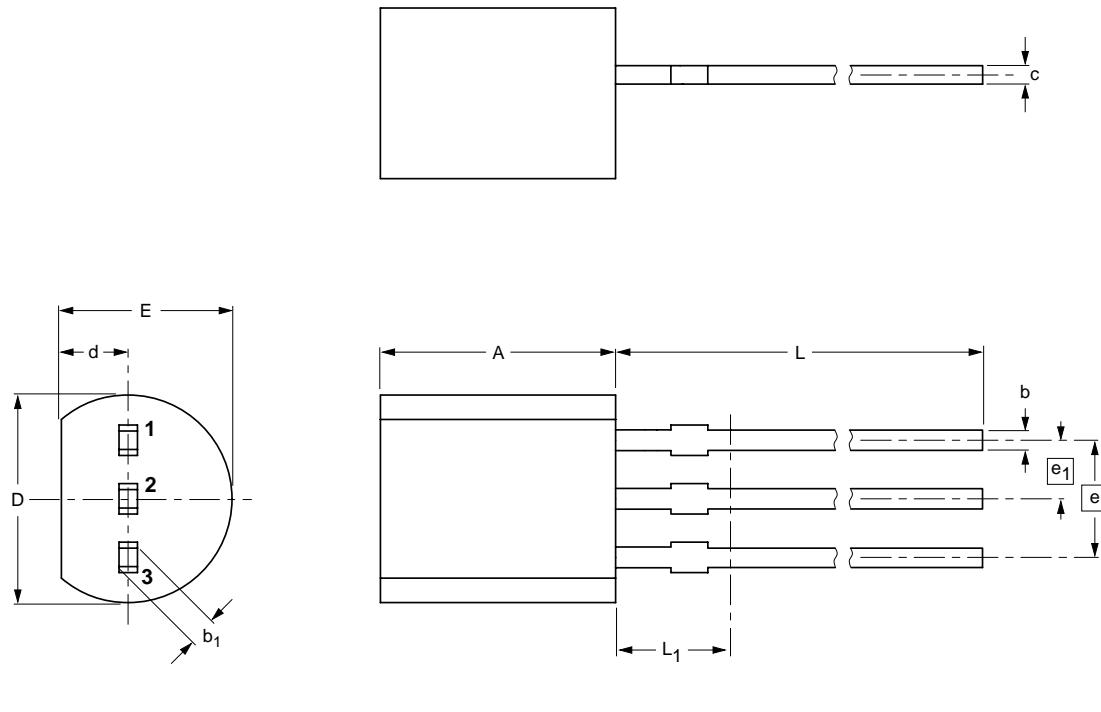
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	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				-97-02-28- 99-09-13

PNP resistor-equipped transistors;
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Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

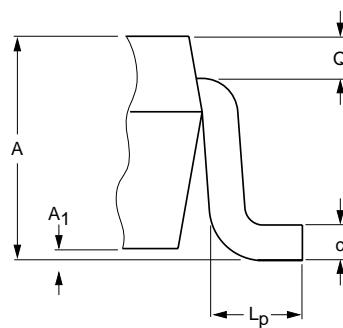
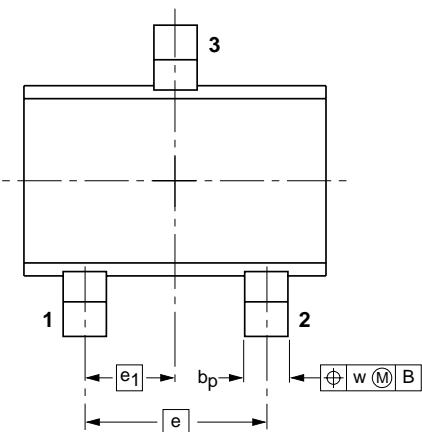
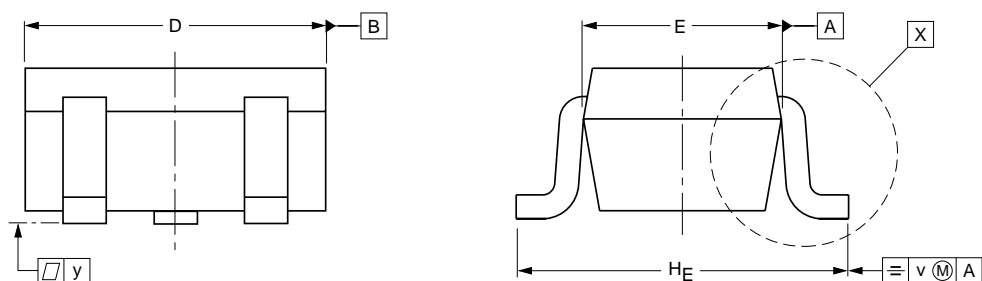
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			-97-02-28 04-06-28

PNP resistor-equipped transistors;
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PDTA124T series

Plastic surface mounted package; 3 leads

SOT323



0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

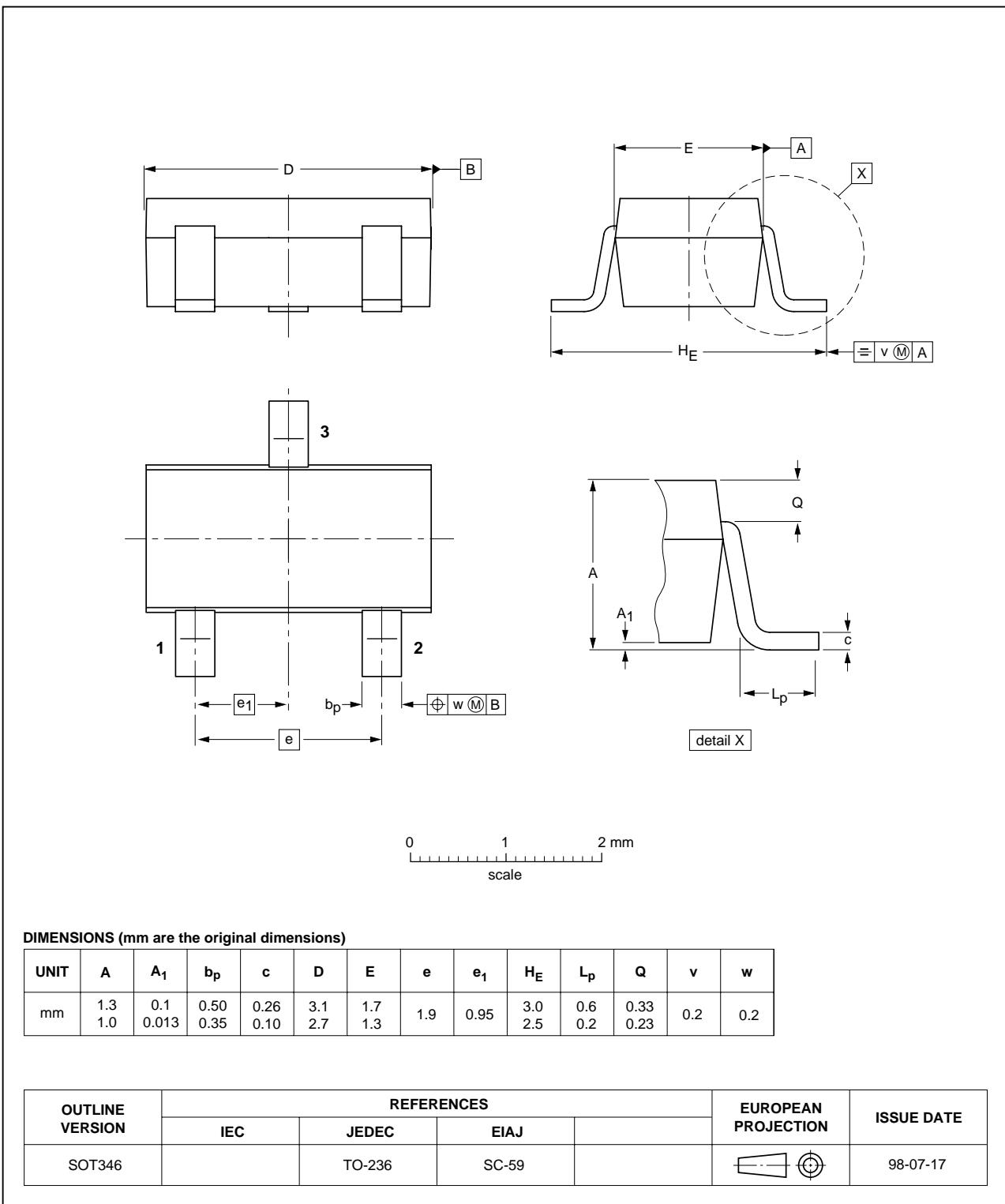
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

PNP resistor-equipped transistors;
R1 = 22 k Ω , R2 = open

PDTA124T series

Plastic surface mounted package; 3 leads

SOT346

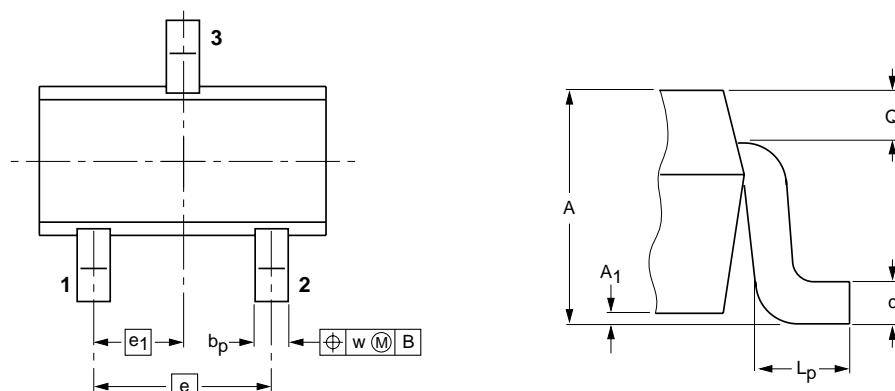
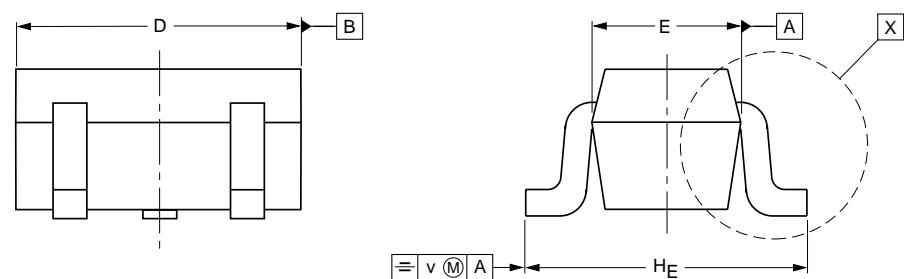


PNP resistor-equipped transistors;
R1 = 22 k Ω , R2 = open

PDTA124T series

Plastic surface mounted package; 3 leads

SOT416



0 0.5 1 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

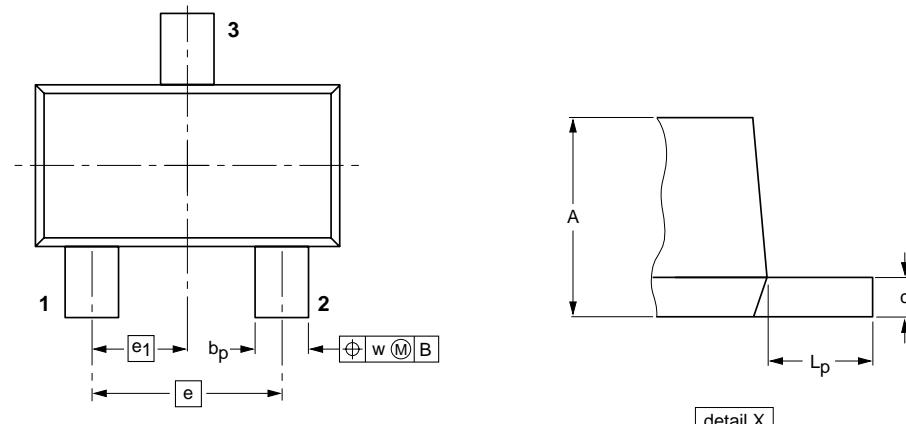
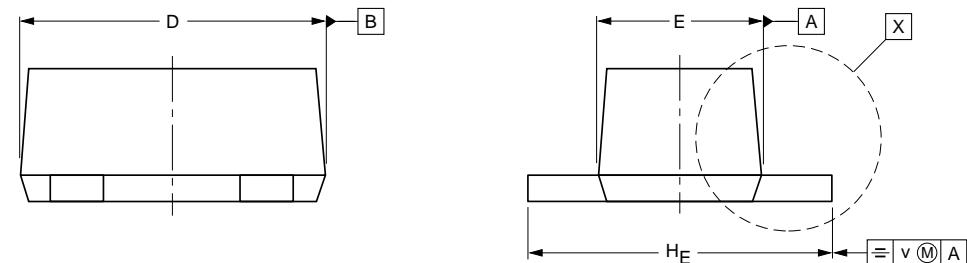
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT416			SC-75			97-02-28

PNP resistor-equipped transistors;
R1 = 22 k Ω , R2 = open

PDTA124T series

Plastic surface mounted package; 3 leads

SOT490



0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	l_p	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

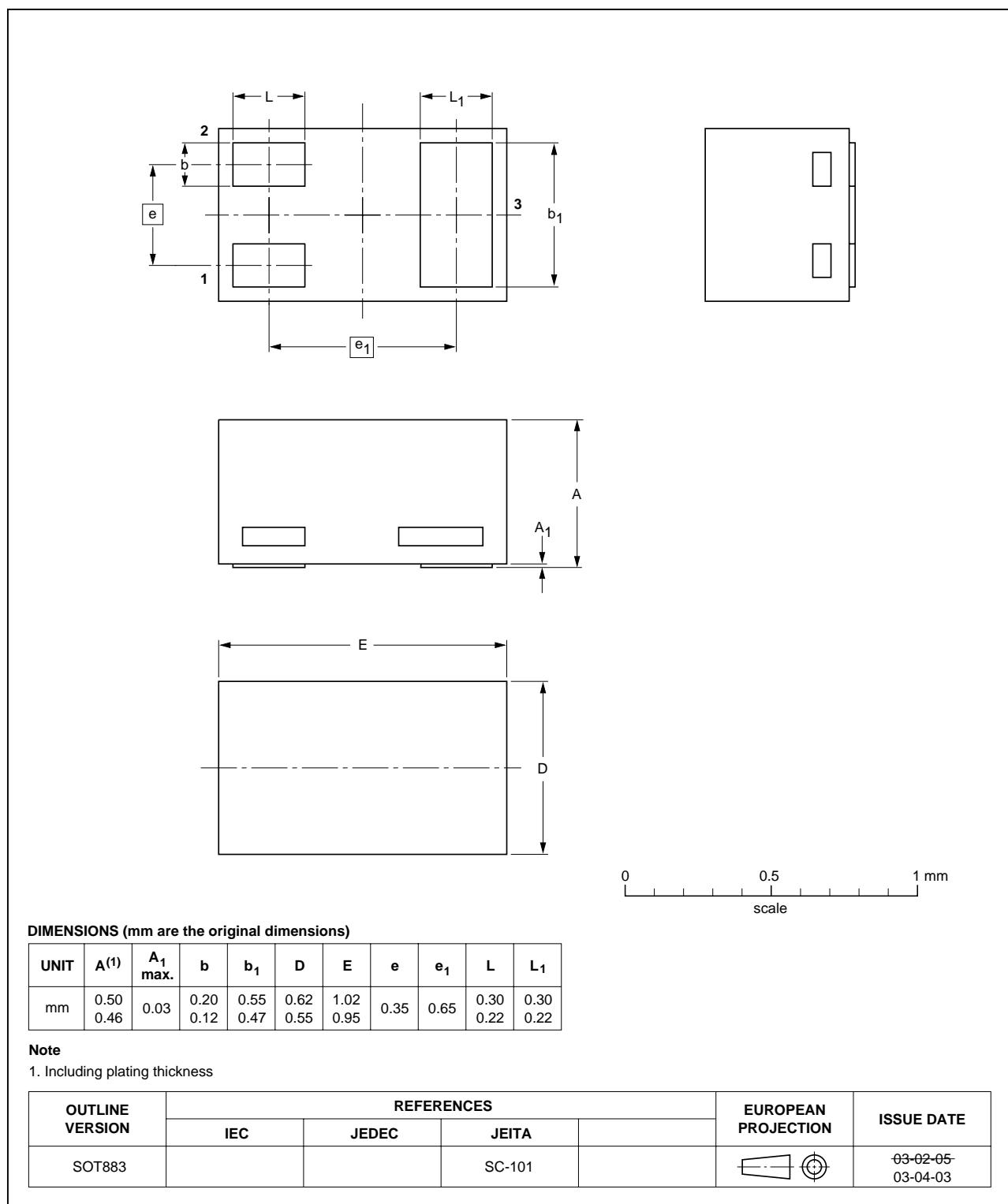
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	IEC	JEDEC	EIAJ	SC-89		
SOT490						98-10-23

PNP resistor-equipped transistors;
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PDTA124T series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



PNP resistor-equipped transistors;
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PDTA124T series

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

R75/03/pp14

Date of release: 2004 Aug 04

Document order number: 9397 750 13653

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