

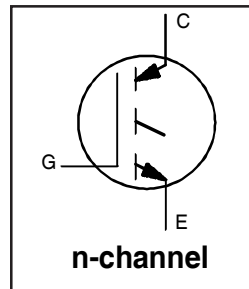
IRG4BC30FPbF

INSULATED GATE BIPOLAR TRANSISTOR

Fast Speed IGBT

Features

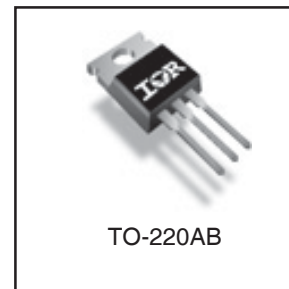
- Fast: optimized for medium operating frequencies (1-5 kHz in hard switching, >20 kHz in resonant mode).
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-220AB package
- Lead-Free



$V_{CES} = 600V$
 $V_{CE(on)} \text{ typ.} = 1.59V$
@ $V_{GE} = 15V, I_C = 17A$

Benefits

- Generation 4 IGBTs offer highest efficiency available
- IGBTs optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	31	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	17	
I_{CM}	Pulsed Collector Current ①	124	
I_{LM}	Clamped Inductive Load Current ②	124	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	10	mJ
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	100	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	$^\circ C$
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	80	
Wt	Weight	2.0 (0.07)	—	g (oz)

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	$V_{GE} = 0V, I_C = 1.0A$
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/ $^\circ\text{C}$	$V_{GE} = 0V, I_C = 1.0mA$
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.59	1.8	V	$I_C = 17A, V_{GE} = 15V$
		—	1.99	—		$I_C = 31A, V_{GE} = 15V$
		—	1.7	—		$I_C = 17A, T_J = 150^\circ\text{C}$ See Fig. 2, 5
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/ $^\circ\text{C}$	$V_{CE} = V_{GE}, I_C = 250\mu A$
g_{fe}	Forward Transconductance ⑤	6.1	10	—	S	$V_{CE} = 100V, I_C = 17A$
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{GE} = 0V, V_{CE} = 600V$
		—	—	2.0		$V_{GE} = 0V, V_{CE} = 10V, T_J = 25^\circ\text{C}$
		—	—	1000		$V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	77	nC	$I_C = 17A$
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.9	12		$V_{CC} = 400V$ See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	19	28		$V_{GE} = 15V$
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	$T_J = 25^\circ\text{C}$ $I_C = 17A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 23\Omega$ Energy losses include "tail" See Fig. 10, 11, 13, 14
t_r	Rise Time	—	15	—		
$t_{d(off)}$	Turn-Off Delay Time	—	200	300		
t_f	Fall Time	—	180	270		
E_{on}	Turn-On Switching Loss	—	0.23	—	mJ	See Fig. 10, 11, 13, 14
E_{off}	Turn-Off Switching Loss	—	1.18	—		
E_{ts}	Total Switching Loss	—	1.41	2.0		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	$T_J = 150^\circ\text{C}$, $I_C = 17A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 23\Omega$ Energy losses include "tail" See Fig. 13, 14
t_r	Rise Time	—	16	—		
$t_{d(off)}$	Turn-Off Delay Time	—	290	—		
t_f	Fall Time	—	350	—		
E_{ts}	Total Switching Loss	—	2.5	—	mJ	
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1100	—	pF	$V_{GE} = 0V$
C_{oes}	Output Capacitance	—	74	—		$V_{CC} = 30V$ See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	14	—		$f = 1.0MHz$

Notes:

- ① Repetitive rating; $V_{GE} = 20V$, pulse width limited by max. junction temperature. (See fig. 13b)
- ② $V_{CC} = 80\%(V_{CES})$, $V_{GE} = 20V$, $L = 10\mu H$, $R_G = 23\Omega$, (See fig. 13a)
- ③ Repetitive rating; pulse width limited by maximum junction temperature.

- ④ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
- ⑤ Pulse width $5.0\mu s$, single shot.

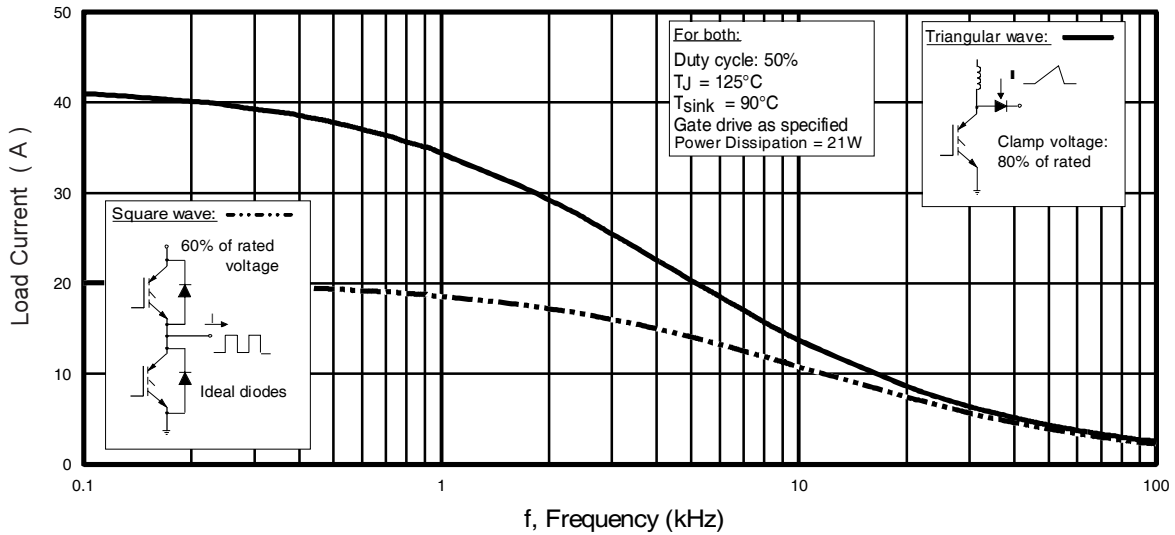


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I = I_{\text{RMS}}$ of fundamental; for triangular wave, $I = I_{\text{PK}}$)

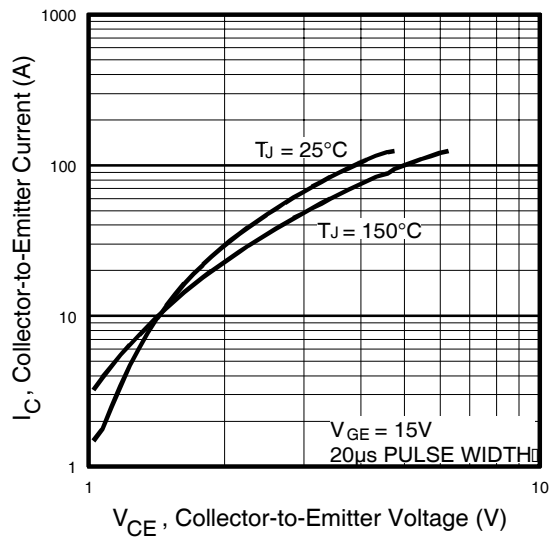


Fig. 2 - Typical Output Characteristics

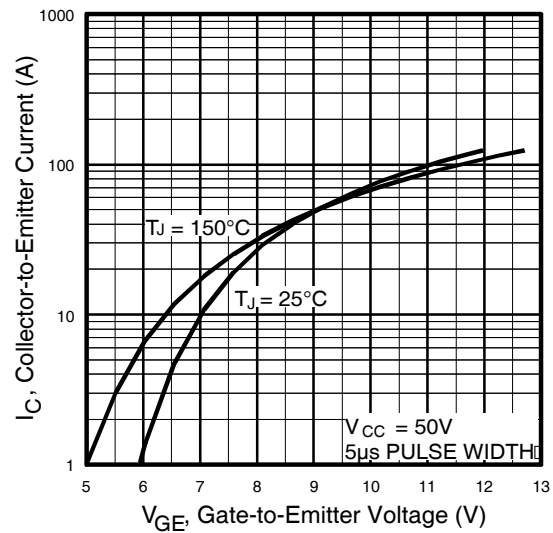


Fig. 3 - Typical Transfer Characteristics

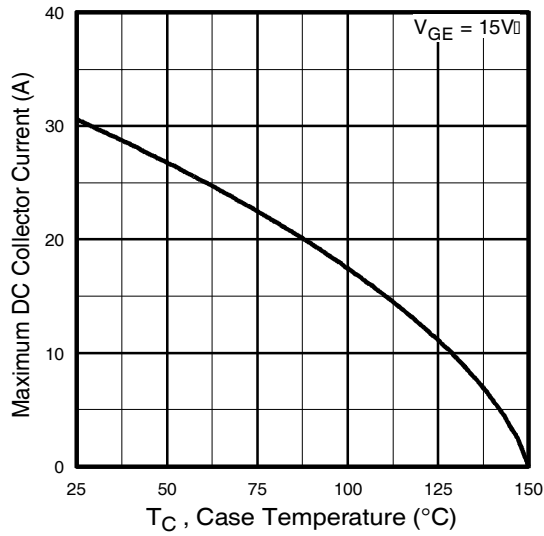


Fig. 4 - Maximum Collector Current vs. Case Temperature

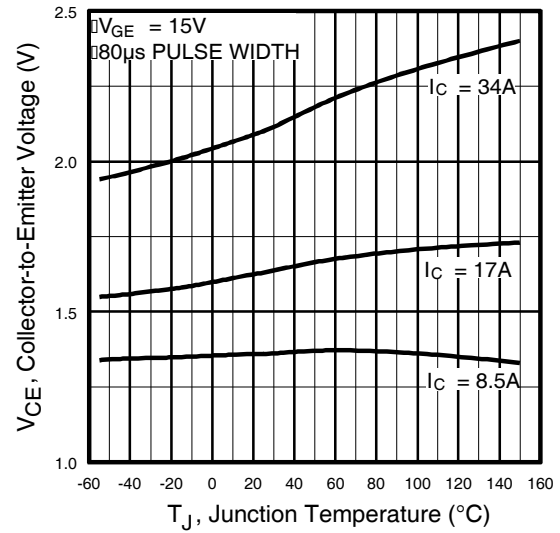


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

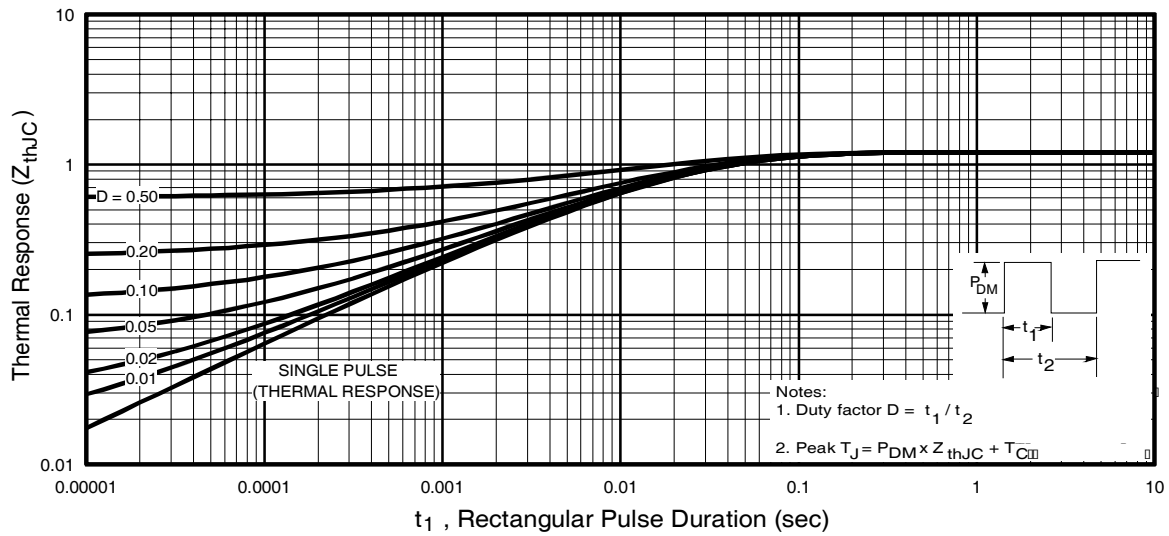


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

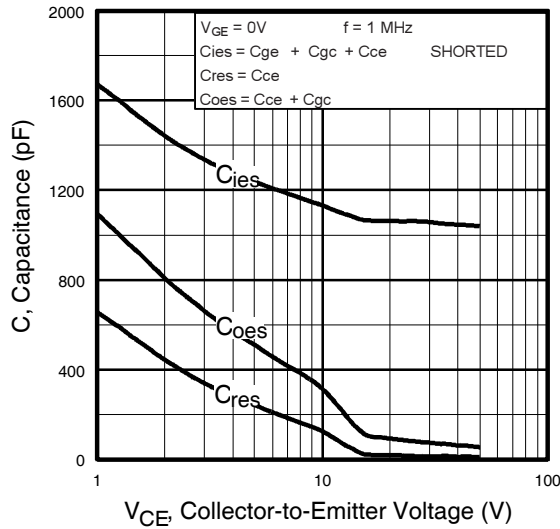


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

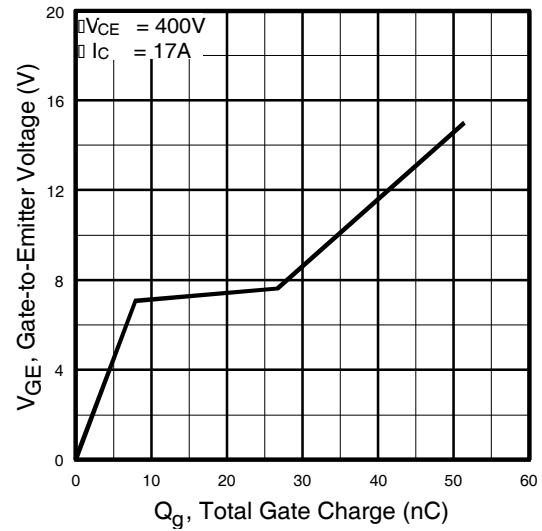


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

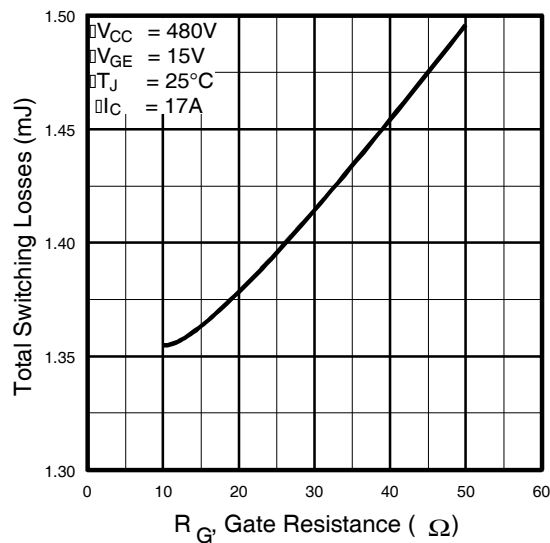


Fig. 9 - Typical Switching Losses vs. Gate Resistance

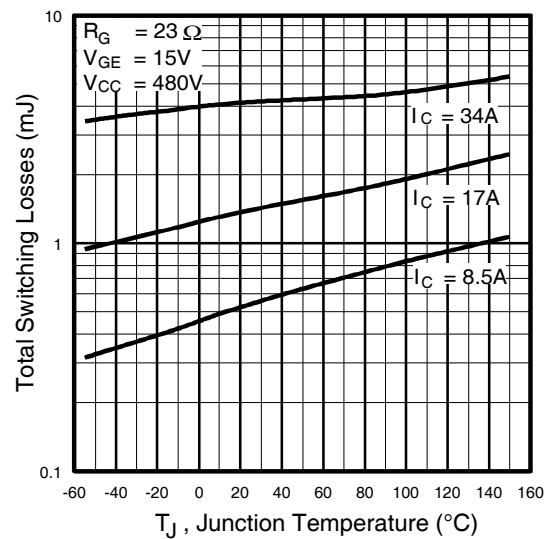


Fig. 10 - Typical Switching Losses vs. Junction Temperature

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IR Rectifier

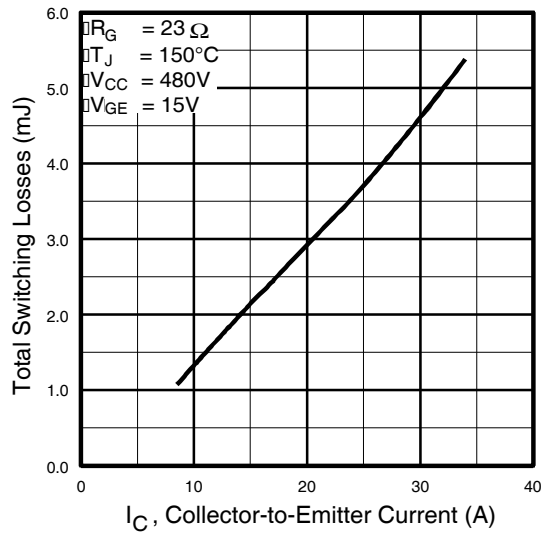


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

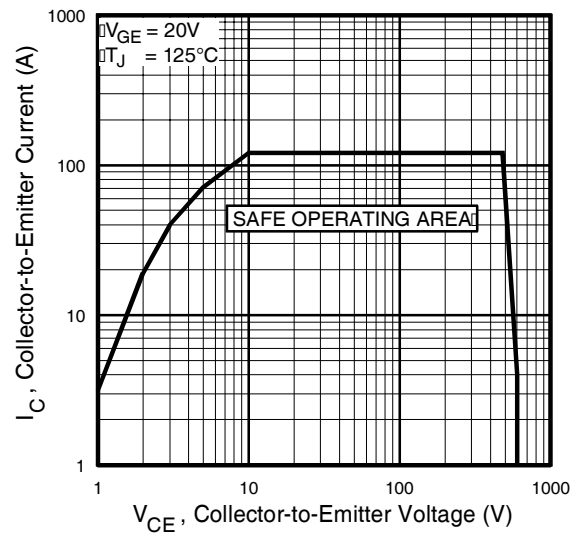


Fig. 12 - Turn-Off SOA

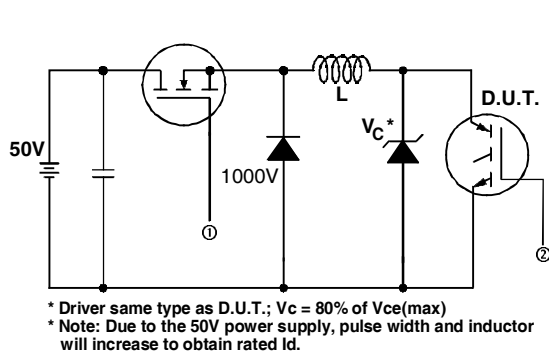


Fig. 13a - Clamped Inductive Load Test Circuit

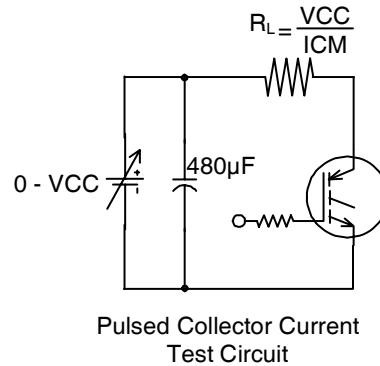


Fig. 13b - Pulsed Collector Current Test Circuit

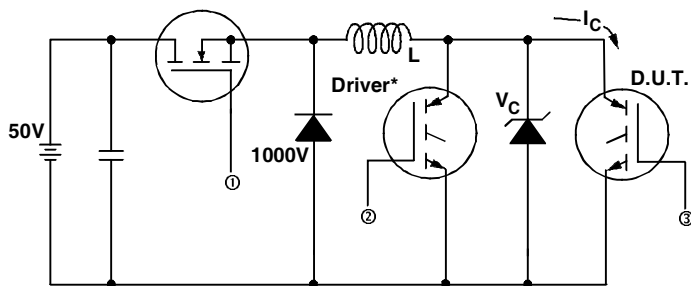


Fig. 14a - Switching Loss Test Circuit

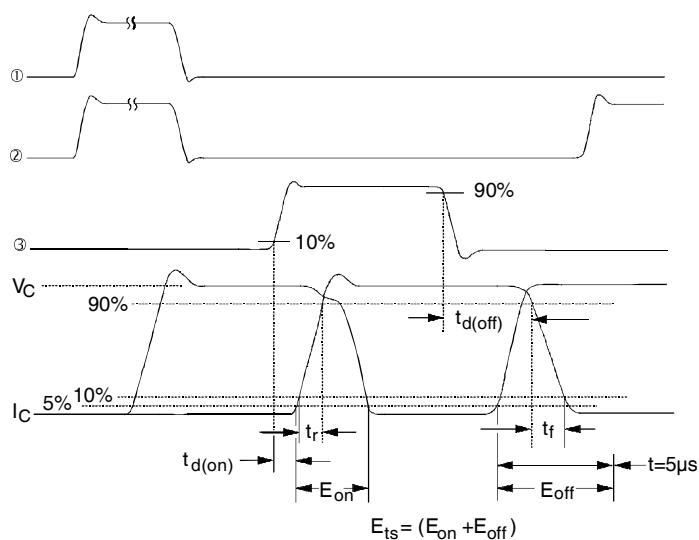


Fig. 14b - Switching Loss Waveforms

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IOR Rectifier

[illegible]

- NOTES:
- 1- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
 - 2- LEAD DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
 - 3- LEAD DIMENSION AND FINISH UNCONTROLLED IN E1
 - 4- DIMENSION D1 & E1 DO NOT INCLUDE MOUNTING FLANGE WELD FLASH
 - 5- SMALL PART EXCEEDS 0.0127 (0.500) IN SIZE. THESE DIMENSIONS ARE MEASURED AT THE OUTSIDE SURFACES OF THE PLASTIC BODY.
 - 6- DIMENSION D1, D3 & C1 APPLY TO BARE METAL ONLY.
 - 7- CONTROLLING DIMENSION - INCHES
 - 8- THERMAL PAIR CONTOUR OPTIONAL. WITHIN DIMENSIONS E1/2D2 & E1 DIMENSION D2 IS 1/2 OF DIMENSION E1. WHEN HEATING AND SINGULATION IRREGULARITIES ARE ALLOWED.
 - 9- OUTLINE CONFORMS TO JEDEC J-220, EXCEPT D1 (max) and D2 (min). WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE SIZE.

SYMBOL	DIMENSIONS				NOTE
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.035	0.491	.0014	.0193	
A2	0.035	2.92	.0014	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.36	0.61	.014	.024	5
D	3.8	0.56	.151	.022	5
D1	14.6	2.22	.575	.088	4
D2	11.68	12.89	.460	.507	7
E	9.65	10.87	.380	.425	4, 7
E1	8.8	8.89	.350	.350	4
E2	—	.76	—	.030	8
e	2.54	3.81	.100	.150	
e1	—	—	.000	.000	
H	5.84	6.86	.230	.270	7.8
H1	12.70	14.33	.500	.580	
H2	3.56	4.06	.140	.160	3
W	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXLET

1.- GATE
2.- DRAIN
3.- SOURCE

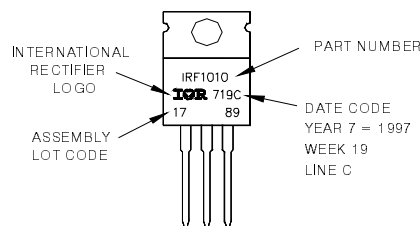
GRID/CAPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

DIODES

1.- ANODE
2.- CATHODE
3.- ANODE

EXAMPLE: THIS IS AN IRF101 0
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE 'C'
Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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