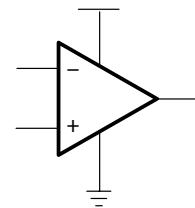


TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

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- **Wide Bandwidth . . . 10 MHz**
- **High Output Drive**
 - $I_{OH} . . . 57 \text{ mA}$ at $V_{DD} = 1.5 \text{ V}$
 - $I_{OL} . . . 55 \text{ mA}$ at 0.5 V
- **High Slew Rate**
 - $SR+ . . . 16 \text{ V}/\mu\text{s}$
 - $SR- . . . 19 \text{ V}/\mu\text{s}$
- **Wide Supply Range . . . 4.5 V to 16 V**
- **Supply Current . . . 1.9 mA/Channel**
- **Ultralow Power Shutdown Mode**
 $I_{DD} . . . 125 \mu\text{A}/\text{Channel}$
- **Low Input Noise Voltage . . . 7 nV/ $\sqrt{\text{Hz}}$**
- **Input Offset Voltage . . . 60 μV**
- **Ultra-Small Packages**
 - 8 or 10 Pin MSOP (TLC070/1/2/3)

Operational Amplifier



description

The first members of TI's new BiMOS general-purpose operational amplifier family are the TLC07x. The BiMOS family concept is simple: provide an upgrade path for BiFET users who are moving away from dual-supply to single-supply systems and demand higher AC and dc performance. With performance rated from 4.5 V to 16 V across commercial (0°C to 70°C) and an extended industrial temperature range (-40°C to 125°C), BiMOS suits a wide range of audio, automotive, industrial and instrumentation applications. Familiar features like offset nulling pins, and new features like MSOP PowerPAD™ packages and shutdown modes, enable higher levels of performance in a variety of applications.

Developed in TI's patented LBC3 BiCMOS process, the new BiMOS amplifiers combine a very high input impedance low-noise CMOS front end with a high-drive bipolar output stage, thus providing the optimum performance features of both. AC performance improvements over the TL07x BiFET predecessors include a bandwidth of 10 MHz (an increase of 300%) and voltage noise of 7 nV/ $\sqrt{\text{Hz}}$ (an improvement of 60%). DC improvements include a factor of 4 reduction in input offset voltage down to 1.5 mV (maximum) in the standard grade, and a power supply rejection improvement of greater than 40 dB to 130 dB. Added to this list of impressive features is the ability to drive $\pm 50\text{-mA}$ loads comfortably from an ultrasmall-footprint MSOP PowerPAD package, which positions the TLC07x as the ideal high-performance general-purpose operational amplifier family.

FAMILY PACKAGE TABLE

| DEVICE | NO. OF CHANNELS | PACKAGE TYPES | | | | SHUTDOWN | UNIVERSAL EVM BOARD |
|--------|-----------------|---------------|------|------|-------|----------|---|
| | | MSOP | PDIP | SOIC | TSSOP | | |
| TLC070 | 1 | 8 | 8 | 8 | — | Yes | Refer to the EVM Selection Guide (Lit# SLOU060) |
| TLC071 | 1 | 8 | 8 | 8 | — | — | |
| TLC072 | 2 | 8 | 8 | 8 | — | — | |
| TLC073 | 2 | 10 | 14 | 14 | — | Yes | |
| TLC074 | 4 | — | 14 | 14 | 20 | — | |
| TLC075 | 4 | — | 16 | 16 | 20 | Yes | |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
OPERATIONAL AMPLIFIERS**

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TLC070 and TLC071 AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | | | |
|----------------|-----------------------------------|-------------------------------------|--------------------|------------------------|
| | SMALL OUTLINE (D) [†] | SMALL OUTLINE (DGN) [†] | SYMBOL | PLASTIC DIP (P) |
| 0°C to 70°C | TLC070CD TLC071CD | TLC070CDGN TLC071CDGN | xxTIACS xxTIACU | TLC070CP TLC071CP |
| –40°C to 125°C | TLC070ID TLC071ID | TLC070IDGN TLC071IDGN | xxTIACT xxTIACV | TLC070IP TLC071IP |
| | TLC070AID TLC071AID | — — | — — | TLC070AIP TLC071AIP |

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC070CDR).

TLC072 and TLC073 AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | | | | | PLASTIC DIP (N) | PLASTIC DIP (P) | | |
|----------------|--------------------------------------|--------------------|---------------------|--------------------|---------------------|-----------------------|-----------------------|--|--|
| | SMALL OUTLINE (D) [†] | MSOP | | | | | | | |
| | | (DGN) [†] | SYMBOL [‡] | (DGQ) [†] | SYMBOL [‡] | | | | |
| 0°C to 70°C | TLC072CD TLC073CD | TLC072CDGN — | xxTIADV — | — TLC073CDGQ | — xxTIADX | — TLC073CN | TLC072CP — | | |
| –40°C to 125°C | TLC072ID TLC073ID | TLC072IDGN — | xxTIADW — | — TLC073IDGQ | — xxTIADY | — TLC073IN | TLC072IP — | | |
| | TLC072AID TLC073AID | — — | — — | — — | — — | — TLC073AIN | TLC072AIP — | | |

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC072CDR).

[‡] xx represents the device date code.

TLC074 and TLC075 AVAILABLE OPTIONS

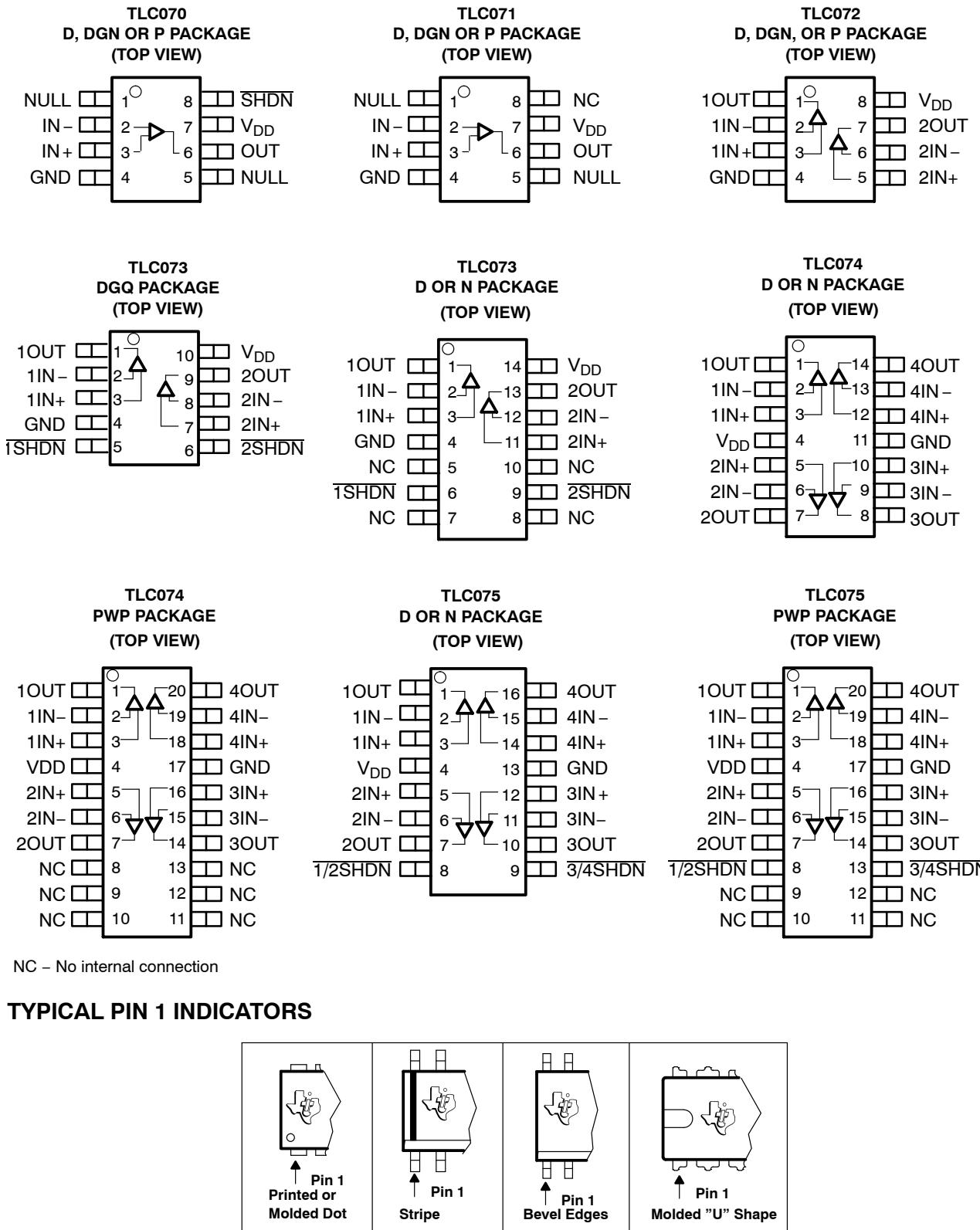
| T _A | PACKAGED DEVICES | | |
|----------------|-----------------------------------|------------------------|-----------------------------|
| | SMALL OUTLINE (D) [†] | PLASTIC DIP (N) | TSSOP (PWP) [†] |
| 0°C to 70°C | TLC074CD TLC075CD | TLC074CN TLC075CN | TLC074CPWP TLC075CPWP |
| –40°C to 125°C | TLC074ID TLC075ID | TLC074IN TLC075IN | TLC074IPWP TLC075IPWP |
| | TLC074AID TLC075AID | TLC074AIN TLC075AIN | TLC074AIPWP TLC075AIPWP |

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC074CDR).

**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
OPERATIONAL AMPLIFIERS**

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TLC07x PACKAGE PIN OUTS



**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|------------------------------|
| Supply voltage, V_{DD} (see Note 1) | 17 V |
| Differential input voltage range, V_{ID} | $\pm V_{DD}$ |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A : C suffix | 0°C to 70°C |
| I suffix | -40°C to 125°C |
| Maximum junction temperature, T_J | 150°C |
| Storage temperature range, T_{STG} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

| PACKAGE | θ_{JC} (°C/W) | θ_{JA} (°C/W) | $T_A \leq 25^\circ\text{C}$ POWER RATING |
|------------|-------------------------|-------------------------|---|
| D (8) | 38.3 | 176 | 710 mW |
| D (14) | 26.9 | 122.3 | 1022 mW |
| D (16) | 25.7 | 114.7 | 1090 mW |
| DGN (8) | 4.7 | 52.7 | 2.37 W |
| DGQ (10) | 4.7 | 52.3 | 2.39 W |
| N (14, 16) | 32 | 78 | 1600 mW |
| P (8) | 41 | 104 | 1200 mW |
| PWP (20) | 1.40 | 26.1 | 4.79 W |

recommended operating conditions

| | | MIN | MAX | UNIT |
|--|---------------|------------|--------------|------|
| Supply voltage, V_{DD} | Single supply | 4.5 | 16 | V |
| | Split supply | ± 2.25 | ± 8 | |
| Common-mode input voltage, V_{ICR} | | +0.5 | $V_{DD}-0.8$ | V |
| Shutdown on/off voltage level [‡] | V_{IH} | 2 | | V |
| | V_{OL} | | 0.8 | |
| Operating free-air temperature, T_A | C-suffix | 0 | 70 | °C |
| | I-suffix | -40 | 125 | |

[‡] Relative to the voltage on the GND terminal of the device.

**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | T_A^\dagger | MIN | TYP | MAX | UNIT | |
|----------------|---|--|-----------------------------|---------------|------|------|-----|------------------------------|--|
| V_{IO} | Input offset voltage | $V_{DD} = 5\text{ V}$, $V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$ | TLC070/1/2/3, TLC074/5 | 25°C | 390 | 1900 | | μV | |
| | | | Full range | | | 3000 | | | |
| | | | TLC070/1/2/3A, TLC074/5A | 25°C | 390 | 1400 | | | |
| | | | Full range | | | 2000 | | | |
| α_{VIO} | Temperature coefficient of input offset voltage | | | | | 1.2 | | $\mu\text{V}/^\circ\text{C}$ | |
| I_{IO} | Input offset current | $V_{DD} = 5\text{ V}$, $V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$ | TLC07XC | 25°C | 0.7 | 50 | | pA | |
| | | | Full range | | | 100 | | | |
| | | | TLC07XI | | | 700 | | | |
| | | | | 25°C | 1.5 | 50 | | | |
| I_{IB} | Input bias current | $V_{DD} = 5\text{ V}$, $V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$ | TLC07XC | | | 100 | | pA | |
| | | | Full range | | | 700 | | | |
| | | | TLC07XI | 25°C | 1.5 | 50 | | | |
| | | | | | | 100 | | | |
| V_{ICR} | Common-mode input voltage | $R_S = 50\ \Omega$ | | 25°C | 0.5 | | | V | |
| | | | | | to | | | | |
| | | | | | 4.2 | | | | |
| | | | Full range | 25°C | 0.5 | | | | |
| | | | | | to | | | | |
| | | | | | 4.2 | | | | |
| V_{OH} | High-level output voltage | $V_{IC} = 2.5\text{ V}$ | $I_{OH} = -1\text{ mA}$ | 25°C | 4.1 | 4.3 | | V | |
| | | | | Full range | 3.9 | | | | |
| | | | $I_{OH} = -20\text{ mA}$ | 25°C | 3.7 | 4 | | | |
| | | | | Full range | 3.5 | | | | |
| | | | $I_{OH} = -35\text{ mA}$ | 25°C | 3.4 | 3.8 | | | |
| | | | | Full range | 3.2 | | | | |
| | | | $I_{OH} = -50\text{ mA}$ | 25°C | 3.2 | 3.6 | | | |
| | | | | -40°C to 85°C | | 3 | | | |
| V_{OL} | Low-level output voltage | $V_{IC} = 2.5\text{ V}$ | $I_{OL} = 1\text{ mA}$ | 25°C | 0.18 | 0.25 | | V | |
| | | | | Full range | | 0.35 | | | |
| | | | $I_{OL} = 20\text{ mA}$ | 25°C | 0.35 | 0.39 | | | |
| | | | | Full range | | 0.45 | | | |
| | | | $I_{OL} = 35\text{ mA}$ | 25°C | 0.43 | 0.55 | | | |
| | | | | Full range | | 0.7 | | | |
| | | | $I_{OL} = 50\text{ mA}$ | 25°C | 0.48 | 0.63 | | | |
| | | | | -40°C to 85°C | | 0.7 | | | |
| I_{OS} | Short-circuit output current | Sourcing | | 25°C | 100 | | | mA | |
| | | Sinking | | 25°C | 100 | | | | |
| I_O | Output current | $V_{OH} = 1.5\text{ V}$ from positive rail | | 25°C | 57 | | | mA | |
| | | $V_{OL} = 0.5\text{ V}$ from negative rail | | 25°C | 55 | | | | |

[†] Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
OPERATIONAL AMPLIFIERS**

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**electrical characteristics at specified free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)
(continued)**

| PARAMETER | TEST CONDITIONS | T_A^\dagger | MIN | TYP | MAX | UNIT |
|---|---|---------------|------|-----|-----|----------|
| A_{VD} Large-signal differential voltage amplification | $V_{O(PP)} = 3$ V, $R_L = 10$ k Ω | 25°C | 100 | 120 | | dB |
| | | Full range | 100 | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 1000 | | | GeV |
| C_{IC} Common-mode input capacitance | $f = 10$ kHz | 25°C | 22.9 | | | pF |
| z_o Closed-loop output impedance | $f = 10$ kHz, $A_V = 10$ | 25°C | 0.25 | | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = 1$ to 3 V, $R_S = 50$ Ω | 25°C | 80 | 95 | | dB |
| | | Full range | 80 | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD} = 4.5$ V to 16 V, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 100 | | dB |
| | | Full range | 80 | | | |
| I_{DD} Supply current (per channel) | $V_O = 2.5$ V, No load | 25°C | 1.9 | 2.5 | | mA |
| | | Full range | | 3.5 | | |
| $I_{DD(SHDN)}$ Supply current in shutdown mode (per channel) (TLC070, TLC073, TLC075) | $SHDN \leq 0.8$ V | 25°C | 125 | 200 | | μ A |
| | | Full range | | 250 | | |

[†] Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
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operating characteristics at specified free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | TA [†] | MIN | TYP | MAX | UNIT | |
|------------------------|--------------------------------------|--|--|-----------------|---------------------------------------|-----|---------|------------------------|--|
| SR+ | Positive slew rate at unity gain | $V_{O(PP)} = 0.8$ V, $R_L = 10$ k Ω | | 25°C | 10 | 16 | | V/ μ s | |
| | | | | Full range | 9.5 | | | | |
| SR- | Negative slew rate at unity gain | $V_{O(PP)} = 0.8$ V, $R_L = 10$ k Ω | | 25°C | 12.5 | 19 | | V/ μ s | |
| | | | | Full range | 10 | | | | |
| V _n | Equivalent input noise voltage | $f = 100$ Hz | | 25°C | 12 | | | nV/ $\sqrt{\text{Hz}}$ | |
| | | $f = 1$ kHz | | 25°C | 7 | | | | |
| I _n | Equivalent input noise current | $f = 1$ kHz | | 25°C | 0.6 | | | fA/ $\sqrt{\text{Hz}}$ | |
| THD + N | Total harmonic distortion plus noise | $V_{O(PP)} = 3$ V, $R_L = 10$ k Ω and 250 Ω , $f = 1$ kHz | | 25°C | A _V = 1 | | 0.002% | | |
| | | | | | A _V = 10 | | 0.012% | | |
| | | | | | A _V = 100 | | 0.085% | | |
| t _(on) | Amplifier turn-on time [‡] | $R_L = 10$ k Ω | | 25°C | 0.15 | | μ s | | |
| t _(off) | Amplifier turn-off time [‡] | | | 25°C | 1.3 | | μ s | | |
| Gain-bandwidth product | | $f = 10$ kHz, $R_L = 10$ k Ω | | 25°C | 10 | | MHz | | |
| t _s | Settling time | $V_{(STEP)PP} = 1$ V, A _V = -1, C _L = 10 pF, R _L = 10 k Ω | | 25°C | 0.1% | | 0.18 | μ s | |
| | | | | | 0.01% | | 0.39 | | |
| | | $V_{(STEP)PP} = 1$ V, A _V = -1, C _L = 47 pF, R _L = 10 k Ω | | | 0.1% | | 0.18 | | |
| | | | | | 0.01% | | 0.39 | | |
| | | | | | $R_L = 10$ k Ω , $C_L = 50$ pF | | 32° | | |
| ϕ_m | Phase margin | $R_L = 10$ k Ω , $C_L = 0$ pF | | 25°C | 40° | | | | |
| | | $R_L = 10$ k Ω , $C_L = 50$ pF | | | 2.2 | | | | |
| Gain margin | | $R_L = 10$ k Ω , $C_L = 0$ pF | | 25°C | 3.3 | | | dB | |

[†] Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

[‡] Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

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FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
OPERATIONAL AMPLIFIERS**

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electrical characteristics at specified free-air temperature, $V_{DD} = 12$ V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A^\dagger | MIN | TYP | MAX | UNIT | |
|---|---|-----------------------------|---------------|-------------------|------|------------|--|
| V_{IO} Input offset voltage | $V_{DD} = 12$ V $V_{IC} = 6$ V, $V_O = 6$ V, $R_S = 50 \Omega$ | TLC070/1/2/3, TLC074/5 | 25°C | 390 | 1900 | μ V | |
| | | Full range | | | 3000 | | |
| | | TLC070/1/2/3A, TLC074/5A | 25°C | 390 | 1400 | | |
| | | Full range | | | 2000 | | |
| α_{VIO} Temperature coefficient of input offset voltage | | | | 1.2 | | μ V/°C | |
| I_{IO} Input offset current | $V_{DD} = 12$ V $V_{IC} = 6$ V, $V_O = 6$ V, $R_S = 50 \Omega$ | TLC07xC | 25°C | 0.7 | 50 | p A | |
| | | Full range | | | 100 | | |
| | | TLC07xI | | | 700 | | |
| I_{IB} Input bias current | $V_{DD} = 12$ V $V_{IC} = 6$ V, $V_O = 6$ V, $R_S = 50 \Omega$ | TLC07xC | 25°C | 1.5 | 50 | p A | |
| | | Full range | | | 100 | | |
| | | TLC07xI | | | 700 | | |
| V_{ICR} Common-mode input voltage | $R_S = 50 \Omega$ | | 25°C | 0.5 to 11.2 | | V | |
| | | | Full range | 0.5 to 11.2 | | | |
| V_{OH} High-level output voltage | $V_{IC} = 6$ V | $I_{OH} = -1$ mA | 25°C | 11.1 | 11.2 | V | |
| | | | Full range | 11 | | | |
| | | $I_{OH} = -20$ mA | 25°C | 10.8 | 10.9 | | |
| | | | Full range | 10.7 | | | |
| | | $I_{OH} = -35$ mA | 25°C | 10.6 | 10.7 | | |
| | | | Full range | 10.3 | | | |
| | | $I_{OH} = -50$ mA | 25°C | 10.4 | 10.5 | | |
| | | | -40°C to 85°C | 10.3 | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 6$ V | $I_{OL} = 1$ mA | 25°C | 0.17 | 0.25 | V | |
| | | | Full range | | 0.35 | | |
| | | $I_{OL} = 20$ mA | 25°C | 0.35 | 0.45 | | |
| | | | Full range | | 0.5 | | |
| | | $I_{OL} = 35$ mA | 25°C | 0.4 | 0.52 | | |
| | | | Full range | | 0.6 | | |
| | | $I_{OL} = 50$ mA | 25°C | 0.45 | 0.6 | | |
| | | | -40°C to 85°C | | 0.65 | | |
| I_{OS} Short-circuit output current | Sourcing | | 25°C | | 150 | mA | |
| | Sinking | | 25°C | | 150 | | |
| I_O Output current | $V_{OH} = 1.5$ V from positive rail | | 25°C | | 57 | mA | |
| | $V_{OL} = 0.5$ V from negative rail | | 25°C | | 55 | | |

[†] Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
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**electrical characteristics at specified free-air temperature, $V_{DD} = 12$ V (unless otherwise noted)
(continued)**

| PARAMETER | TEST CONDITIONS | T_A^\dagger | MIN | TYP | MAX | UNIT |
|--|--|---------------|------|-----|-----|----------|
| A_{VD} Large-signal differential voltage amplification | $V_{O(PP)} = 8$ V, $R_L = 10$ k Ω | 25°C | 120 | 140 | | dB |
| | | Full range | 120 | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 1000 | | | GeV |
| C_{IC} Common-mode input capacitance | $f = 10$ kHz | 25°C | 21.6 | | | pF |
| z_o Closed-loop output impedance | $f = 10$ kHz, $A_V = 10$ | 25°C | 0.25 | | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = 1$ to 10 V, $R_S = 50$ Ω | 25°C | 80 | 100 | | dB |
| | | Full range | 80 | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD} = 4.5$ V to 16 V, $V_{IC} = V_{DD}/2$, No load | 25°C | 80 | 100 | | dB |
| | | Full range | 80 | | | |
| I_{DD} Supply current (per channel) | $V_O = 7.5$ V, No load | 25°C | 2.1 | 2.9 | | mA |
| | | Full range | | 3.5 | | |
| $I_{DD(SHDN)}$ Supply current in shutdown mode (TLC070, TLC073, TLC075) (per channel) | $SHDN \leq 0.8$ V | 25°C | 125 | 200 | | μ A |
| | | Full range | | 250 | | |

[†] Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
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operating characteristics at specified free-air temperature, $V_{DD} = 12$ V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | TA [†] | MIN | TYP | MAX | UNIT | |
|------------------------|--------------------------------------|--|--|-----------------|--------|-----|-----|------------------------|--|
| SR+ | Positive slew rate at unity gain | $V_{O(PP)} = 2$ V, $R_L = 10$ k Ω | $C_L = 50$ pF, | 25°C | 10 | 16 | | V/ μ s | |
| | | | | Full range | 9.5 | | | | |
| SR- | Negative slew rate at unity gain | $V_{O(PP)} = 2$ V, $R_L = 10$ k Ω | $C_L = 50$ pF, | 25°C | 12.5 | 19 | | V/ μ s | |
| | | | | Full range | 10 | | | | |
| V _n | Equivalent input noise voltage | $f = 100$ Hz | | 25°C | | 12 | | nV/ $\sqrt{\text{Hz}}$ | |
| | | $f = 1$ kHz | | 25°C | | 7 | | | |
| I _n | Equivalent input noise current | $f = 1$ kHz | | 25°C | | 0.6 | | fA/ $\sqrt{\text{Hz}}$ | |
| THD + N | Total harmonic distortion plus noise | $V_{O(PP)} = 8$ V, $R_L = 10$ k Ω and 250 Ω , $f = 1$ kHz | $A_V = 1$ $A_V = 10$ $A_V = 100$ | 25°C | 0.002% | | | | |
| | | | | | 0.005% | | | | |
| | | | | | 0.022% | | | | |
| t _(on) | Amplifier turn-on time [‡] | $R_L = 10$ k Ω | | 25°C | 0.47 | | | μ s | |
| t _(off) | Amplifier turn-off time [‡] | | | 25°C | 2.5 | | | μ s | |
| Gain-bandwidth product | | $f = 10$ kHz, $R_L = 10$ k Ω | | 25°C | 10 | | | MHz | |
| t _s | Settling time | $V_{(STEP)PP} = 1$ V, $A_V = -1$, $C_L = 10$ pF, $R_L = 10$ k Ω | 0.1% 0.01% | 25°C | 0.17 | | | μ s | |
| | | | | | 0.22 | | | | |
| | | $V_{(STEP)PP} = 1$ V, $A_V = -1$, $C_L = 47$ pF, $R_L = 10$ k Ω | 0.1% 0.01% | | 0.17 | | | | |
| | | | | | 0.29 | | | | |
| ϕ_m | Phase margin | $R_L = 10$ k Ω , | $C_L = 50$ pF | 25°C | 37° | | | | |
| | | $R_L = 10$ k Ω , | $C_L = 0$ pF | | 42° | | | | |
| | Gain margin | $R_L = 10$ k Ω , | $C_L = 50$ pF | 25°C | 3.1 | | | dB | |
| | | $R_L = 10$ k Ω , | $C_L = 0$ pF | | 4 | | | | |

[†] Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

[‡] Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

TYPICAL CHARACTERISTICS

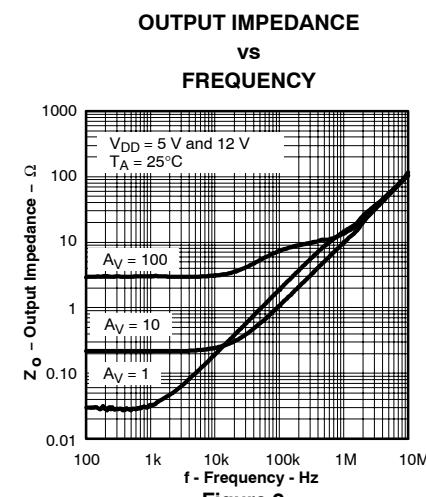
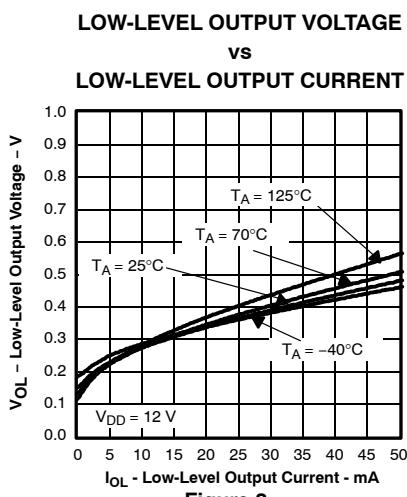
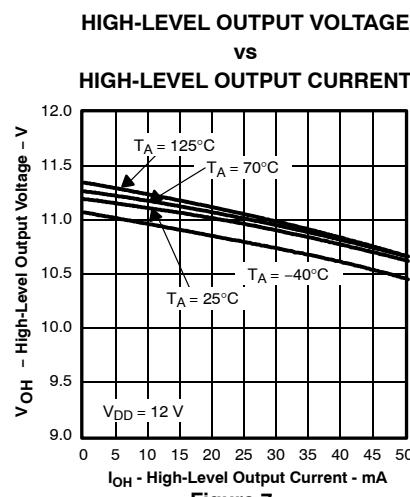
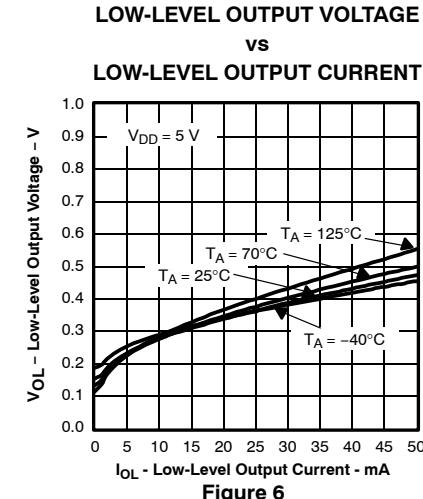
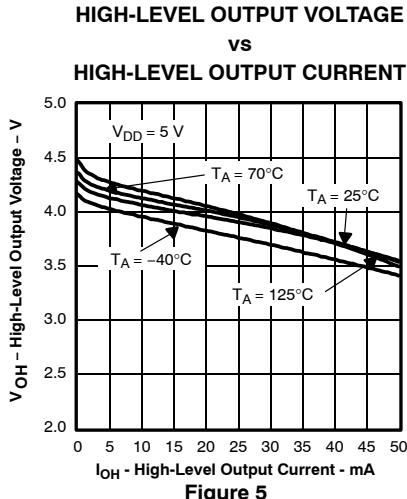
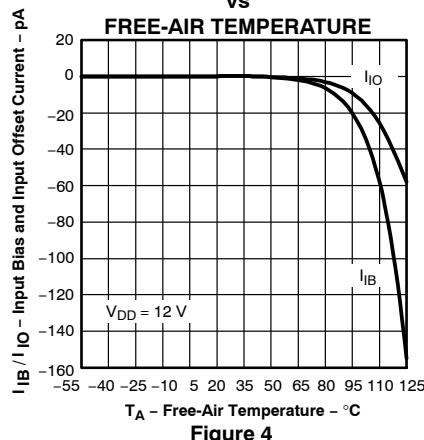
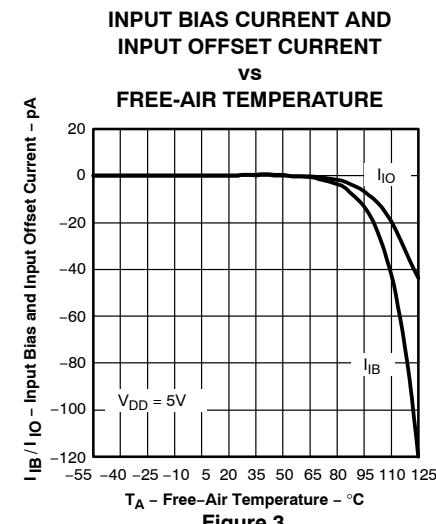
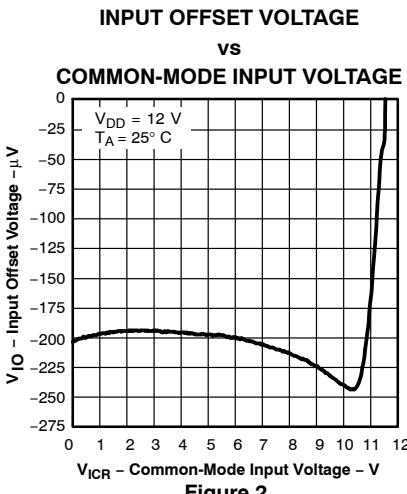
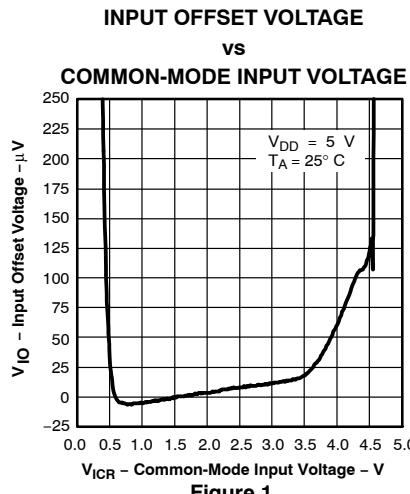
Table of Graphs

| | | FIGURE |
|-------------|---------------------------------------|--|
| V_{IO} | Input offset voltage | vs Common-mode input voltage 1, 2 |
| I_{IO} | Input offset current | vs Free-air temperature 3, 4 |
| I_{IB} | Input bias current | vs Free-air temperature 3, 4 |
| V_{OH} | High-level output voltage | vs High-level output current 5, 7 |
| V_{OL} | Low-level output voltage | vs Low-level output current 6, 8 |
| Z_o | Output impedance | vs Frequency 9 |
| I_{DD} | Supply current | vs Supply voltage 10 |
| PSRR | Power supply rejection ratio | vs Frequency 11 |
| CMRR | Common-mode rejection ratio | vs Frequency 12 |
| V_n | Equivalent input noise voltage | vs Frequency 13 |
| $V_{O(PP)}$ | Peak-to-peak output voltage | vs Frequency 14, 15 |
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| | Gain-bandwidth product | vs Supply voltage 23 |
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| | Large-signal inverting pulse response | 34, 35 |
| | Small-signal inverting pulse response | 36 |
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| | Shutdown reverse isolation | 39, 40 |
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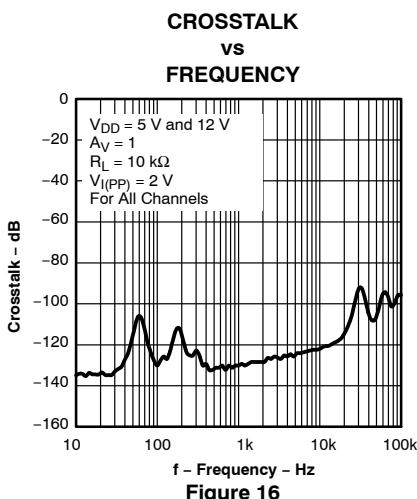
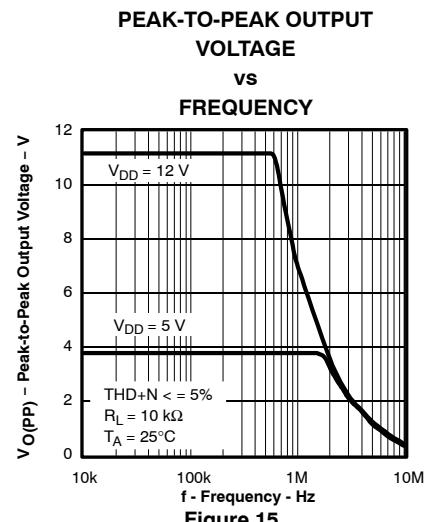
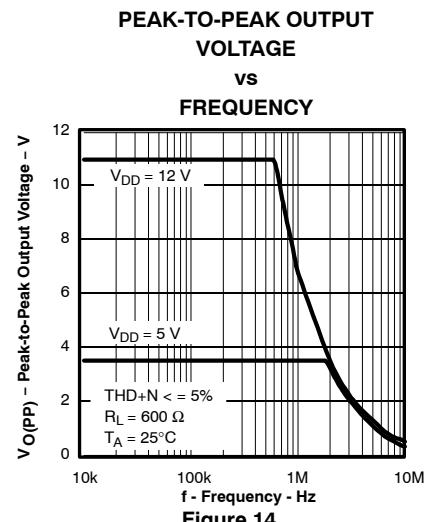
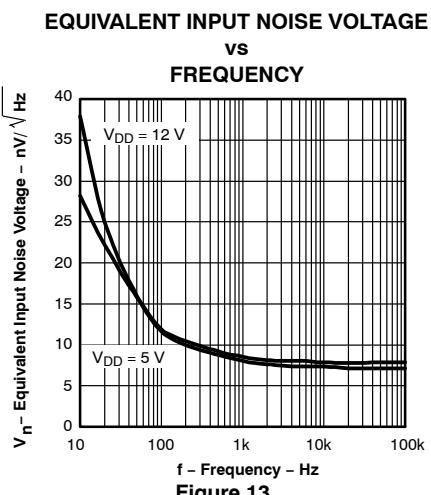
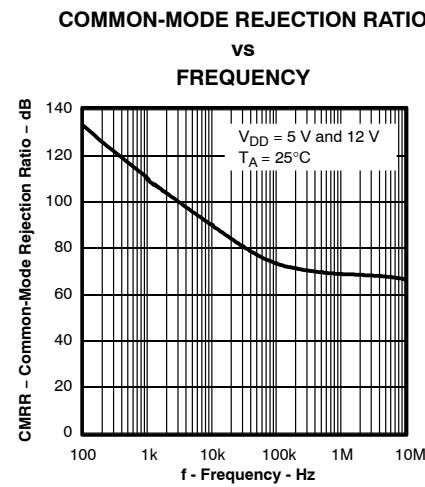
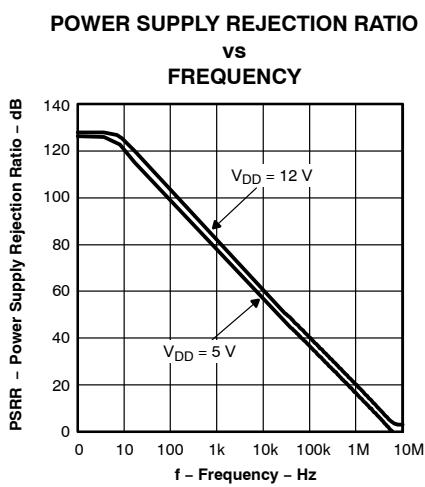
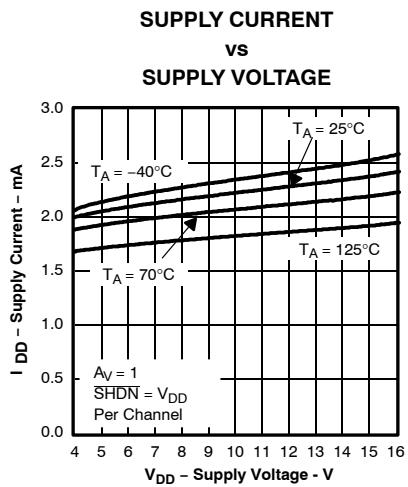
TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

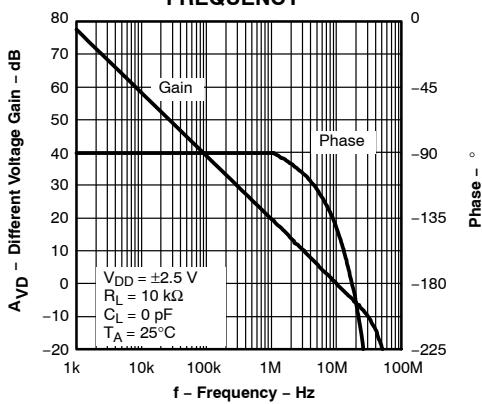


Figure 17

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

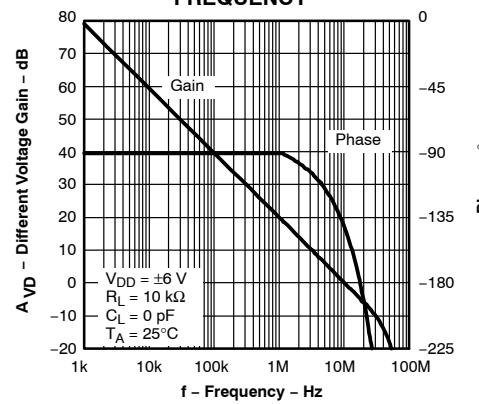


Figure 18

PHASE MARGIN vs

LOAD CAPACITANCE

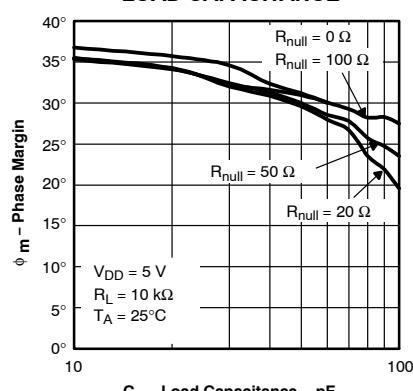


Figure 19

PHASE MARGIN vs

LOAD CAPACITANCE

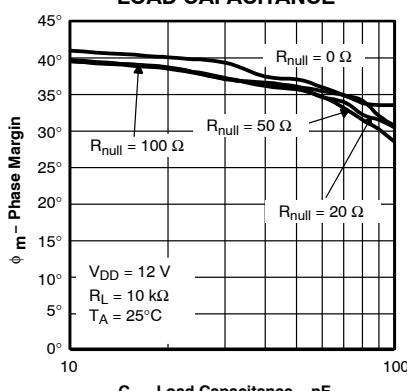


Figure 20

GAIN MARGIN vs

LOAD CAPACITANCE

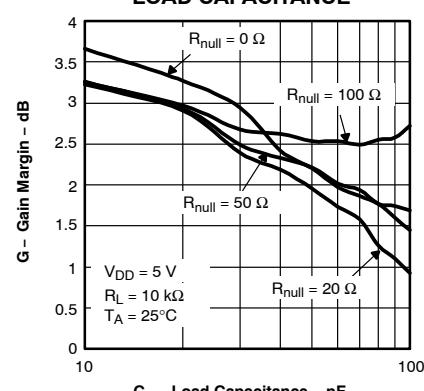


Figure 21

GAIN MARGIN vs

LOAD CAPACITANCE

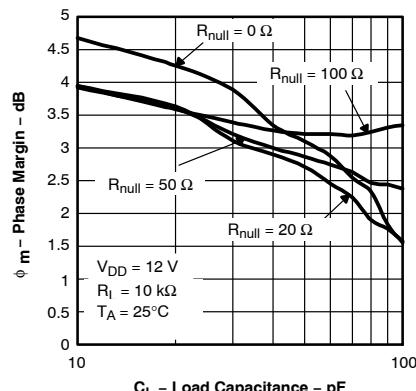


Figure 22

GAIN BANDWIDTH PRODUCT vs

SUPPLY VOLTAGE

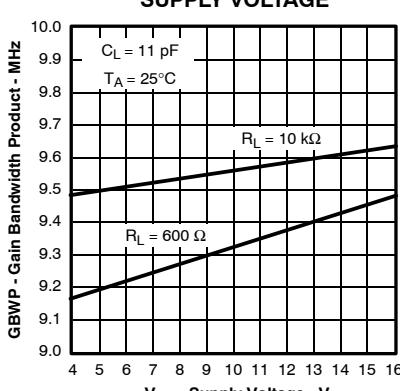


Figure 23

SLEW RATE vs

SUPPLY VOLTAGE

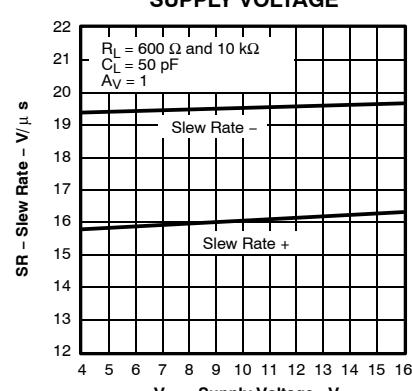


Figure 24

**TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
OPERATIONAL AMPLIFIERS**

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TYPICAL CHARACTERISTICS

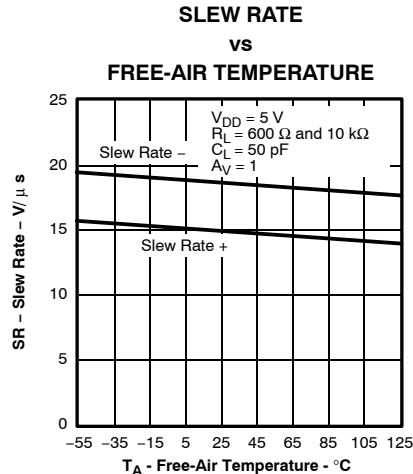


Figure 25

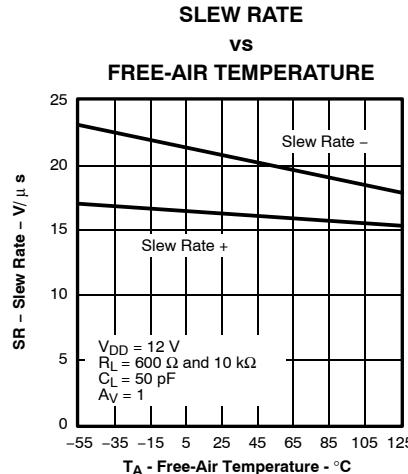


Figure 26

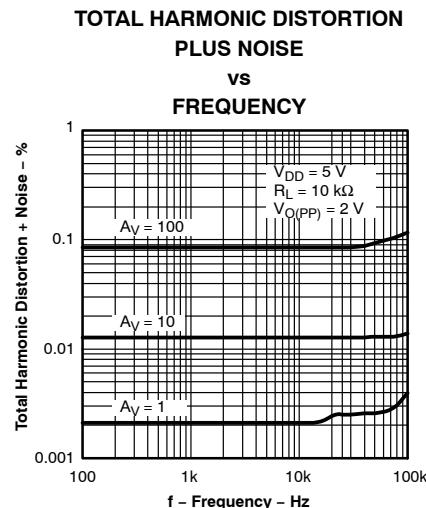


Figure 27

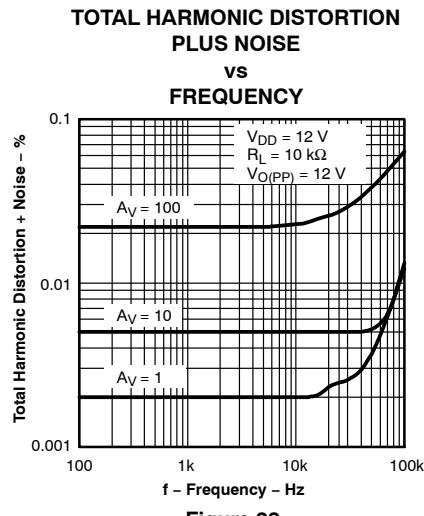


Figure 28

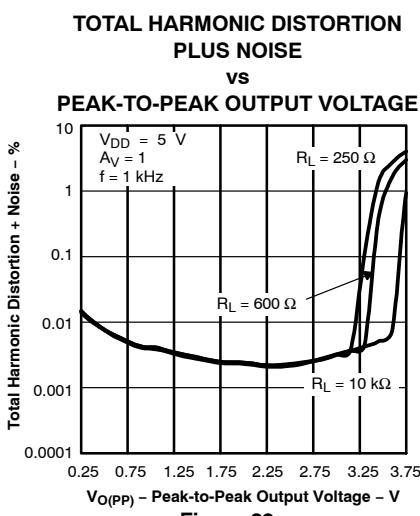


Figure 29

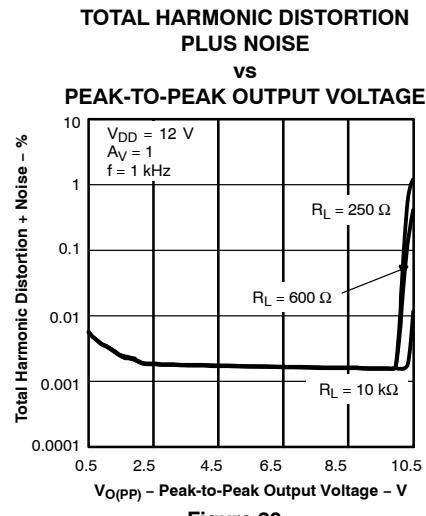


Figure 30

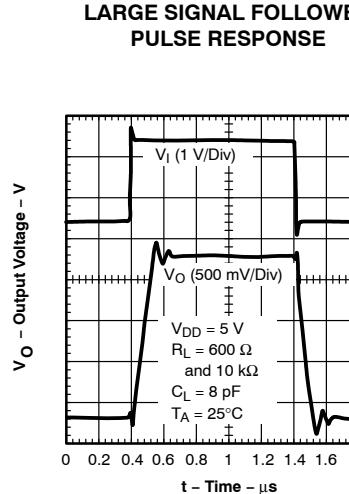


Figure 31

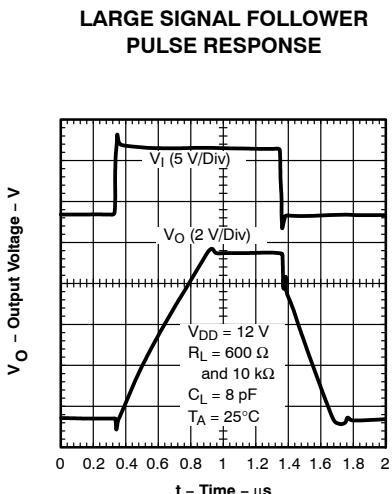


Figure 32

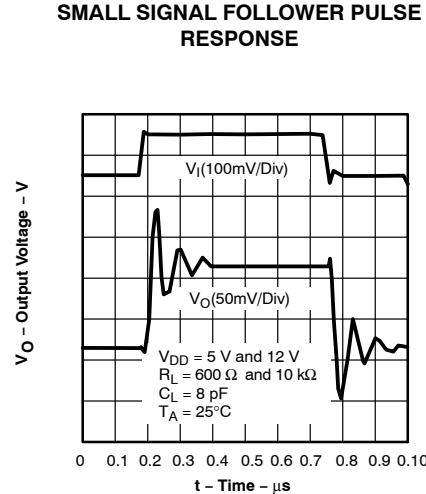


Figure 33

TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

LARGE SIGNAL INVERTING PULSE RESPONSE

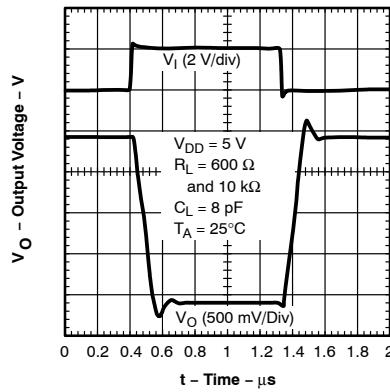


Figure 34

LARGE SIGNAL INVERTING PULSE RESPONSE

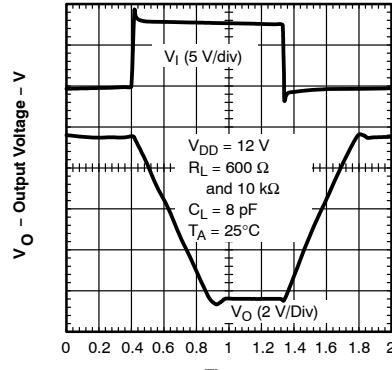


Figure 35

SMALL SIGNAL INVERTING PULSE RESPONSE

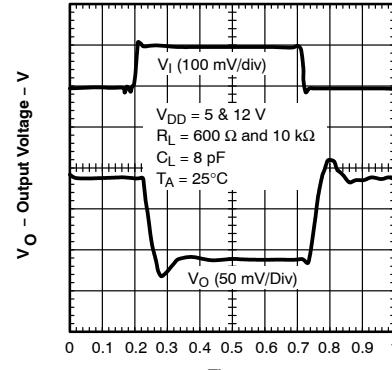


Figure 36

SHUTDOWN FORWARD ISOLATION

vs

FREQUENCY

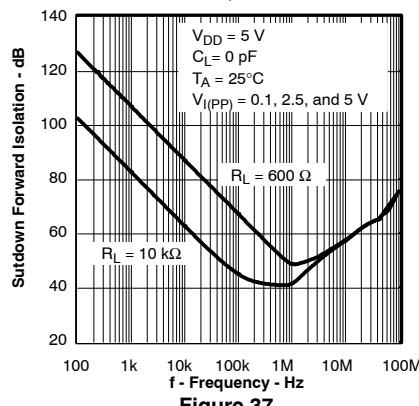


Figure 37

SHUTDOWN FORWARD ISOLATION

vs

FREQUENCY

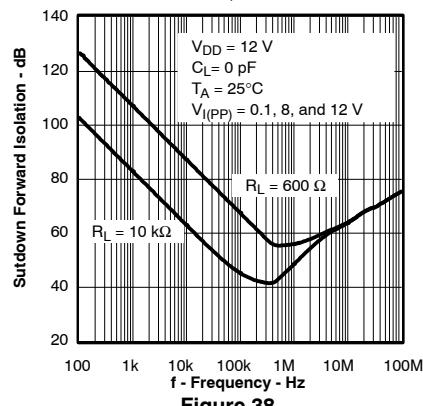


Figure 38

SHUTDOWN REVERSE ISOLATION

vs

FREQUENCY

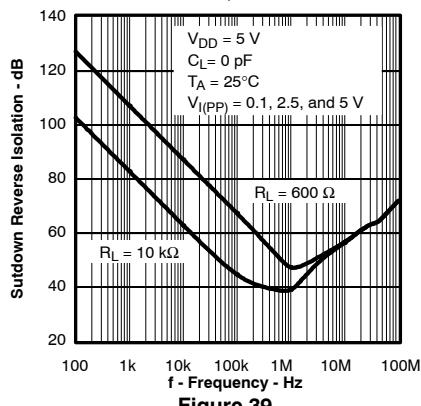


Figure 39

SHUTDOWN REVERSE ISOLATION

vs

FREQUENCY

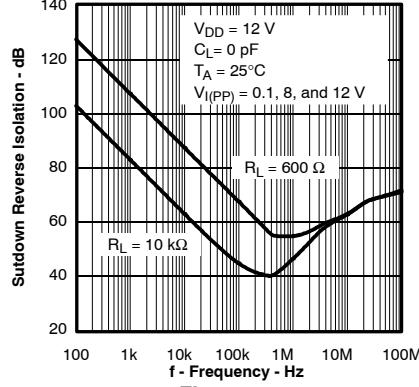


Figure 40

SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE

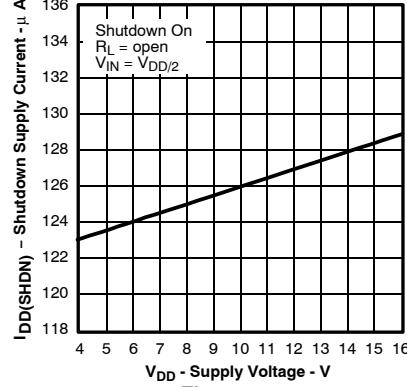


Figure 41

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

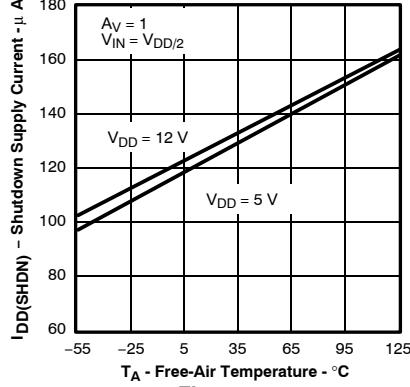
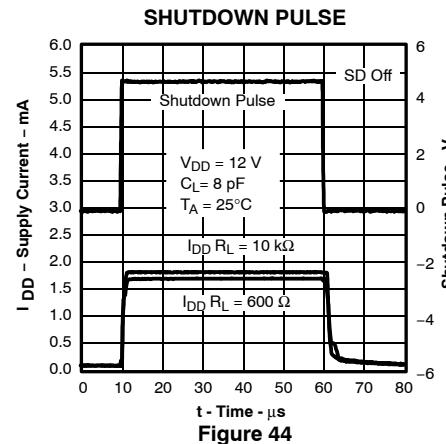
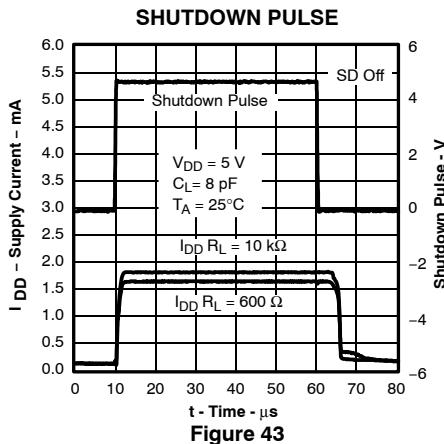


Figure 42

TYPICAL CHARACTERISTICS



PARAMETER MEASUREMENT INFORMATION

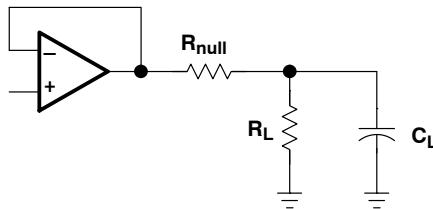
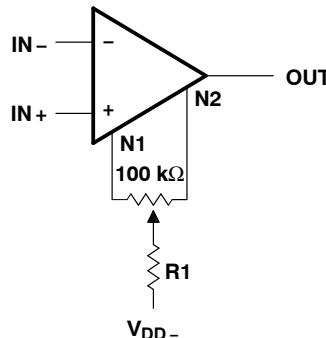


Figure 45

APPLICATION INFORMATION

input offset voltage null circuit

The TLC070 and TLC071 has an input offset nulling function. Refer to Figure 46 for the diagram.



NOTE A: $R_1 = 5.6 \text{ k}\Omega$ for offset voltage adjustment of $\pm 10 \text{ mV}$.

$R_1 = 20 \text{ k}\Omega$ for offset voltage adjustment of $\pm 3 \text{ mV}$.

Figure 46. Input Offset Voltage Null Circuit

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APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 47. A minimum value of 20 Ω should work well for most applications.

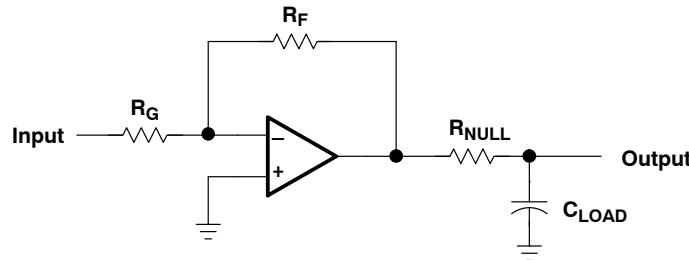


Figure 47. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

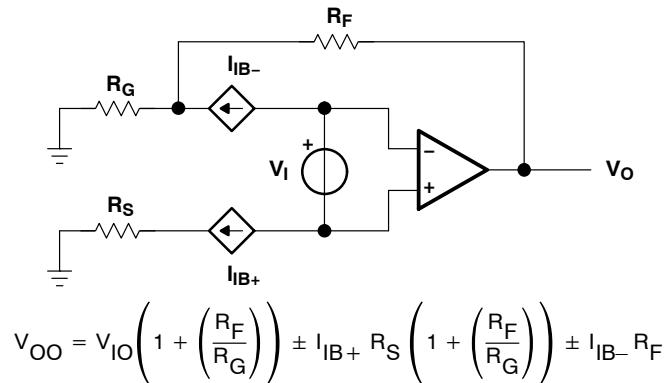


Figure 48. Output Offset Voltage Model

APPLICATION INFORMATION

high speed CMOS input amplifiers

The TLC07x is a family of high-speed low-noise CMOS input operational amplifiers that has an input capacitance of the order of 20 pF. Any resistor used in the feedback path adds a pole in the transfer function equivalent to the input capacitance multiplied by the combination of source resistance and feedback resistance. For example, a gain of -10, a source resistance of 1 k Ω , and a feedback resistance of 10 k Ω add an additional pole at approximately 8 MHz. This is more apparent with CMOS amplifiers than bipolar amplifiers due to their greater input capacitance.

This is of little consequence on slower CMOS amplifiers, as this pole normally occurs at frequencies above their unity-gain bandwidth. However, the TLC07x with its 10-MHz bandwidth means that this pole normally occurs at frequencies where there is on the order of 5 dB gain left and the phase shift adds considerably.

The effect of this pole is the strongest with large feedback resistances at small closed loop gains. As the feedback resistance is increased, the gain peaking increases at a lower frequency and the 180° phase shift crossover point also moves down in frequency, decreasing the phase margin.

For the TLC07x, the maximum feedback resistor recommended is 5 k Ω ; larger resistances can be used but a capacitor in parallel with the feedback resistor is recommended to counter the effects of the input capacitance pole.

The TLC073 with a 1-V step response has an 80% overshoot with a natural frequency of 3.5 MHz when configured as a unity gain buffer and with a 10-k Ω feedback resistor. By adding a 10-pF capacitor in parallel with the feedback resistor, the overshoot is reduced to 40% and eliminates the natural frequency, resulting in a much faster settling time (see Figure 49). The 10-pF capacitor was chosen for convenience only.

Load capacitance had little effect on these measurements due to the excellent output drive capability of the TLC07x.

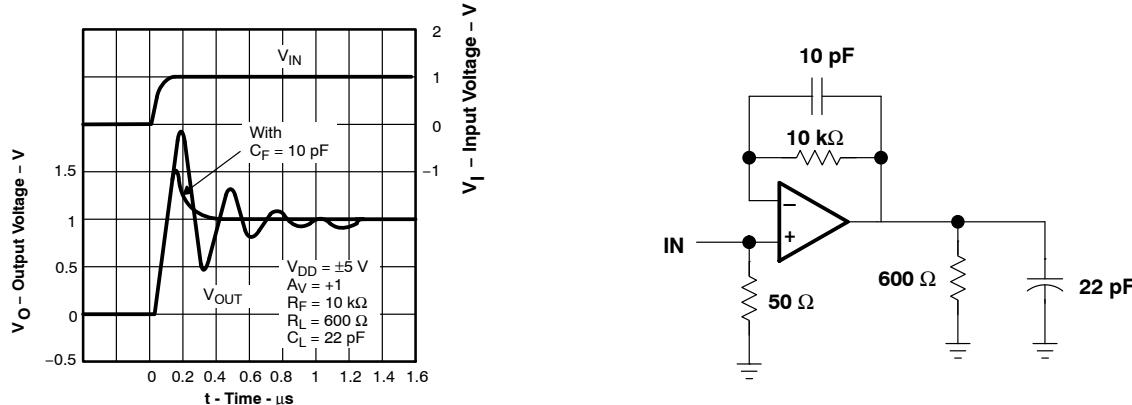


Figure 49. 1-V Step Response

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APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 50).

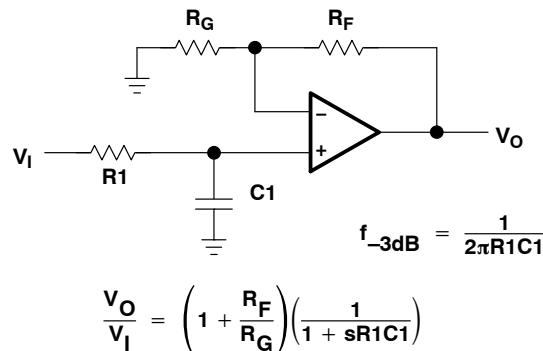


Figure 50. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

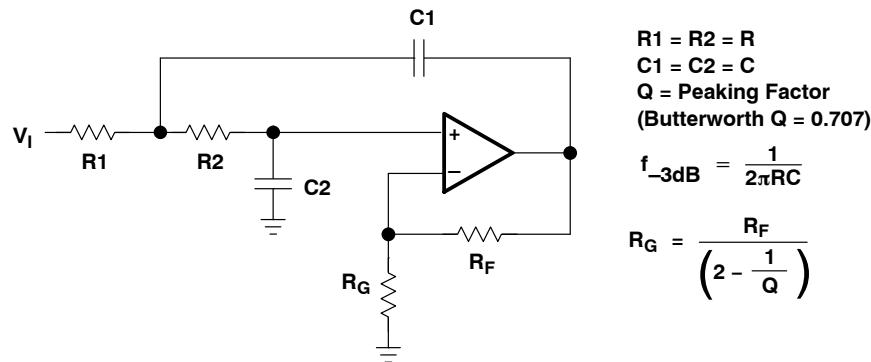


Figure 51. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

shutdown function

Three members of the TLC07x family (TLC070/3/5) have a shutdown terminal (SHDN) for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 125 μ A/channel, the amplifier is disabled, and the outputs are placed in a high-impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to the voltage on the GND terminal of the device. Therefore, when operating the device with split supply voltages (e.g. ± 2.5 V), the shutdown terminal needs to be pulled to V_{DD-} (not system ground) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 43 and 44. The amplifier is powered with a single 5-V supply and is configured as noninverting with a gain of 5. The amplifier turn-on and turn-off times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figures 37, 38, 39, and 40 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency using 0.1 V_{PP} , 2.5 V_{PP} , and 5 V_{PP} input signals at ± 2.5 V supplies and 0.1 V_{PP} , 8 V_{PP} , and 12 V_{PP} input signals at ± 6 V supplies.

circuit layout considerations

To achieve the levels of high performance of the TLC07x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- **Ground planes** – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- **Proper power supply decoupling** – Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- **Sockets** – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs/compact part placements** – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- **Surface-mount passive components** – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

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APPLICATION INFORMATION

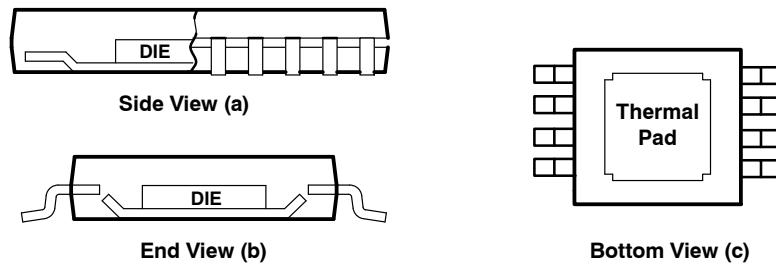
general PowerPAD design considerations

The TLC07x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 52(a) and Figure 52(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 52(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

Soldering the PowerPAD to the PCB is always required, even with applications that have low-power dissipation. This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with mechanical methods of heatsinking.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 52. Views of Thermally-Enhanced DGN Package

APPLICATION INFORMATION

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

general PowerPAD design considerations (continued)

1. The thermal pad must be connected to the same voltage potential as the GND pin.
2. Prepare the PCB with a top side etch pattern as illustrated in the thermal land pattern mechanical drawing at the end of this document. There should be etch for the leads as well as etch for the thermal pad.
3. Place five holes (single and dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLC07x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane that is the same potential as the device GND pin.
6. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLC07x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
9. With these preparatory steps in place, the TLC07x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA} , the maximum power dissipation is shown in Figure 54 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLC07x IC (watts)

T_{MAX} = Absolute maximum junction temperature (150°C)

T_A = Free-ambient air temperature (°C)

θ_{JA} = $\theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

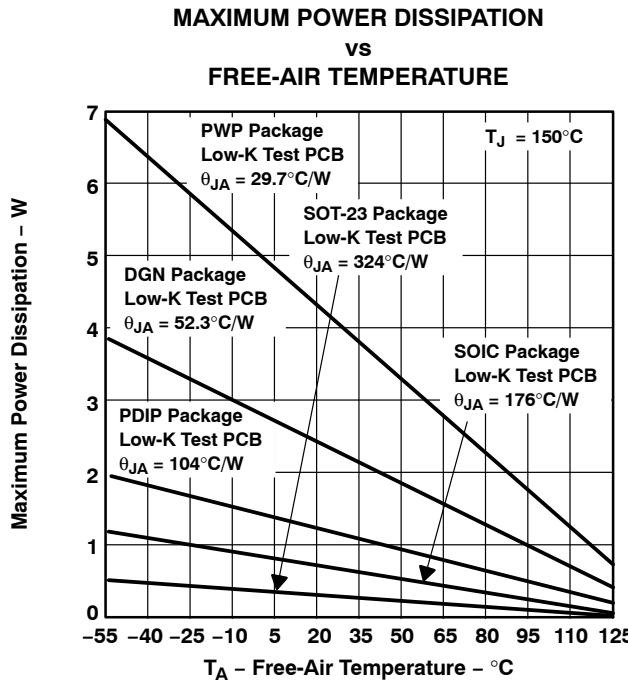
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

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APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

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macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 1) and subcircuit in Figure 55 are generated using the TLC07x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

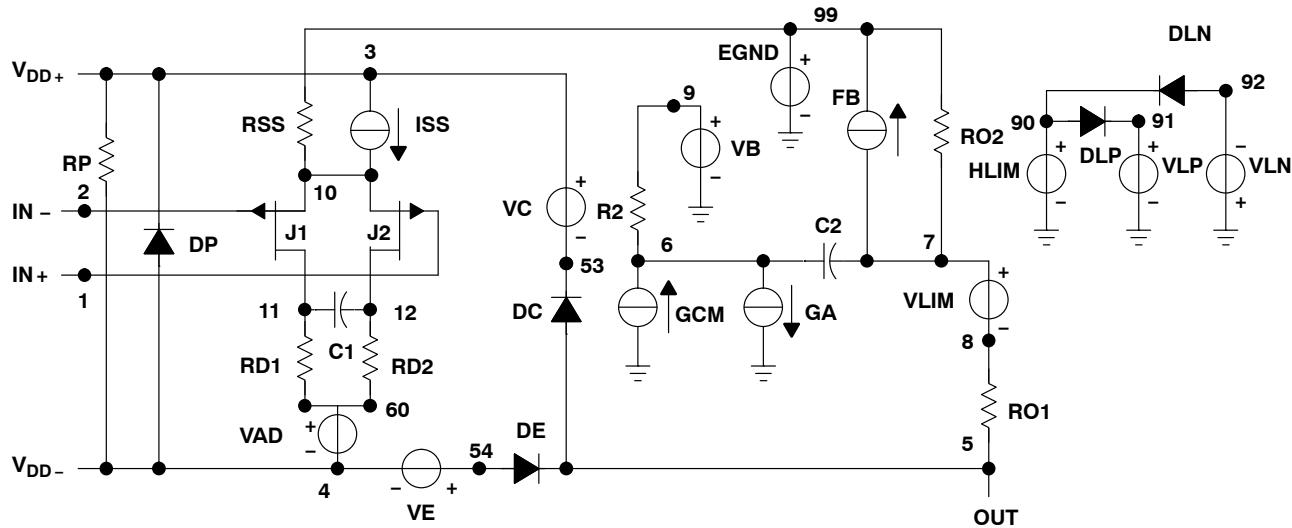
NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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APPLICATION INFORMATION



*DEVICE=TLC07X_5V, OPAMP, PJF, INT

* TLC07X – 5V operational amplifier "macromodel" subcircuit

* created using Parts release 8.0 on 12/16/99 at 08:38

* Parts is a MicroSim product.

*

* connections:
 * non-inverting input
 * inverting input
 * positive power supply
 * negative power supply
 * output
 *

.subckt TLC07X_5V 1 2 3 4 5

*

c1 11 12 4.8697E-12
 c2 6 7 8.0000E-12
 css 10 99 4.0063E-12
 dc 5 53 dy
 de 54 5 dy
 dlp 90 91 dx
 dln 92 90 dx
 dp 4 3 dx
 egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
 fb 7 99 poly(5) vb vc ve vlp vln 0 6.9132E6 -1E3 1E3
 6E6 -6E6

| | | | | |
|--------|-----|--|------|--------------|
| ga | 6 | 0 | 11 | 12 457.42E-6 |
| gcm | 0 | 6 | 10 | 99 1.1293E-6 |
| iss | 3 | 10 | dc | 183.67E-6 |
| ioff | 0 | 6 | dc | .806E-6 |
| hlim | 90 | 0 | vlim | 1K |
| j1 | 11 | 2 | 10 | jx1 |
| j2 | 12 | 1 | 10 | jx2 |
| r2 | 6 | 9 | | 100.00E3 |
| rd1 | 4 | 11 | | 2.1862E3 |
| rd2 | 4 | 12 | | 2.1862E3 |
| ro1 | 8 | 5 | 10 | |
| ro2 | 7 | 99 | 10 | |
| rp | 3 | 4 | | 2.4728E3 |
| rss | 10 | 99 | | 1.0889E6 |
| vb | 9 | 0 | dc | 0 |
| vc | 3 | 53 | dc | 1.5410 |
| ve | 54 | 4 | dc | .84403 |
| vlim | 7 | 8 | dc | 0 |
| vlp | 91 | 0 | dc | 119 |
| vln | 0 | 92 | dc | 119 |
| .model | dx | D(ls=800.00E-18) | | |
| .model | dy | D(ls=800.00E-18 Rs=1m Cjo=10p) | | |
| .model | jx1 | PJF(ls=117.50E-15 Beta=1.1391E-3 Vto=-1) | | |
| .model | jx2 | PJF(ls=117.50E-15 Beta=1.1391E-3 Vto=-1) | | |
| .ends | | | | |

Figure 54. Boyle Macromodel and Subcircuit

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|---------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| TLC070AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C070AI | Samples |
| TLC070AIP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC070AI | Samples |
| TLC070AIPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC070AI | Samples |
| TLC070CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C070C | Samples |
| TLC070CDGNR | OBsolete | MSOP-PowerPAD | DGN | 8 | | TBD | Call TI | Call TI | 0 to 70 | ACS | |
| TLC070CDGNRG4 | OBsolete | MSOP-PowerPAD | DGN | 8 | | TBD | Call TI | Call TI | 0 to 70 | | |
| TLC070CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C070C | Samples |
| TLC070ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C070I | Samples |
| TLC070IDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ACT | Samples |
| TLC070IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C070I | Samples |
| TLC070IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC070I | Samples |
| TLC071AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C071AI | Samples |
| TLC071AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C071AI | Samples |
| TLC071AIP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC071AI | Samples |
| TLC071AIPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC071AI | Samples |
| TLC071CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C071C | Samples |
| TLC071CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C071C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|---------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLC071CDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ACU | Samples |
| TLC071CDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ACU | Samples |
| TLC071CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C071C | Samples |
| TLC071CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLC071C | Samples |
| TLC071CPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLC071C | Samples |
| TLC071ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C071I | Samples |
| TLC071IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C071I | Samples |
| TLC071IDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ACV | Samples |
| TLC071IDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ACV | Samples |
| TLC071IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C071I | Samples |
| TLC071IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC071I | Samples |
| TLC072AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C072AI | Samples |
| TLC072AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C072AI | Samples |
| TLC072AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C072AI | Samples |
| TLC072AIDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C072AI | Samples |
| TLC072AIP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | C072AI | Samples |
| TLC072AIP4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | C072AI | Samples |
| TLC072CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C072C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|---------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| TLC072CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C072C | Samples |
| TLC072CDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ADV | Samples |
| TLC072CDGNG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ADV | Samples |
| TLC072CDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ADV | Samples |
| TLC072CDGNRG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ADV | Samples |
| TLC072CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C072C | Samples |
| TLC072CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C072C | Samples |
| TLC072CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | C072C | Samples |
| TLC072CPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | C072C | Samples |
| TLC072ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C072I | Samples |
| TLC072IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C072I | Samples |
| TLC072IDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADW | Samples |
| TLC072IDGNG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADW | Samples |
| TLC072IDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADW | Samples |
| TLC072IDGNRG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADW | Samples |
| TLC072IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C072I | Samples |
| TLC072IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C072I | Samples |
| TLC072IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | C072I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|---------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLC072IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | C072I | Samples |
| TLC073AID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C073AI | Samples |
| TLC073AIDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C073AI | Samples |
| TLC073CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C073C | Samples |
| TLC073CDGQ | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ADX | Samples |
| TLC073CDGQG4 | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ADX | Samples |
| TLC073CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | C073C | Samples |
| TLC073IDGQ | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADY | Samples |
| TLC073IDGQR | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADY | Samples |
| TLC073IDGQRG4 | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ADY | Samples |
| TLC073IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | C073I | Samples |
| TLC074AID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC074AI | Samples |
| TLC074AIDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC074AI | Samples |
| TLC074AIDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC074AI | Samples |
| TLC074AIDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC074AI | Samples |
| TLC074AIN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC074AI | Samples |
| TLC074AIPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | TBD | Call TI | Call TI | -40 to 125 | TLC074AI | Samples |
| TLC074CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC074C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLC074CDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC074C | Samples |
| TLC074CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC074C | Samples |
| TLC074CDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC074C | Samples |
| TLC074CN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLC074C | Samples |
| TLC074CNE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLC074C | Samples |
| TLC074CPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TLC074C | Samples |
| TLC074CPWPG4 | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TLC074C | Samples |
| TLC074CPWPR | ACTIVE | HTSSOP | PWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TLC074C | Samples |
| TLC074ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC074I | Samples |
| TLC074IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC074I | Samples |
| TLC074IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC074I | Samples |
| TLC074IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC074I | Samples |
| TLC074IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC074I | Samples |
| TLC074IPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLC074I | Samples |
| TLC075AID | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC075AI | Samples |
| TLC075AIDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC075AI | Samples |
| TLC075AIDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLC075AI | Samples |
| TLC075AIN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC075AI | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| TLC075AIPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLC075AI | Samples |
| TLC075CD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC075C | Samples |
| TLC075CN | OBsolete | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | TLC075C | |
| TLC075CNE4 | ACTIVE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | Samples |
| TLC075CPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TLC075C | Samples |
| TLC075IPWP | ACTIVE | HTSSOP | PWP | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLC075I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

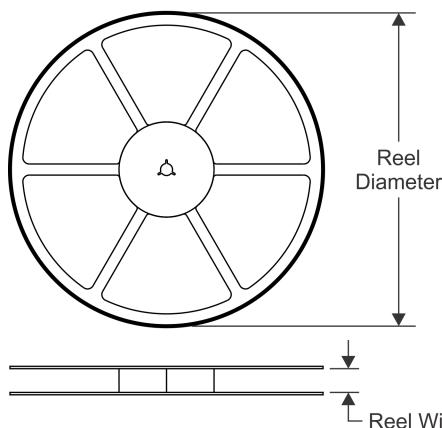
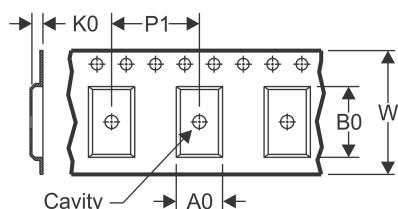
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC072 :

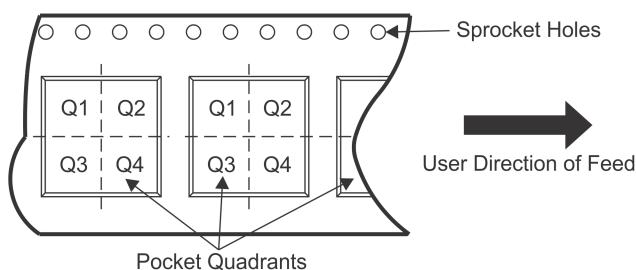
- Automotive: [TLC072-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


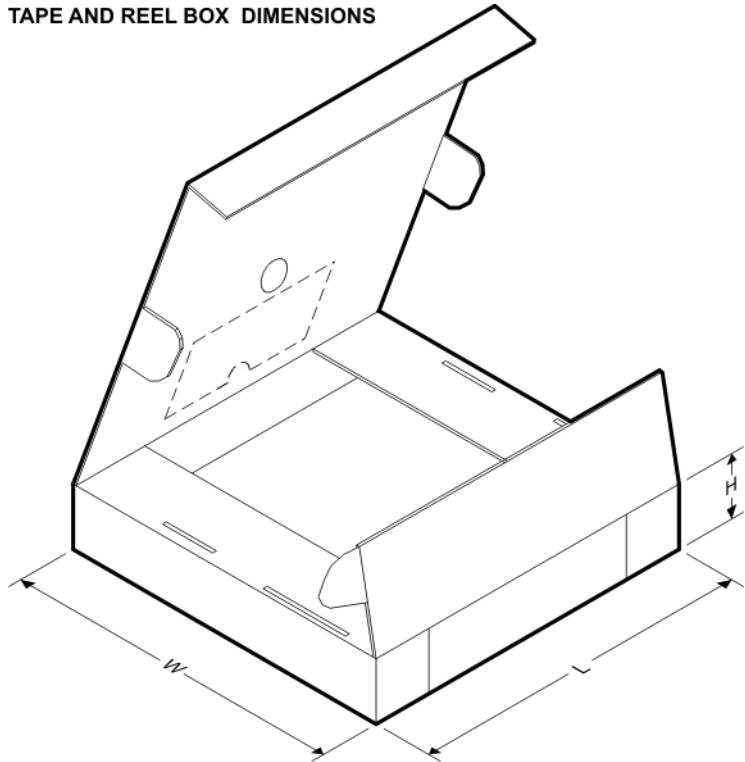
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|----------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC070CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC070IDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLC070IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC070IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC071CDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLC071CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC071IDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLC071IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC072AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC072CDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLC072CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC072IDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|----------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| | PAD | | | | | | | | | | | |
| TLC072IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC073AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC073CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC073IDGQR | MSOP-Power PAD | DGQ | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLC074AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC074CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC074CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC074CPWPR | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TLC074IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC075AIDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


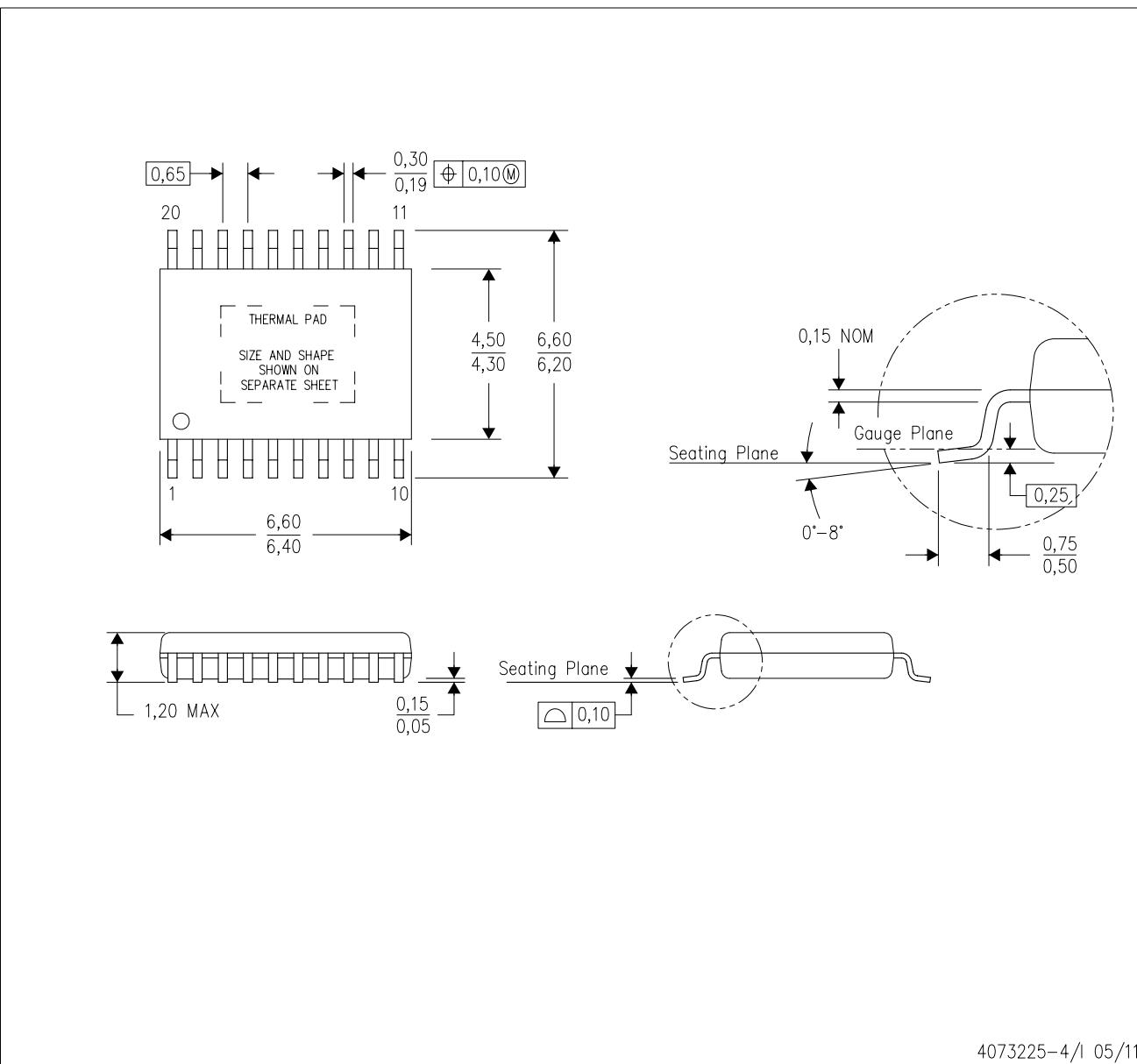
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|---------------|-----------------|------|------|-------------|------------|-------------|
| TLC070CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC070IDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLC070IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC070IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|---------------|-----------------|------|------|-------------|------------|-------------|
| TLC071CDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLC071CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC071IDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLC071IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC072AIDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC072CDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLC072CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC072IDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLC072IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC073AIDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC073CDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC073IDGQR | MSOP-PowerPAD | DGQ | 10 | 2500 | 358.0 | 335.0 | 35.0 |
| TLC074AIDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC074CDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC074CDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLC074CPWPR | HTSSOP | PWP | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TLC074IDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC075AIDR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G20)

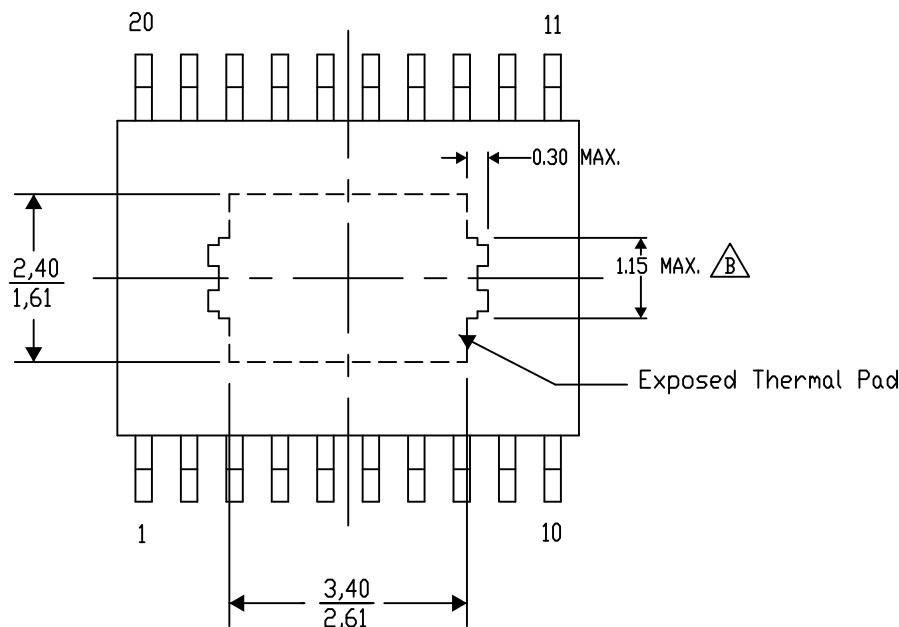
PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-15/AH 11/13

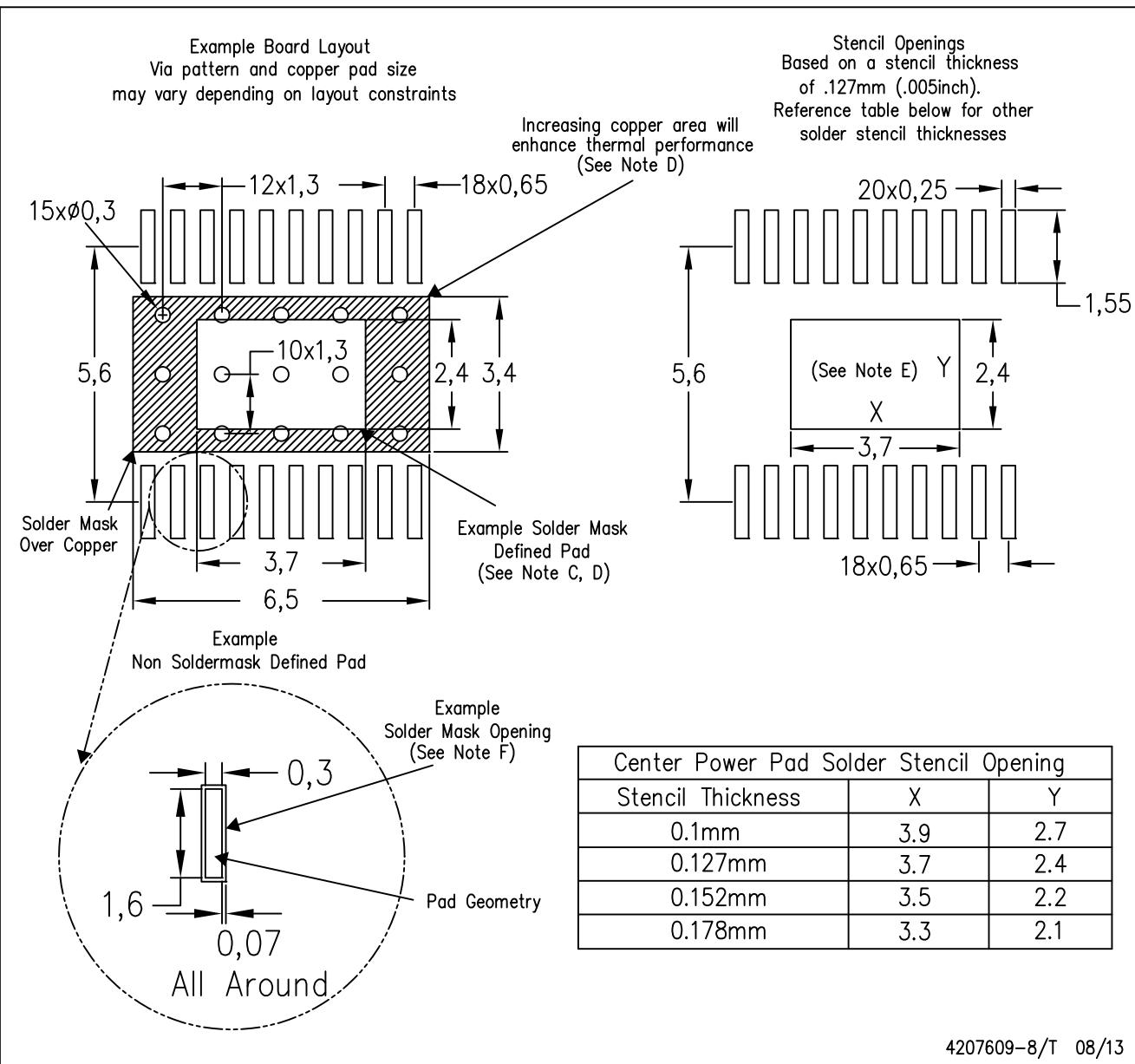
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE

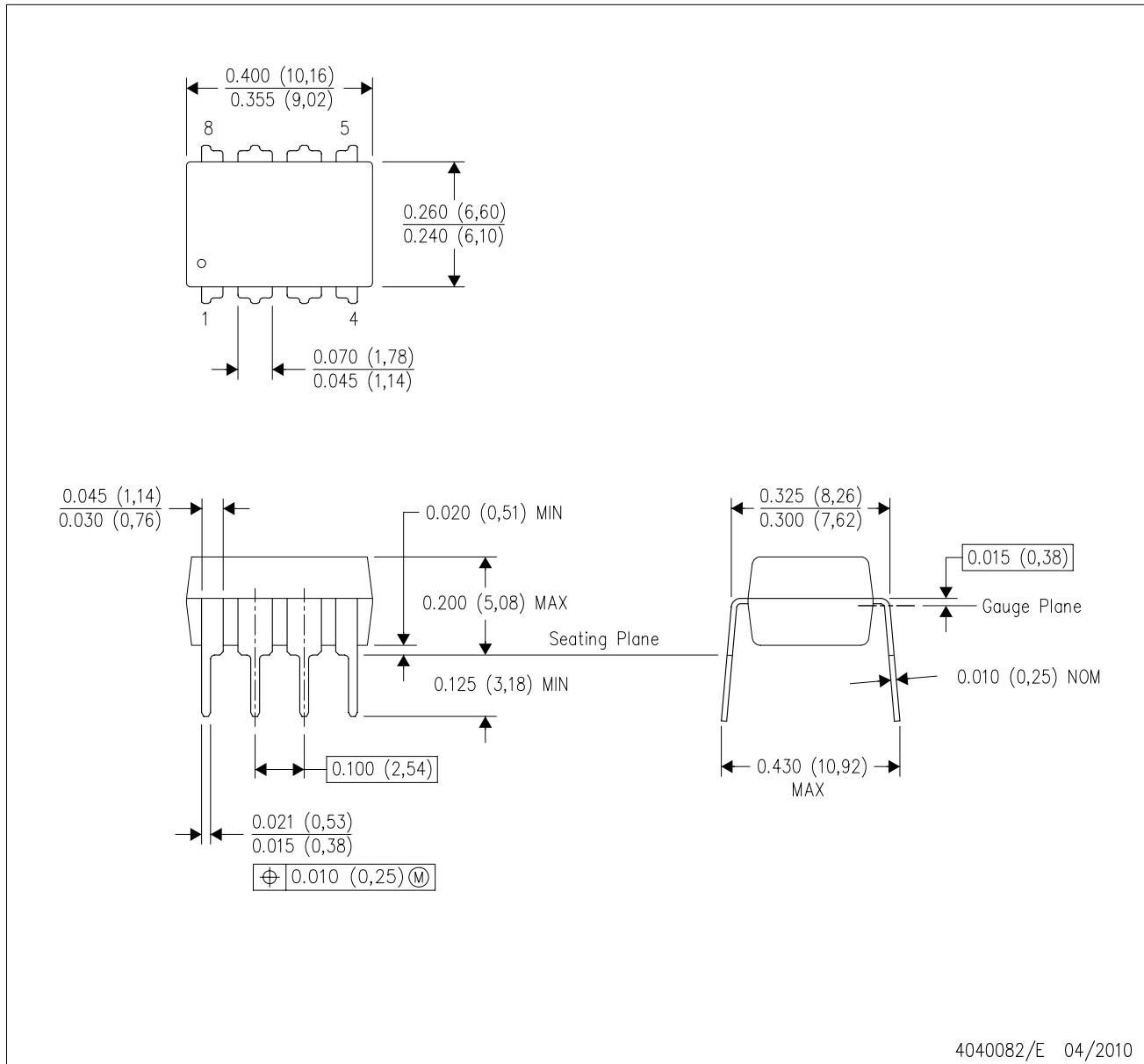


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

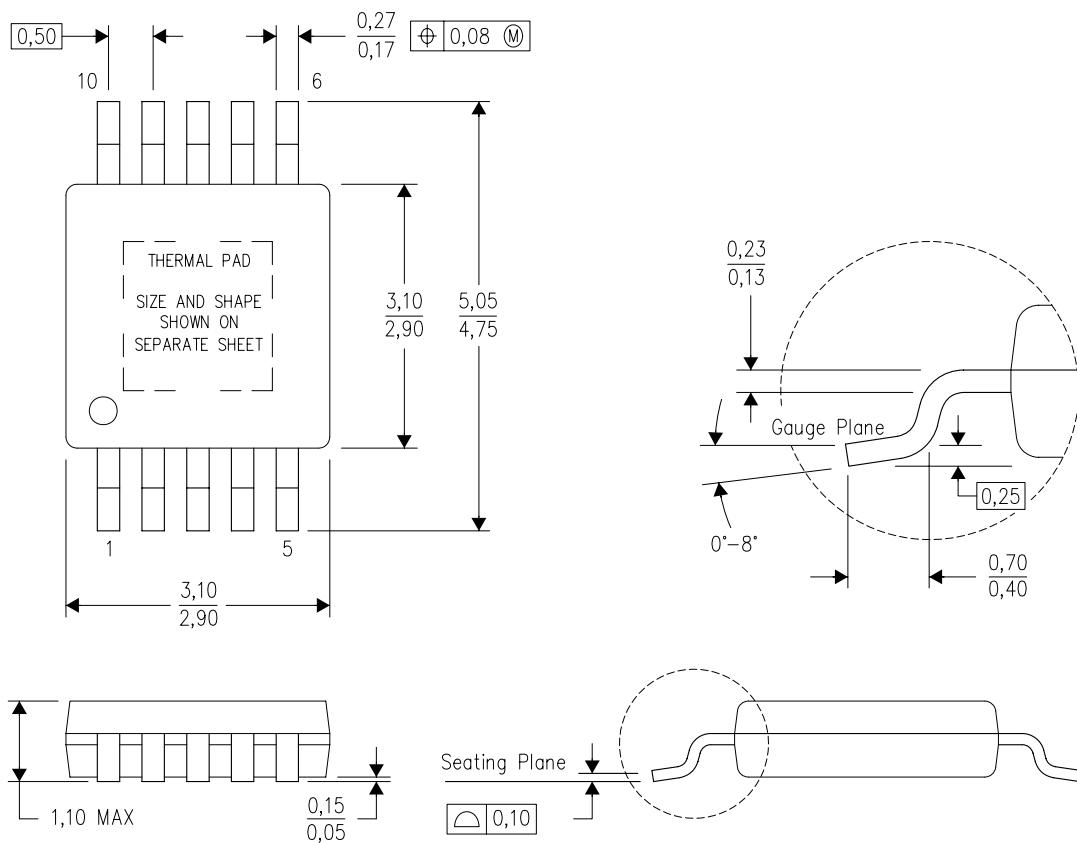


NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 variation BA.

4040082/E 04/2010

DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL OUTLINE



4073273/F 11/11

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC M0-187 variation BA-T.

PowerPAD is a trademark of Texas Instruments.

DGQ (S-PDSO-G10)

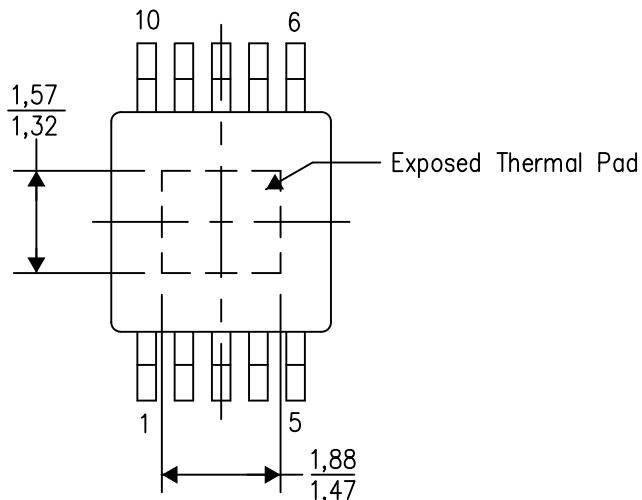
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206324-2/G 05/13

NOTE: A. All linear dimensions are in millimeters

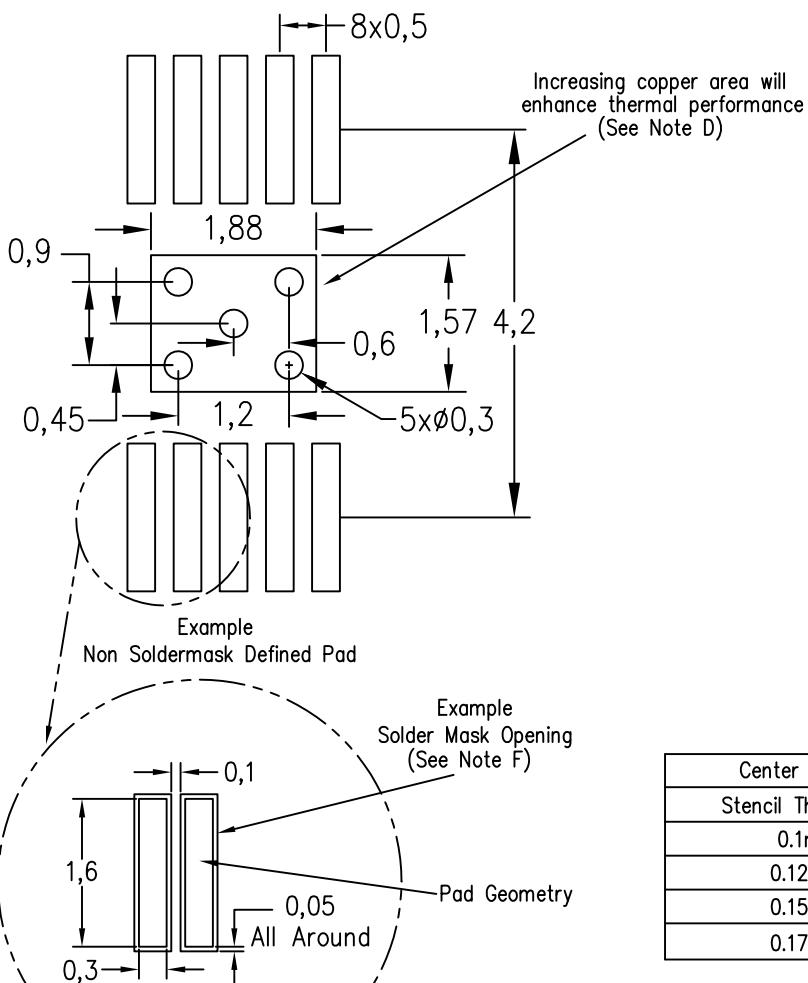
PowerPAD is a trademark of Texas Instruments

LAND PATTERN DATA

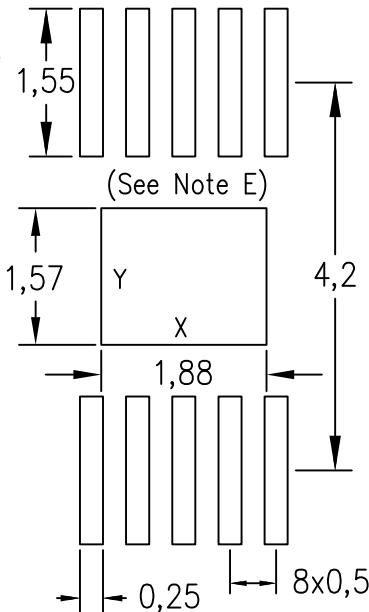
DGQ (S-PDS0-G10)

PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses



| Center Power Pad | Solder Stencil | Opening |
|-------------------|----------------|---------|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.88 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

4207733-2/E 11/12

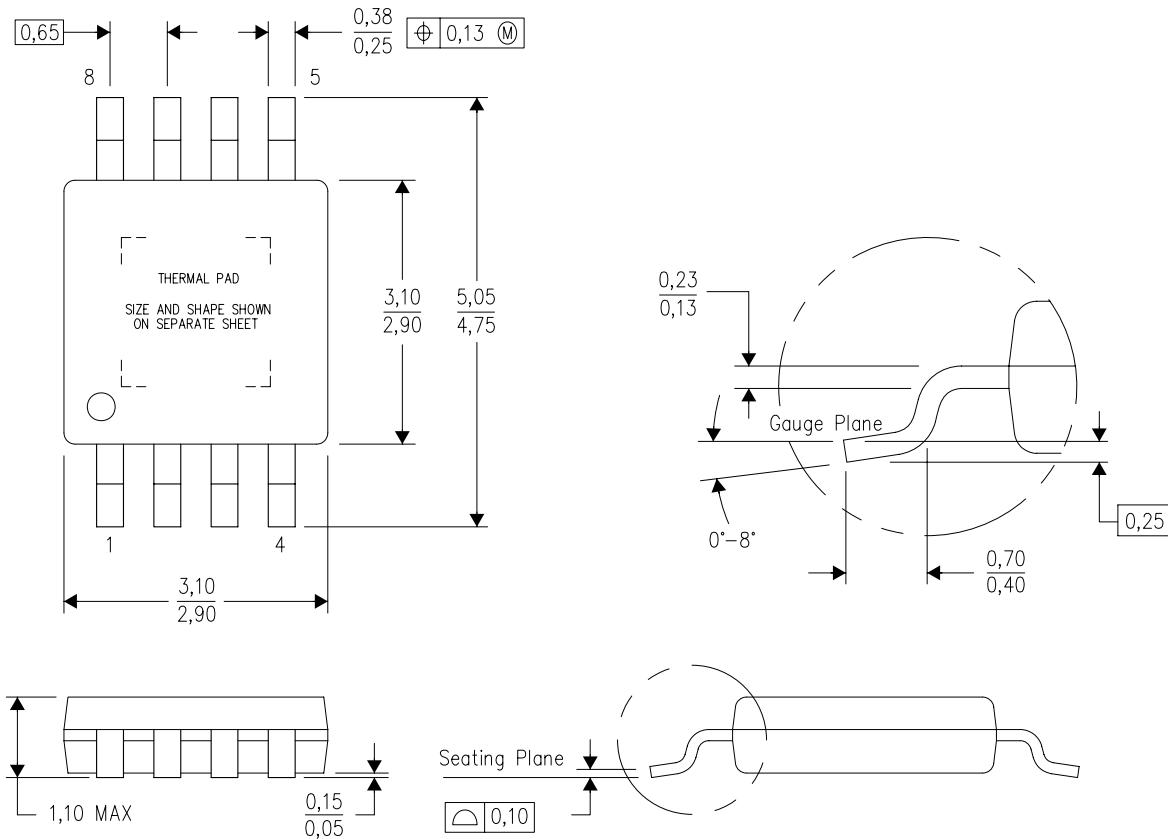
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



4073271/F 05/11

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

DGN (S-PDSO-G8)

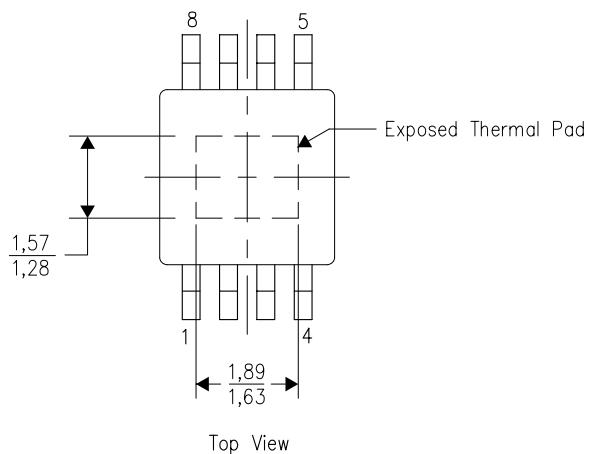
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

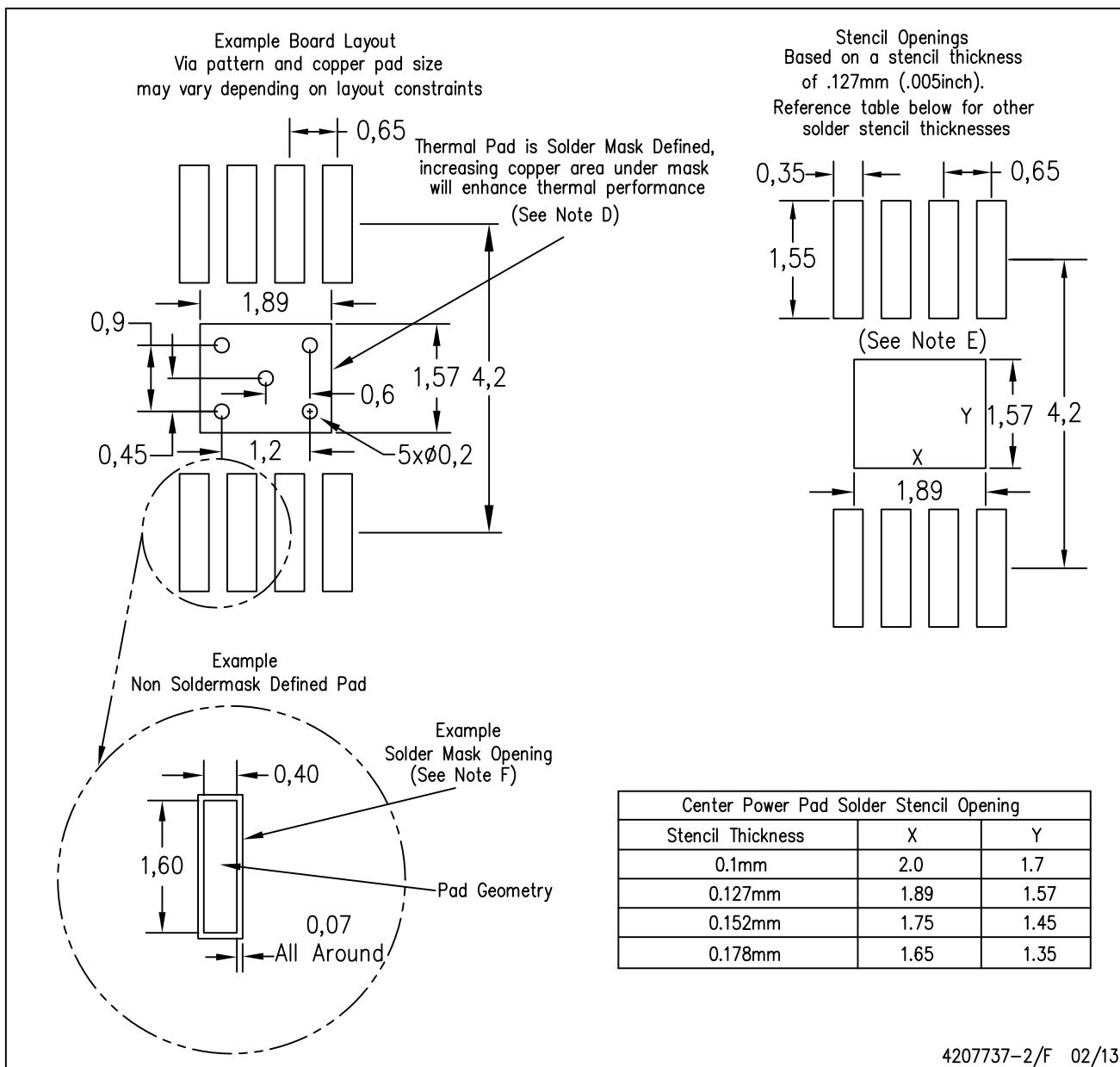


Exposed Thermal Pad Dimensions

4206323-2/1 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



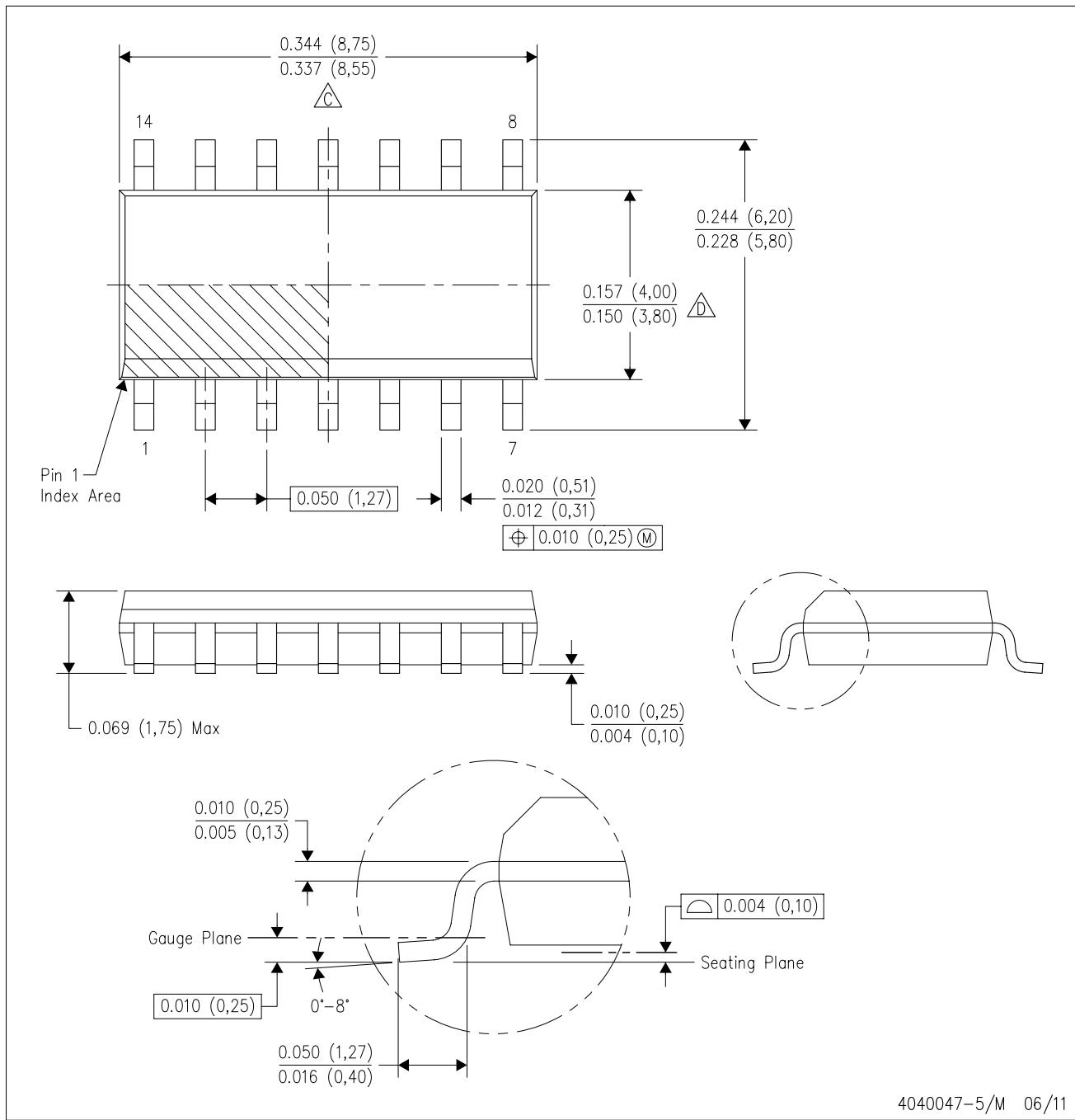
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com (<http://www.ti.com>).
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

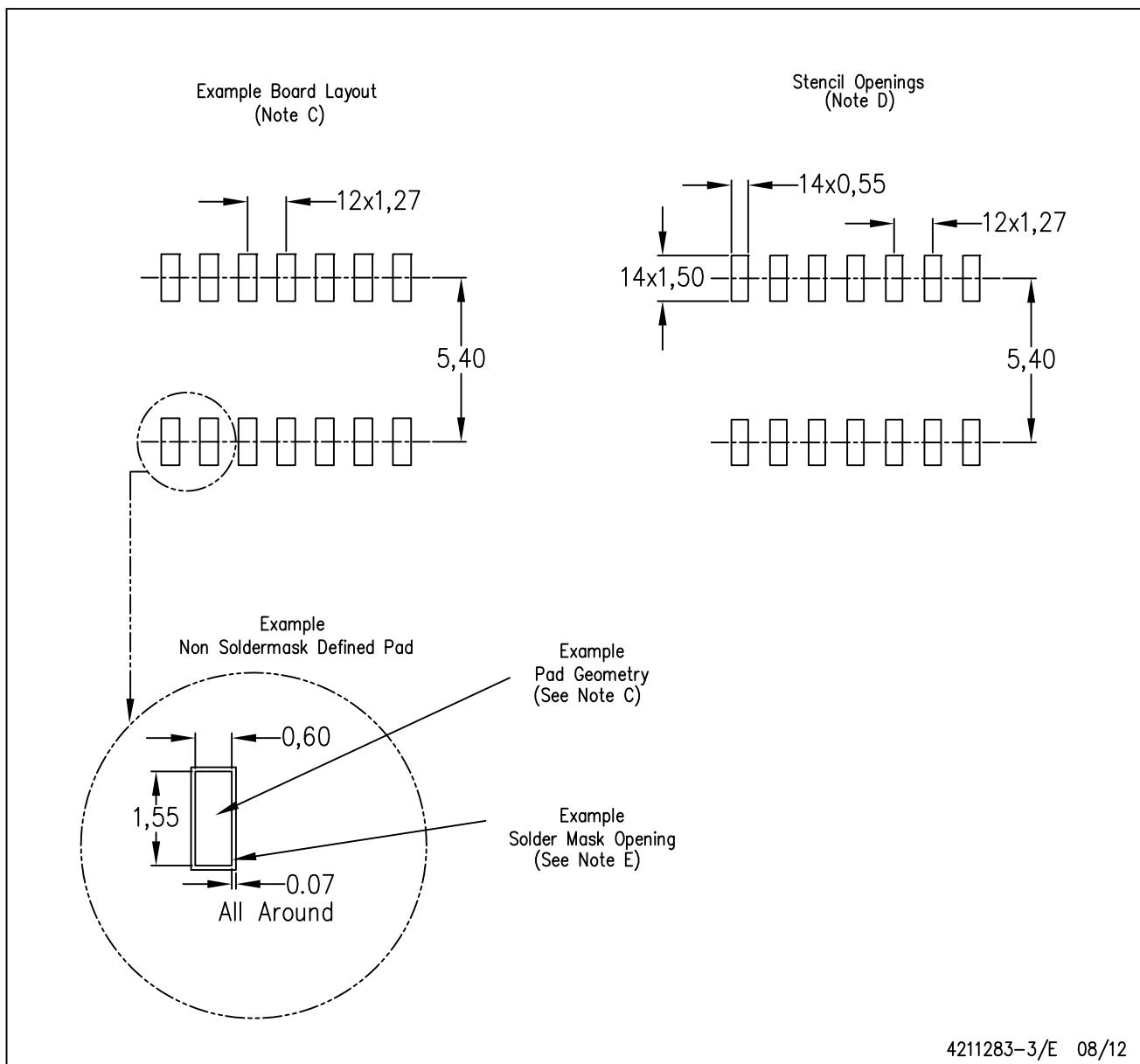
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



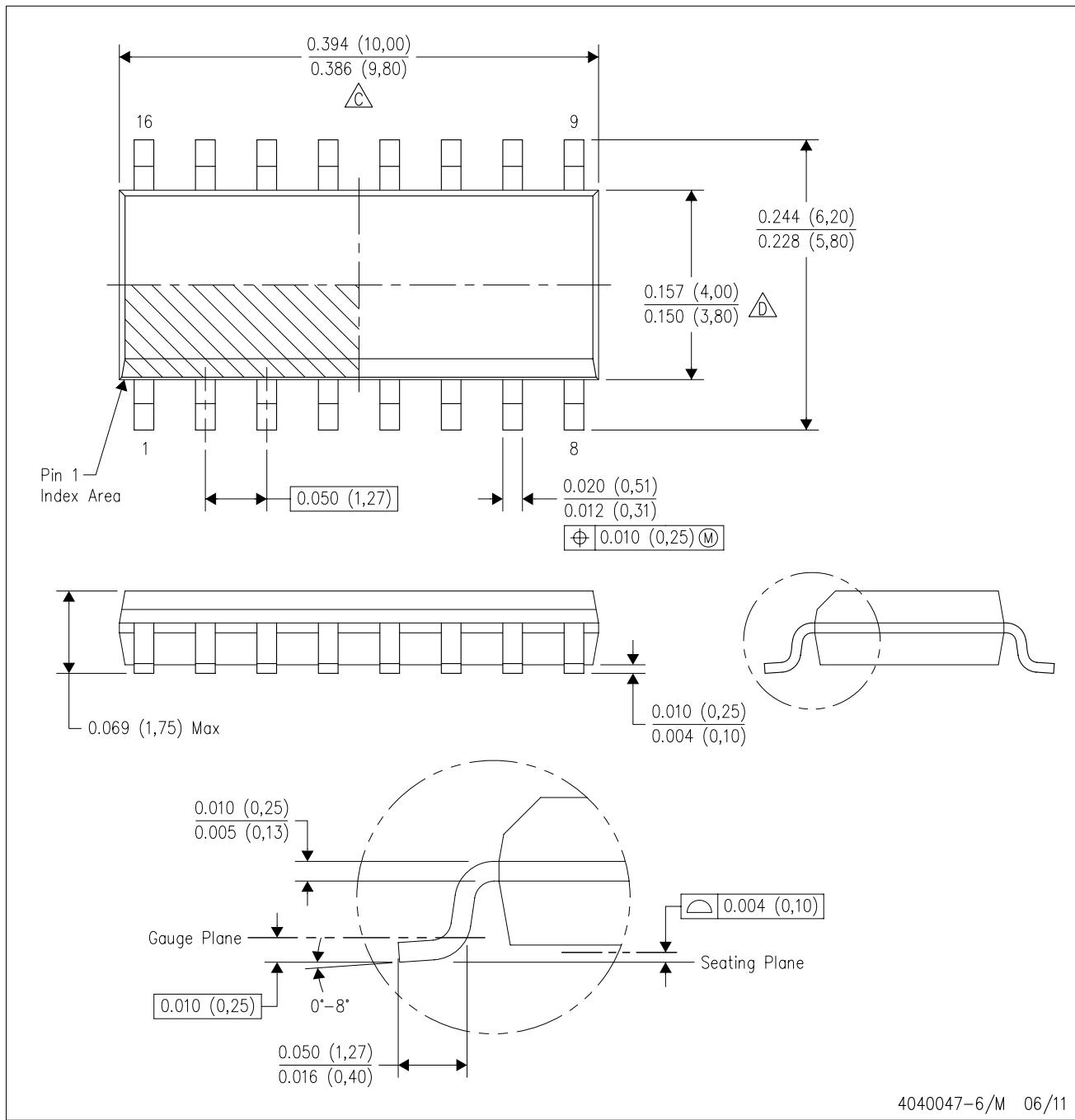
4211283-3/E 08/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

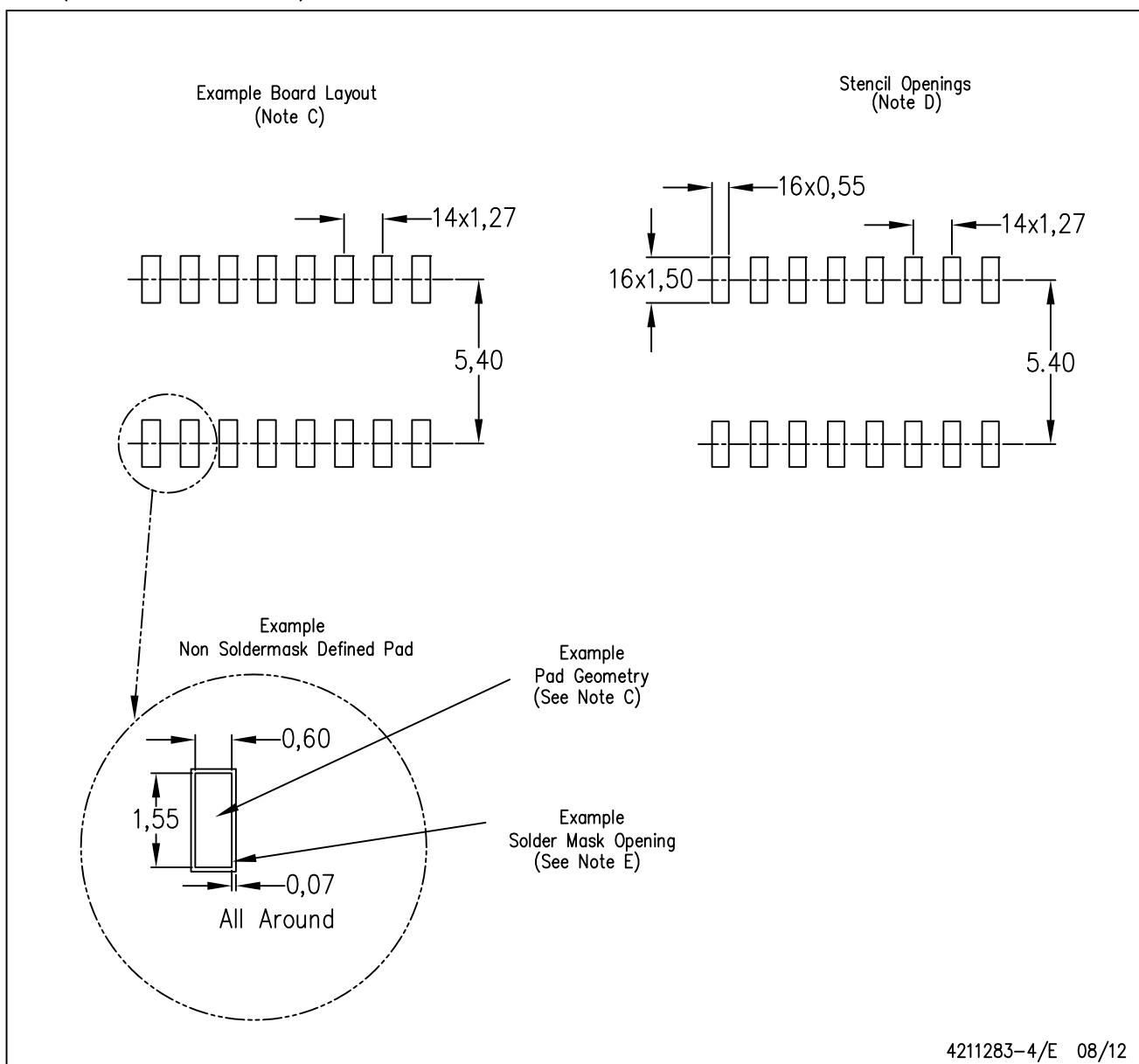
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



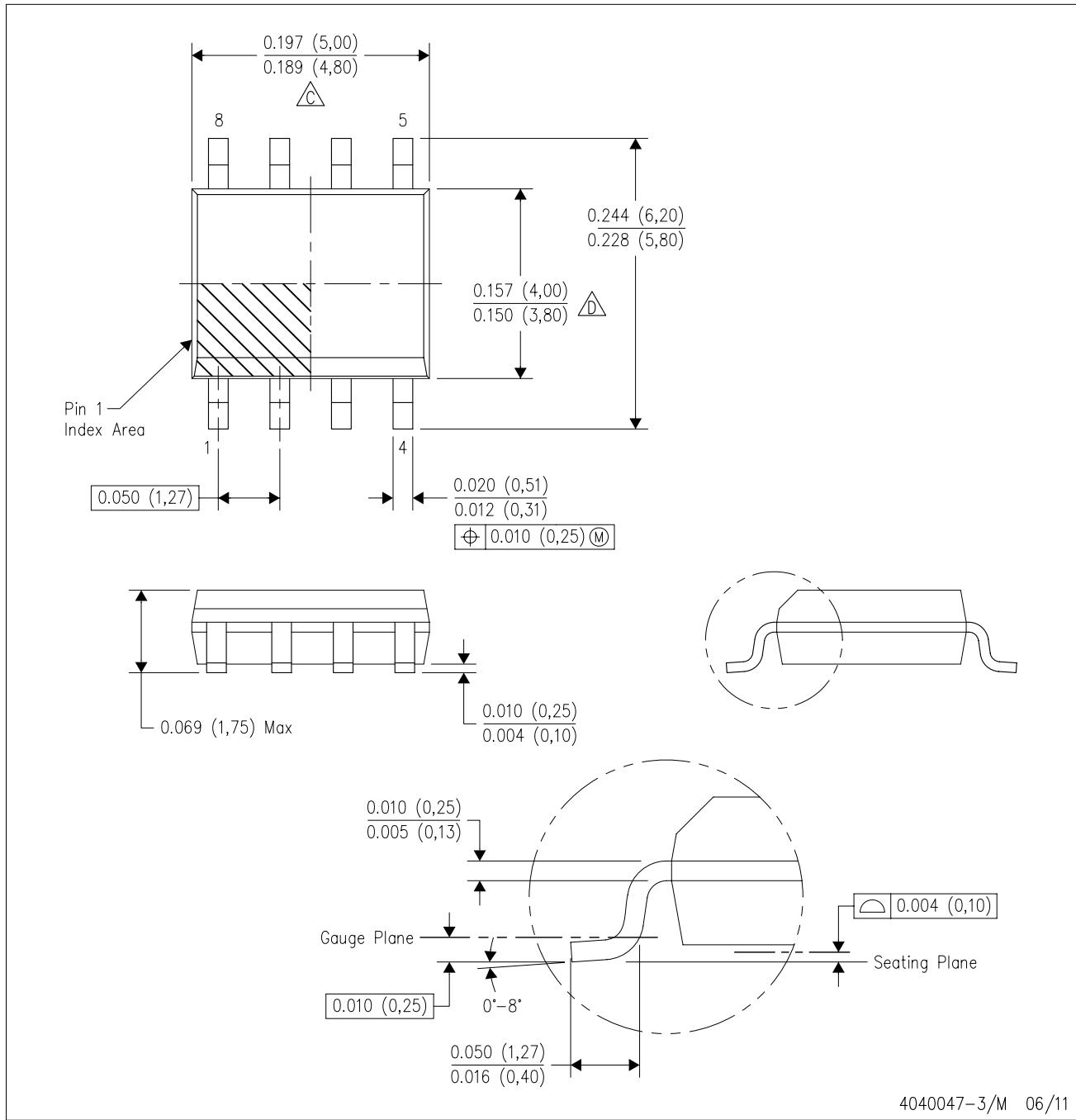
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

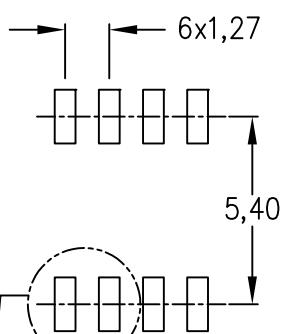
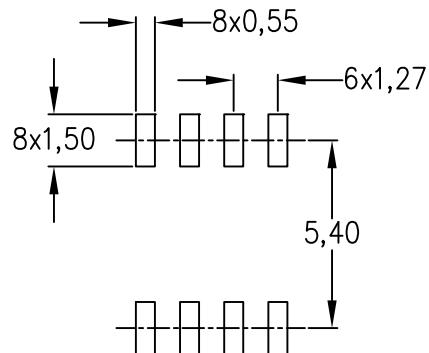
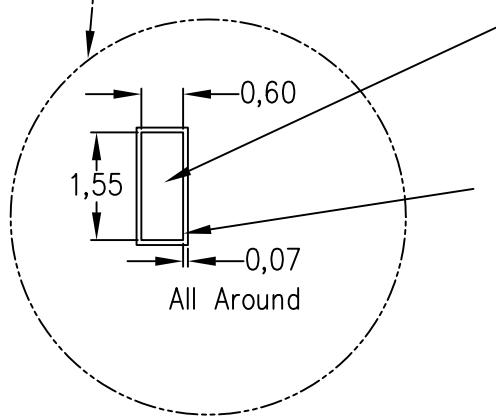
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-2/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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