Altera Product Catalog

Version 15.0

ALTERA®
MEASURABLE ADVANTAGE™

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Altera Solutions Portfolio

Altera delivers the broadest portfolio of programmable logic devices—FPGAs, SoCs, and CPLDs—together with software tools, intellectual property (IP), embedded processors, customer support, and technical training. Altera's product leadership, excellent value, and superior quality of service give you a measurable advantage. Bring your great ideas to life faster, better, and more cost effectively.

FPGAs and CPLDs

Altera FPGAs and CPLDs give you the flexibility to innovate, differentiate, and stay ahead in the market. We have four classes of FPGAs to meet your market needs, from the industry's highest density and performance to the most cost effective.

High-End FPGAs

- Highest bandwidth, highest density
- Integrated transceiver variants
- Design entire systems on a chip

Midrange FPGAs

- Balanced cost, power, and performance
- Integrated transceiver and processor variants
- Comprehensive design protection

Lowest Cost and Power FPGAs

- Lowest system cost and power
- Integrated transceiver and processor variants
- Fastest time to market

Non-Volatile FPGAs and Low-Cost CPLDs

- Instant-on, non-volatile solution
- Single-chip, dual-configuration non-volatile FPGA
- Low-cost, low-power CPLDs

SoCs

SoCs bring high integration and advanced system, power, and security management capabilities to your platform. Altera SoCs are supported by industry-standard ARM® tools and a broad ecosystem of operating systems and development tools.

High-End SoCs

- 64 bit quad-core ARM Cortex®-A53 processor
- Performance/power efficiency
- Virtualization support

Midrange SoCs

- 32 bit dual-core ARM Cortex-A9 processor
- 1.5 GHz maximum CPU frequency
- Hardened floating-point digital signal processing (DSP)
- ARM Development Studio 5 (DS-5™) Altera Edition tools

Lowest Cost and Power SoCs

- 32 bit dual-core ARM Cortex-A9 processor
- 925 MHz maximum CPU frequency
- Broad ecosystem support
- ARM DS-5 Altera Edition tools

Power Solutions

Power your FPGA with Enpirion power management products. Our integrated products provide an industry-leading combination of small footprint, low noise performance, and high efficiency to complete your design faster.

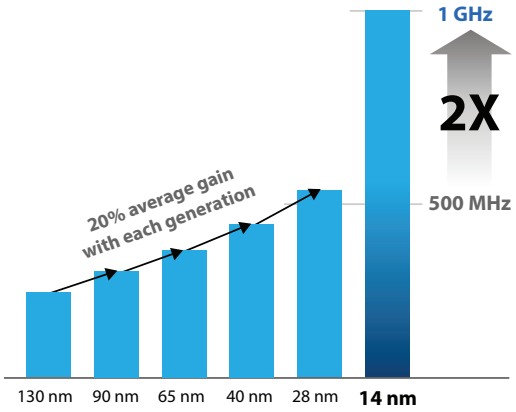
Productivity-Enhancing Design Software, Embedded Processing, IP, Development Kits, and Training

With Altera, you get a complete design environment and a wide choice of design tools—all built to work together so your designs are up and running fast. You can try one of our training classes to get a jump-start on your designs. Choose Altera and see how we enhance your productivity and make a difference to your bottom line.

Generation 10 FPGAs and SoCs

Altera's Generation 10 FPGAs and SoCs optimize process technology and architecture to deliver the industry's highest performance and highest levels of system integration at the lowest power. Generation 10 families include Stratix 10, Arria 10, and MAX 10 FPGAs.

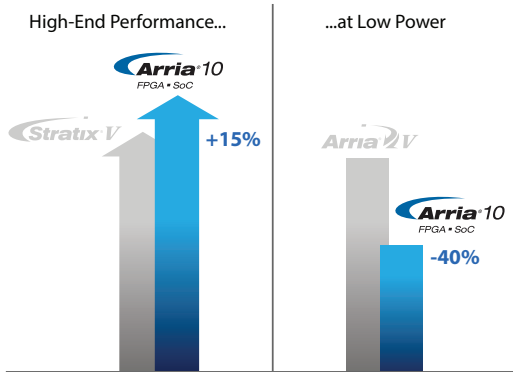
Stratix 10 FPGA • SoC



Description

- 2X core performance with revolutionary HyperFlex™ architecture
- Up to 70% power savings
- Highest density FPGA with up to 5.5 M logic elements (LEs)
- 64 bit quad-core ARM Cortex-A53 processor system
- Up to 10 tera floating point operations per second (TFLOPS) single-precision floating-point throughput
- Built on Intel's 14 nm Tri-Gate process technology

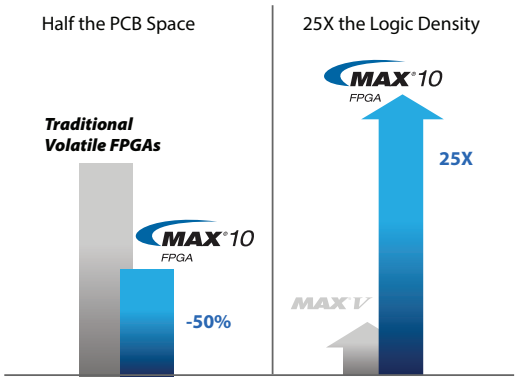
Arria 10 FPGA • SoC



Description

- 15% higher performance than current high-end devices
- 40% lower midrange power
- 1.5 GHz dual-core ARM Cortex-A9 processor
- Best-in-class IP core support, including 100G Ethernet, 100G Interlaken, and PCI Express® (PCIe®) Gen3
- Built on TSMC's 20 nm process technology

MAX 10 FPGA



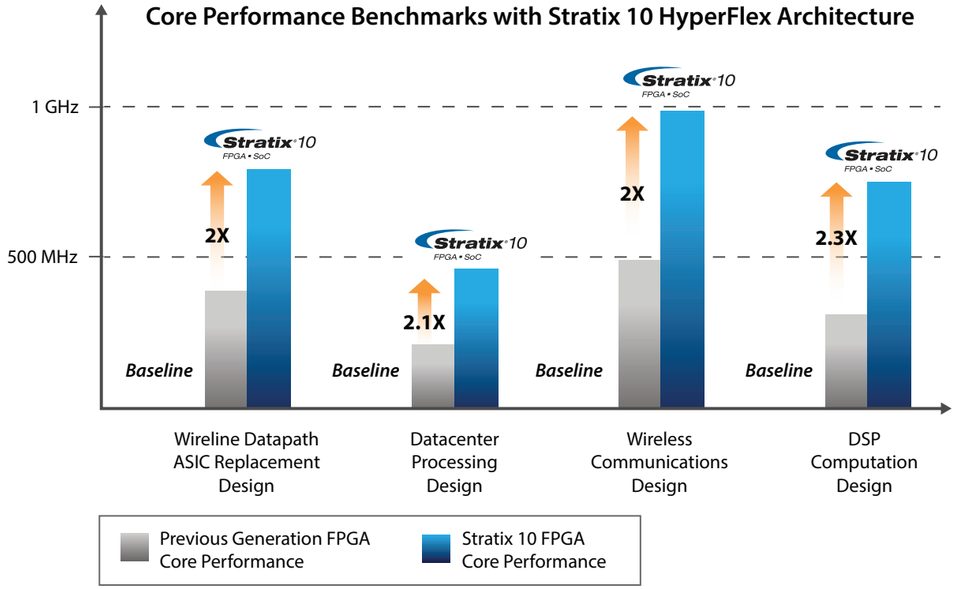
Description

- Single-chip, dual-configuration non-volatile FPGA
- Optimal system component integration for half the PCB space of traditional volatile FPGAs
- Broad range of IP including analog-to-digital converters (ADCs), DSP, and the Nios II embedded processor

Stratix 10 FPGA and SoC Overview

Stratix 10 FPGAs and SoCs deliver breakthrough advantages in performance, power efficiency, density, and system integration, unmatched in the industry. Featuring the revolutionary HyperFlex core fabric architecture and built on the Intel 14 nm Tri-Gate process, Stratix 10 devices deliver 2X core performance gains over previous-generation, high-performance FPGAs with up to 70% lower power.

HyperFlex™ ARCHITECTURE



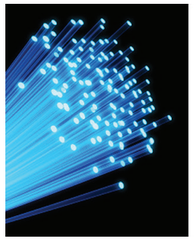
The figure above shows the core performance benchmarks achieved by early access customers using the Stratix 10 HyperFlex architecture. With the 2X performance increase, customers in multiple end markets can achieve a significant improvement in throughput and reduce area utilization, with up to 70% lower power.

Stratix 10 FPGA and SoC system integration breakthroughs include:

- Heterogeneous 3D System-in-Package (SiP) integration
- The highest density FPGA fabric with up to 5.5 million LEs
- Up to 10 TFLOPS of IEEE 754 compliant single-precision floating-point DSP throughput
- Secure Device Manager (SDM) with the most comprehensive security capabilities
- Integrated quad-core 64 bit ARM Cortex-A53 hard processor system up to 1.5 GHz
- Complementary optimized and validated Enpirion power solutions

These unprecedented capabilities make Stratix 10 devices uniquely positioned to address the design challenges in next-generation, high-performance systems in virtually all end markets including wireline and wireless communications, computing, storage, military, broadcast, medical, and test and measurement.

Communications



- 400G/500G/1T optical transmission
- 200G/400G bridging and aggregation
- 982 MHz remote radio head
- Mobile backhaul
- 5G wireless communications

Computing and Storage



- Data center server acceleration
- High-performance computing (HPC)
- Oil and gas exploration
- Bioscience

Defense



- Next-generation radar
- Secure communications
- Avionics and guidance systems

Broadcast



- High-end broadcast studio
- High-end broadcast distribution
- Headend encoder or EdgeQAM or converged multiservice access platform (CMAP)

DEVICES: GENERATION 10 DEVICE PORTFOLIO

Stratix 10 FPGA and SoC Features

www.altera.com/devices

The following features, packages, and I/O matrices give you an overview of our devices. For more details about these devices or previous generation devices, please visit www.altera.com/devices.

View device ordering codes on **page 40**

	Product Line	Stratix 10 FPGAs and SoCs									
		GX 500 SX 500	GX 650 SX 650	GX 850 SX 850	GX 1100 SX 1100	GX 1650 SX 1650	GX 2100 SX 2100	GX 2500 SX 2500	GX 2800 SX 2800	GX 4500 SX 4500	GX 5500 SX 5500
Resources	LEs[1]	484,000	646,000	841,000	1,092,000	1,624,000	2,005,000	2,422,000	2,753,000	4,463,000	5,510,000
	Adaptive logic modules (ALMs)	164,160	218,880	284,960	370,080	550,540	679,680	821,150	933,120	1,512,820	1,867,680
	ALM registers	656,640	875,520	1,139,840	1,480,320	2,202,160	2,718,720	3,284,600	3,732,480	6,051,280	7,470,720
	Hyper-Registers from HyperFlex architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric									
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees									
	M20K memory blocks	2,196	2,583	3,477	4,401	5,851	6,501	9,963	11,721	7,033	7,033
	M20K memory size (Mb)	43	50	68	86	114	127	195	229	137	137
	MLAB memory size (Mb)	3	3	4	6	8	11	13	15	23	29
	Variable-precision DSP blocks	1,152	1,440	2,016	2,520	3,145	3,744	5,011	5,760	1,980	1,980
	18 x 19 multipliers	2,304	2,880	4,032	5,040	6,290	7,488	10,022	11,520	3,960	3,960
	Peak fixed-point performance (TMACS)[2]	4.6	5.8	8.1	10.1	12.6	15.0	20.0	23.0	7.9	7.9
	Peak floating-point performance (TFLOPS)[3]	1.8	2.3	3.2	4.0	5.0	6.0	8.0	9.2	3.2	3.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection									
	Hard processor system[4]	Quad-core 64 bit ARM Cortex-A53 cache coherency unit, up to 1.5 GHz with 32 KB I/D cache, NEON™ coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general-purpose timers x7, watchdog timer x4									
	Maximum user I/O pins	488	488	736	736	704	704	1160	1160	1640	1640
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	240	240	360	360	336	336	576	576	816	816
	Total full duplex transceiver count	24	24	48	48	96	96	144	144	72	72
	GXT full duplex transceiver count (up to 30 Gbps)	16	16	32	32	64	64	96	96	48	48
	GX full duplex transceiver count (up to 17.4 Gbps)	8	8	16	16	32	32	48	48	24	24
	PCIe hard intellectual property (IP) blocks (Gen3 x16)	1	1	2	2	4	4	6	6	3	3
	Memory devices supported	DDR4, DDR3, LPDDR3, RLDRAM 3, QDR IV, QDR II+, QDR II+ Extreme, QDR II, HMC, MoSys									
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[5, 6]											
F1152 pin (35 mm x 35 mm, 1.0 mm pitch)		344,8,172,24	344,8,172,24	–	–	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		488,8,240,24	488,8,240,24	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	736,16,360,48	736,16,360,48	–	–	–	–	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	–	–	648,24,312,72	648,24,312,72	648,24,312,72	648,24,312,72	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	–	–	464,32,216,96	464,32,216,96	–	–	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	648,24,312,72	648,24,312,72
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	–	–	–	–	1160,8,576,16	1160,8,576,16	1256,8,624,16	1256,8,624,16
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96	–	–
F2597 pin (52.5 mm x 52.5 mm, 1.0 mm pitch)		–	–	–	–	–	–	432,48,216,144	432,48,216,144	–	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	1640,8,816,16	1640,8,816,16

Notes:
1. LE counts valid in comparing across Altera devices, and are conservative vs. competing FPGAs.
2. Fixed-point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE 754 compliant single precision.
4. Quad-core ARM Cortex-A53 hard processor system only available in Stratix 10 SX SoCs.
5. A subset of pins for each package are used for high-voltage, 3.0 V and 2.5 V interfaces.
6. Select devices available with pin migration from Arria 10 device family to Stratix 10 device family. Contact Altera for more information.
7. All data is preliminary, and may be subject to change without prior notice.

344,8,172,24 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.
Indicates pin migration path.

Stratix 10 SoC Hard Processor System

	Hard Processor System (HPS)
Processor	Quad-core 64 bit ARM Cortex-A53 MPCore™ processor
Maximum processor frequency	1.5 GHz[1]
Processor cache and co-processors	L1 instruction cache (32 KB) L1 data cache (32 KB) with error correction code (ECC) Level 2 cache (1 MB) with ECC Floating-point unit (FPU) single and double precision ARM NEON™ media engine ARM CoreSight™ debug and trace technology System Memory Management Unit (SMMU) Cache Coherency Unit (CCU)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4, DDR3, and LP DDR3 (Up to 64 bit with ECC)
DMA controller	8 channels
EMAC	3X 10/100/1000 EMAC with integrated DMA
USB on-the-go (OTG) controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
Serial peripheral interface (SPI) controller	4X SPI
I^2C controller	5X I^2C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	1X ONFI 1.0 or later 8 and 16 bit support
General-purpose timers	7X
HPS DDR Shared I/O	3X 48 - May be assigned to HPS for HPS DDR access
Direct I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitsream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side channel attack protection

Notes:
1. With overdrive feature.

Arria 10 FPGA and SoC Overview

Arria 10 FPGAs and SoCs deliver the highest performance at 20 nm offering a one speed-grade performance advantage over competing devices. Arria 10 FPGAs and SoCs are up to 40% lower power than previous generation FPGAs and SoCs, and feature the industry's only hard floating-point DSP blocks with speeds up to 1,500 giga floating-point operations per second (GFLOPs). The Arria 10 FPGAs and SoCs are ideal for the following end market applications:

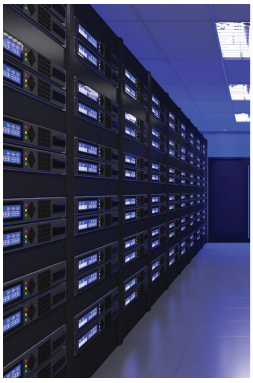
Wireless



Applications

- Remote radio head
- Mobile backhaul
- Active antenna
- Base station
- 4G/Long Term Evolution (LTE) macro eNB
- Wideband Code Division Multiple Access (W-CDMA)

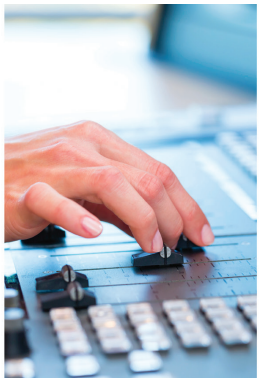
Cloud Service and Storage



Applications

- Flash cache
- Cloud
- Server
- Financial
- Bioscience
- Oil and gas

Broadcast


Applications

- Switcher
- Server
- Encoder/decoder
- Capture cards
- Editing
- Monitors
- Multiviewers

DEVICES: GENERATION 10 DEVICE PORTFOLIO

Arria 10 FPGA Features

www.altera.com/devices

The following features, packages, and I/O matrices give you an overview of our devices. For more details about these devices or previous generation devices, please visit www.altera.com/devices.

View device ordering codes on **page 40**.

	Product Line	Arria 10 GX FPGAs[1]									Arria 10 GT FPGAs[1]	
		GX 160	GX 220	GX 270	GX 320	GX 480	GX 570	GX 660	GX 900	GX 1150	GT 900	GT 1150
Resources	Part number reference	10AX016	10AX022	10AX027	10AX032	10AX048	10AX057	10AX066	10AX090	10AX115	10AT090	10AT115
	LEs (K)	160	220	270	320	480	570	660	900	1,150	900	1,150
	Adaptive logic modules (ALMs)	61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200	339,620	427,700
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800	1,358,480	1,708,800
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133	2,423	2,713	2,423	2,713
	M20K memory (Mb)	9	11	15	17	28	35	42	47	53	47	53
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7	9.2	12.7	9.2	12.7
	Hardened single-precision floating-point multipliers/adders	156/156	191/191	830/830	985/985	1,368/1,368	1,523/1,523	1,688/1,688	1,518/1,518	1,518/1,518	1,518/1,518	1,518/1,518
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,376	3,036	3,036	3,036	3,036
	Peak GMACS	343	420	1,826	2,167	3,010	3,351	3,714	3,340	3,340	3,340	3,340
	GFLOPS	140	172	747	887	1,231	1,371	1,519	1,366	1,366	1,366	1,366
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	32	32	32	32	32	32	32	32	32	32	32
	Regional clocks	8	8	8	8	8	8	16	16	16	16	16
	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0[2]										
	I/O standards supported	**3 V I/O pins only:** 3 V LVTTL, 2.5 V CMOS **DDR and LVDS I/O pins:** POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL **All I/Os:** 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-135, SSTL-125, SSTL-18 (1 and II), SSTL-15 (I and II), Differential SSTL-12, SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-135, Differential SSTL-125, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12									
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	270	270	384	384	312	312
	Maximum user I/O pins	288	288	384	384	492	624	624	768	768	624	624
	Transceiver count (17.4 Gbps)	12	12	24	24	36	48	48	96	96	96	96
	Transceiver count (28.3 Gbps)	–	–	–	–	–	–	–	–	–	16	16
	PCIe hard IP blocks (Gen3)	1	1	2	2	2	2	2	4	4	4	4
	Maximum 3 V I/O pins	48	48	48	48	48	48	48	–	–	–	–
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II, HMC										
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count												
U19	U484 pin (19 mm)	192, 48, 72, 6	192, 48, 72,6	–	–	–	–	–	–	–	–	–
F27	F672 pin (27 mm)	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	–	–	–	–	–	–	–
F29	F780 pin (29 mm)	288, 48, 120, 12	288, 48, 120, 12	360, 48, 156, 12	360, 48, 156, 12	360, 48, 156, 12	–	–	–	–	–	–
F34	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	492, 48, 222, 24	492, 48, 222, 24	492, 48, 222, 24	504, 0, 252, 24	504, 0, 252, 24	–	–
F35	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	396, 48, 174, 36	396, 48, 174, 36	396, 48, 174, 36	–	–	–	–
KF40	F1517 pin (40 mm)	–	–	–	–	–	696, 96, 324, 36	696, 96, 324, 36	–	–	–	–
NF40	F1517 pin (40 mm)	–	–	–	–	–	588, 48, 270, 48	588, 48, 270, 48	600, 0, 300, 48	600, 0, 300, 48	600, 0, 300, 48	600, 0, 300, 48
RF40	F1517 pin (40 mm)	–	–	–	–	–	–	–	342, 0, 154, 66	342, 0, 154, 66	–	–
NF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	768, 0, 384, 48	768, 0, 384, 48	–	–
SF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	624, 0, 312, 72	624, 0, 312, 72	624, 0, 312, 72	624, 0, 312, 72
UF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	480, 0, 240, 96	480, 0, 240, 96	480, 0, 240, 96	480, 0, 240, 96

Notes:

1. 216, 48, 72, 6 — Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.
2. — Indicates pin migration.
3. All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
4. A subset of pins for each package are used for 3.3 V and 2.5 V interfaces.
5. Each LVDS pair can be configured as either a differential input or a differential output.
6. F36 Package does not have SX variant.
7. Certain packages might not bond out all PCIe hard IP blocks.
8. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

DEVICES: GENERATION 10 DEVICE PORTFOLIO

Arria 10 SoC Features

20 nm Arria 10 SoCs deliver all the features and benefits of Arria 10 FPGAs plus a second-generation hard processor system with 87% higher processor performance (1.5 GHz dual-core ARM Cortex-A9 MPCore™ processor). Additionally, they include enhancements such as Secure Boot, three Ethernet media access controller (EMAC) hard IP cores, and 64 bit DDR4 SDRAM support—all while maintaining full software compatibility with 28 nm SoCs.

View device ordering codes on **page 41**.

	Product Line	SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Resources	Part number reference	10AS016	10AS022	10AS027	10AS032	10AS048	10AS057	10AS066
	LEs (K)	160	220	270	320	480	570	660
	ALMs	61,510	83,730	101,620	118,730	181,790	217,080	250,540
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133
	M20K memory (Mb)	9	11	15	17	28	35	42
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7
	Hardened single-precision floating-point multiplers /adders	156/156	191/191	830/830	985/985	1,368/1,368	1,523/1,523	1,688/1,688
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,376
	Peak GMACS	343	420	1,826	2,167	3,010	3,351	3,714
	GFLOPS	140	172	747	887	1,231	1,371	1,519
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	32	32	32	32	32	32	32
	Regional clocks	8	8	8	8	8	8	16
	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0[2]						
	I/O standards supported	**3 V I/O pins only:** 3 V LVTTL, 2.5 V CMOS **DDR and LVDS I/O pins:** POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL **All I/Os:** 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-135, SSTL-125, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-135, Differential SSTL-125, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-12, Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12						
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	270	270
	Maximum user I/O pins	288	288	384	384	492	624	624
	Transceiver count (17.4 Gbps)	12	12	24	24	36	48	48
	Transceiver count (28 Gbps)	–	–	–	–	–	–	–
	PCIe hard IP blocks (Gen3)	1	1	2	2	2	2	2
	Maximum 3 V I/O pins	48	48	48	48	48	48	48
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II, HMC						
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count								
U19	U484 pin (19 mm)	192, 48, 72, 6	192, 48, 72,6	–	–	–	–	–
F27	F672 pin (27 mm)	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	–	–	–
F29	F780 pin (29 mm)	288, 48, 120, 12	288, 48, 120, 12	360, 48, 156, 12	360, 48, 156, 12	360, 48, 156, 12	–	–
F34	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	492, 48, 222, 24	492, 48, 222, 24	492, 48, 222, 24
F35	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	396, 48, 174, 36	396, 48, 174, 36	396, 48, 174, 36
KF40	F1517 pin (40 mm)	–	–	–	–	–	696, 96, 324, 36	696, 96, 324, 36
NF40	F1517 pin (40 mm)	–	–	–	–	–	588, 48, 270, 48	588, 48, 270, 48

Notes:
1. 216, 48, 72, 6 Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.
2. Indicates pin migration.
3. All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
4. A subset of pins for each package are used for 3.3 V and 2.5 V interfaces.
5. Each LVDS pair can be configured as either a differential input or a differential output.
6. F36 package does not have SX variant.
7. Certain packages might not bond out all PCIe hard IP blocks.
8. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

	Hard Processor System (HPS)
Processor	Dual-core ARM Cortex-A9 MPCore processor
Maximum processor frequency	1.5 GHz[1]
Processor cache and co-processors	L1 instruction cache (32 KB) L1 data cache (32 KB) Level 2 cache (512 KB) shared FPU single and double precision ARM Neon media engine ARM CoreSight debug and trace technology Snoop control unit (SCU) Acceleration coherency port (ACP)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4, DDR3, and LP DDR3 (Up to 64 bit with ECC)
DMA controller	8 channels
EMAC	3X 10/100/1000 EMAC with integrated DMA
USB OTG controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
SPI controller	4X SPI
I^2C controller	5X I^2C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	1X ONFI 1.0 or later 8 and 16 bit support
General-purpose timers	7X
Software-programmable GPIOs	Maximum 54 GPIOs
Direct shared I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure boot, AES, and secure hash algorithm

Notes:
1. With overdrive feature.

MAX 10 FPGA Overview

Altera's new MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor, programmable logic device.

MAX 10 FPGAs are built on TSMC's 55 nm flash technology, enabling instant-on configuration so you can quickly control the power-up or initialization of other components in the system. The devices also include full-featured FPGA capabilities, such as DSP, analog functionality, Nios II Gen2 embedded processor support, and memory controllers.

With a robust set of FPGA capabilities, MAX 10 FPGAs are optimized for a wide range of high-volume, cost-sensitive applications, including:

Automotive

- Built on TSMC's 55 nm high-volume flash process tailored for the automotive industry's rigorous safety and quality requirements
- Integrated flash provides instant-on behavior for applications requiring fast boot times such as rear-view cameras in advanced driver assistance systems (ADAS) and infotainment displays
- FPGA-class signal processing acceleration for electric vehicle (EV) applications, such as motor control, battery management, and power conversion

Industrial

- Reduced footprint, increased design security and reliability, and lower system cost
- Accurate environmental condition sensing and efficient real-time controls for motor control, I/O modules, and Internet of Things (IoT) applications
- Single-chip support for multiple industrial Ethernet protocols and machine-to-machine (M2M) communication

Communications

- Analog functionality for sensing board environment allows integration of power-up sequencing and system-monitoring circuitry in a single device
- High I/O count and software-based system management using the Nios II soft processor enable board management integration in an advanced, reliable, single-chip system controller

MAX 10 FPGA Features

View device ordering codes on **page 41**.

Product Line		10M02	10M04	10M08	10M16	10M25	10M40	10M50
LEs (K)		2	4	8	16	25	40	50
Block memory (Kb)		108	189	378	549	675	1,260	1,638
User flash memory[1] (KB)		12	16 – 156	32 – 172	32 – 296	32 – 400	64 – 736	64 – 736
18 x 18 multipliers		16	20	24	45	55	125	144
PLLs[2]		1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
Internal configuration		Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD)[3]		-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
External memory interface (EMIF)		Yes[6]	Yes[6]	Yes[6]	Yes[7]	Yes[7]	Yes[7]	Yes[7]
Package Options and I/O Pins: Feature Set Options, GPIO, True LVDS Transceiver/Receiver								
V36 (D)[8]	WLCSP (3 mm, 0.4 mm pitch)	C, 27, 3/7	–	–	–	–	–	–
V81 (D)	WLCSP (4 mm, 0.4 mm pitch)	–	–	C/F, 56, 7/17	–	–	–	–
F256 (D)	FBGA (17 mm, 1.0 mm pitch)	–	C/F/A, 178, 13/54	C/F/A, 178, 13/54	C/F/A, 178, 13/54	C/F/A, 178, 13/54	C/F/A, 178, 13/54	C/F/A, 178, 13/54
U324 (D)	UBGA (15 mm, 0.8 mm pitch)	C, 160, 9/47	C/F/A, 246, 15/81	C/F/A, 246, 15/81	C/F/A, 246, 15/81	–	–	–
F484 (D)	FBGA (23 mm, 1.0 mm pitch)	–	–	C/F/A, 250, 15/83	C/F/A, 320, 22/116	C/F/A, 360, 24/136	C/F/A, 360, 24/136	C/F/A, 360, 24/136
F672 (D)	FBGA (27 mm, 1.0 mm pitch)	–	–	–	–	–	C/F/A, 500, 30/192	C/F/A, 500, 30/192
E144 (S)[8]	EQFP (22 mm, 0.5 mm pitch)	C, 101, 7/27	C/F/A, 101, 10/27	C/F/A, 101, 10/27	C/F/A, 101, 10/27	C/F/A, 101, 10/27	C/F/A, 101, 10/28	C/F/A, 101, 10/28
M153 (S)	MBGA (8 mm, 0.5 mm pitch)[9]	C, 112, 9/29	C/F/A, 112, 9/29	C/F/A, 112, 9/29	–	–	–	–
U169 (S)	UBGA (11 mm, 0.8 mm pitch)	C, 130, 9/38	C/F/A, 130, 9/38	C/F/A, 130, 9/38	C/F/A, 130, 9/38	–	–	–

Notes:

1. Additional user flash may be available, depending on configuration options.
2. The number of PLLs available is dependent on the package option.
3. Availability of the ADC or TSD varies by package type. Smaller pin-count packages do not have access to the ADC hard IP.
4. C, 27, 3/7 Indicates feature set options, GPIO count, and LVDS transceiver or receiver count. Feature set options: C = Compact (single image), F = Flash (dual image with RSU), A = Analog (analog features block). Each has added premiums.
5. ▪——▪ Indicates pin migration.
6. SRAM only.
7. SRAM, DDR3 SDRAM, DDR2 SDRAM, or LPDDR2.
8. "D" = Dual power supply (1.2 V/2.5 V), "S" = Single power supply (3.3 V or 3.0 V).
9. "Easy PCB" utilizes 0.8 mm PCB design rules.
10. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

DEVICES: 28 nm DEVICE PORTFOLIO

Stratix V FPGA Features

View device ordering codes on **page 42**.

	Product Line	Stratix V GS FPGAs[1]					Stratix V GX FPGAs[1]										Stratix V GT FPGAs[1]		Stratix V E FPGAs[1]	
		5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8	5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6	5SGXB9	5SGXBB	5SGTC5	5SGTC7	5SEE9	5SEEB
Resources	LEs (K)	236	360	457	583	695	340	420	490	622	840	952	490	597	840	952	425	622	840	952
	ALMs	89,000	135,840	172,600	220,000	262,400	128,300	158,500	185,000	234,720	317,000	359,200	185,000	225,400	317,000	359,200	160,400	234,720	317,000	359,200
	Registers	356,000	543,360	690,400	880,000	1,049,600	513,200	634,000	740,000	938,880	1,268,000	1,436,800	740,000	901,600	1,268,000	1,436,800	641,600	938,880	1,268,000	1,436,800
	M20K memory blocks	688	957	2,014	2,320	2,567	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660	2,640	2,640	2,304	2,560	2,640	2,640
	M20K memory (Mb)	13	19	39	45	50	19	37	45	50	52	52	41	52	52	52	45	50	52	52
	MLAB memory (Mb)	2.72	4.15	5.27	6.71	8.01	3.92	4.84	5.65	7.16	9.67	10.96	5.65	6.88	9.67	10.96	4.9	7.16	9.67	10.96
	Variable-precision DSP blocks	600	1,044	1,590	1,775	1,963	256	256	256	256	352	352	399	399	352	352	256	256	352	352
	18 x 18 multipliers	1,200	2,088	3,180	3,550	3,926	512	512	512	512	704	704	798	798	704	704	512	512	704	704
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
	Regional clocks	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]																		
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12																		
	LVDS channels, 1.4 Gbps (receive/transmit)	108	174	174	210	210	174	174	210	210	210	210	150	150	150	150	150	150	210	210
	Transceiver count (14.1 Gbps)	24	36	36	48	48	36	36	48	48	48	48	66	66	66	66	32	32	—	—
	Transceiver count (28.05 Gbps)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	4	4	—	—
	PCIe hard IP blocks (Gen3)	1	1	1	4	4	2	2	4	4	4	4	4	4	4	4	1	1	—	—
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3																		
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count																				
F780 pin (29 mm, 1.0 mm pitch)		360, 90, 12[3]	360, 90, 12[3]	–	–	–	360, 90, 12[3]	–	–	–	–	–	–	–	–	–	–	–	–	–
F1152 pin (35 mm, 1.0 mm pitch)		432, 108, 24	432, 108, 24	552, 138, 24	–	–	432, 108, 24	552, 138, 24	552, 138, 24	552, 138, 24	–	–	–	–	–	–	–	–	–	–
F1152 pin (35 mm, 1.0 mm pitch)		–	–	–	–	–	432, 108, 36	432, 108, 36	432, 108, 36	432, 108, 36	–	–	–	–	–	–	–	–	–	–
F1517 pin (40 mm, 1.0 mm pitch)		–	696, 174, 36	696, 174, 36	696, 174 ,36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36[4]	696, 174, 36[4]	432, 108, 66	432, 108, 66	–	–	–	–	696, 174, 0[4]	696, 174, 0[4]
F1517 pin (40 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	600,150,48	600,150,48	–	–	–	–	–	–	600, 150, 36[5]	600, 150 ,36[5]	–	–
F1760 pin (42.5 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	–	–	–	600, 150, 66	600, 150, 66	600, 150, 66[4]	600, 150, 66[4]	–	–	–	–
F1932 pin (45 mm, 1.0 mm pitch)		–	–	–	840,210,48	840,210,48	–	–	840, 210, 48	840, 210, 48	840, 210, 48	840, 210, 48	–	–	–	–	–	–	840, 210, 0	840, 210, 0

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.
2. 3.3 V compliant, requires a 3.0 V power supply.
3. Hybrid package (flip chip) FBGA: 33 x 33 (mm) 1.0-mm pitch.
4. Hybrid package (flip chip) FBGA: 45 x 45 (mm) 1.0-mm pitch.
5. GX–GT migration. Unused transceiver channels connected to power/ground.
6. 360, 90, 12 Numbers indicate GPIO count, LVDS count, and transceiver count.
7. Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.
8. Stratix series devices are offered for commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered for industrial temperatures (0 °C to 100 °C).

DEVICES: 28 nm DEVICE PORTFOLIO

Arria V FPGA and SoC Features

View device ordering codes on **page 42**.

	Product Line	Arria V GX FPGAs[1]								Arria V GT FPGAs[1]				Arria V GZ FPGAs[1]				Arria V SX SoCs[1]		Arria V ST SoCs[1]	
		5AGXA1	5AGXA3	5AGXA5	5AGXA7	5AGXB1	5AGXB3	5AGXB5	5AGXB7	5AGTC3	5AGTC7	5AGTD3	5AGTD7	5AGZE1	5AGZE3	5AGZE5	5AGZE7	5ASXB3	5ASXB5	5ASTD3	5ASTD5
Resources	LEs (K)	75	156	190	242	300	362	420	504	156	242	362	504	220	360	400	450	350	462	350	462
	ALMs	28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240	58,900	91,680	136,880	190,240	83,020	135,840	150,960	169,800	132,075	174,340	132,075	174,340
	Registers	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960	235,600	366,720	547,520	760,960	332,080	543,360	603,840	679,200	528,300	697,360	528,300	697,360
	M10K memory blocks	800	1,051	1,180	1,366	1,510	1,726	2,054	2,414	1,051	1,366	1,726	2,414	–	–	–	–	1,729	2,282	1,729	2,282
	M20K memory blocks	–	–	–	–	–	–	–	–	–	–	–	–	585	957	1,440	1,700	–	–	–	–
	M10K memory (Kb)	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140	10,510	13,660	17,260	24,140	–	–	–	–	17,290	22,820	17,290	22,820
	M20K memory (Kb)	–	–	–	–	–	–	–	–	–	–	–	–	11,700	19,140	28,800	34,000	–	–	–	–
	MLAB memory (Kb)	463	961	1,173	1,448	1,852	2,098	2,532	2,906	961	1,448	2,098	2,906	2,594	4,245	4,718	5,306	2,014	2,658	2,014	2,658
	Variable-precision DSP blocks	240	396	600	800	920	1,045	1,092	1,156	396	800	1,045	1,156	800	1,044	1,092	1,139	809	1,090	809	1,090
	18 x 18 multipliers	480	792	1,200	1,600	1,840	2,090	2,184	2,312	792	1,600	2,090	2,312	1,600	2,088	2,184	2,278	1,618	2,180	1,618	2,180
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (ARM Cortex-A9)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (GHz)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1.05[2]	1.05[2]	1.05[2]	1.05[2]
	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[3] (FPGA)	10	10	12	12	12	12	16	16	10	12	12	16	20	20	24	24	14	14	14	14
	PLLs (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	3	3	3
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[4]																			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12																			
	LVDS channels (receiver/transmitter)	80/67	80/67	136/120	136/120	176,160	176,160	176,160	176,160	80/70	136/120	176/160	176/160	108/99	108/99	168/166	168/166	120/136	120/136	120/136	120/136
	Transceiver count (6.5536 Gbps)	9	9	24	24	24	24	36	36	3	6	6	6	–	–	–	–	30	30	30	30
	Transceiver count (10.3125 Gbps)[5]	–	–	–	–	–	–	–	–	4	12	12	20	–	–	–	–	–	–	16	16
	Transceiver count (12.5 Gbps)	–	–	–	–	–	–	–	–	–	–	–	–	24	24	36	36	–	–	–	–
	PCIe hard IP blocks (Gen2 x4)	1	1	2	2	2	2	2	2	1	2	2	2	–	–	–	–	2	2	2	2
	PCIe hard IP blocks (Gen2 x8, Gen3)	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1	–	–	–	–
	GPIOs (FPGA)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	540	540	540	540
	GPIOs (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	208	208	208	208
	Hard memory controllers[6] (FPGA)	2	2	4	4	4	4	4	4	2	4	4	4	–	–	–	–	3	3	3	3
	Hard memory controllers (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1
	Memory devices supported	DDR3, DDR2, DDR II+[7], QDR II, QDR II+, RLDRAM II, RLDRAM 3[8], LPDDR[7], LPDDR2[7]																			
Package Options and I/O Pins: GPIO Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count																					
F672 pin (27 mm, 1.0 mm pitch)		336 9,0	336 9,0	336 9,0	336 9,0	–	–	–	–	336 3,4	–	–	–	–	–	–	–	–	–	–	–
H780 pin (29 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	–	–	–	–	342 12	342 12	–	–	–	–		–
F896 pin (31 mm, 1.0 mm pitch)		416 9,0	416 9,0	384 18,0	384 18,0	384 18,0	384 18,0	–	–	416 3,4	384 6,8	384 6,8	–	–	–	–	–	250, 208 12+0	250, 208 12+0	250, 208 12+6	250, 208 12+6
F896 pin (31 mm, 1.0 mm pitch)		320 9,0	320 9,0	320 9,0	320 9,0	320 9,0	–	–	–	320 3,4	320 3,4	320 3,4	–	–	–	–	–	–	–	–	–
F1152 pin (35 mm, 1.0 mm pitch)		–	–	544 24,0	544 24,0	544 24,0	544 24,0	544 24,0	544 24,0	–	544 6,12	544 6,12	544 6,12	414 24	414 24	534 24	534 24	385, 208 18+0	385, 208 18+0	385, 208 18+8	385, 208 18+8
F1517 pin (40 mm, 1.0 mm pitch)		–	–	–	–	704 24,0	704 24,0	704 36,0	704 36,0	–	–	704 6,12	704 6,20	–	–	674 36	674 36	540, 208 30+0	540, 208 30+0	540, 208 30+16	540, 208 30+16

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.
2. 1.15 V operation.
3. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
4. 3.3 V compliant, requires a 3.0 V power supply.
5. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels.
6. With 16 and 32 bit ECC support.
7. These memory interfaces are not available as Altera IP.
8. This memory interface is only available for Arria V GZ devices.

336 / 9,0 — For Arria V GX and GT devices, values on top indicate available user I/O pins and values at the bottom indicate the 6.5536 Gbps and 10.3125 Gbps transceiver count. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels. For Arria V GZ devices, values on top indicate available user I/O pins and values at the bottom indicate the 12.5 Gbps transceiver count.

250, 208 / 12+0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 6.5536 Gbps plus 10.3125 Gbps transceiver count.

Pin migration (same V_{CC}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

Pin migration is only possible if you use up to 320 I/O pins, up to nine 6.5536 Gbps transceiver count (for Arria V GX devices), and up to four 10.3125 Gbps transceiver count (for Arria V GT devices).

DEVICES: 28 nm DEVICE PORTFOLIO

Cyclone V FPGA Features

View device ordering codes on **page 43.**

	Product Line	Cyclone V E FPGAs[1]					Cyclone V GX FPGAs[1]					Cyclone V GT FPGAs[1]		
		5CEA2	5CEA4	5CEA5	5CEA7	5CEA9	5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9	5CGTD5	5CGTD7	5CGTD9
Resources	LEs (K)	25	49	77	149.5	301	35.5	50	77	149.5	301	77	149.5	301
	ALMs	9,434	18,480	29,080	56,480	113,560	13,460	18,868	29,080	56,480	113,560	29,080	56,480	113,560
	Registers	37,736	73,920	116,320	225,920	454,240	53,840	75,472	116,320	225,920	454,240	116,320	225,920	454,240
	M10K memory blocks	176	308	446	686	1,220	135	250	446	686	1,220	446	686	1,220
	M10K memory (Kb)	1,760	3,080	4,460	6,860	12,200	1,350	2,500	4,460	6,860	12,200	4,460	6,860	12,200
	MLAB memory (Kb)	196	303	424	836	1,717	291	295	424	836	1,717	424	836	1,717
	Variable-precision DSP blocks	25	66	150	156	342	57	70	150	156	342	150	156	342
	18 x 18 multipliers	50	132	300	312	684	114	140	300	312	684	300	312	684
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	4	4	6	7	8	4	6	6	7	8	6	7	8
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3												
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS												
	LVDS channels (receiver/transmitter)	56/56	56/56	60/60	120/120	120/120	52/52	84/84	84/84	120/120	140/140	84/84	120/120	140/140
	Transceiver count (3.125 Gbps)	–	–	–	–	–	3	6	6	9	12	–	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	–	–	6	9	12
	PCIe hard IP blocks (Gen1 x4)	–	–	–	–	–	1	2	2	2	2	–	–	–
	PCIe hard IP blocks (Gen2 x1, x2, and x4, Gen1 x4)	–	–	–	–	–	–	–	–	–	–	2	2	2
	Hard memory controllers[5] (FPGA)	1	1	2	2	2	1	2	2	2	2	2	2	2
	Memory devices supported	DDR3, DDR2, LPDDR2												
Package Options and I/O Pins: GPIO Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count														
M301 pin (11 mm, 0.5 mm pitch)								129 4	129 4			129 4		
M383 pin (13 mm, 0.5 mm pitch)		223	223	175				175 6	175 6			175 6		
M484 pin (15 mm, 0.5 mm pitch)					240					240 3			240 3	
U324 pin (15 mm, 0.8 mm pitch		176	176				144 3							
U484 pin (19 mm, 0.8 mm pitch)		224	224	224	240	240	208 3	224 6	224 6	240 6	240 5	224 6	240 6	240 5
F256 pin (17 mm, 1.0 mm pitch)		128	128											
F484 pin (23 mm, 1.0 mm pitch)		224	224	240	240	224	208 3	240 6	240 6	240 6	224 6	240 6	240 6	224 6
F672 pin (27 mm, 1.0 mm pitch					336	336		336 6	336 6	336 9	336 9	336 6	336 9	336 9
F896 pin (31 mm, 1.0 mm pitch					480	480				480 9	480 12		480 9	480 12
F1152 pin (35 mm, 1.0 mm pitch											560 12			560 12

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.
2. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
3. Automotive grade Cyclone V GT FPGAs include a 5 Gbps transceiver.
4. One PCIe hard IP block in U672 package.
5. Includes 16 and 32 bit error correction code ECC support.

129 / 4 — Values on top indicate available user I/O pins; values at the bottom indicate the 3.125 Gbps, 5 Gbps, or 6.144 Gbps transceiver count.

66, 151 / 0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 3.125 Gbps or 5 Gbps transceiver count.

Pin migration (same V_{CC}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

For FPGAs: Pin migration is only possible if you use only up to 175 GPIOs.

DEVICES: 28 nm DEVICE PORTFOLIO

Cyclone V SoC Features

View device ordering codes on **page 44**.

	Product Line	Cyclone V SE SoCs[1]				Cyclone V SX SoCs[1]				Cyclone V ST SoCs[1]	
		5CSEA2	5CSEA4	5CSEA5	5CSEA6	5CSXC2	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
Resources	LEs (K)	25	40	85	110	25	40	85	110	85	110
	ALMs	9,434	15,094	32,075	41,509	9,434	15,094	32,075	41,509	32,075	41,509
	Registers	37,736	60,376	128,300	166,036	37,736	60,376	128,300	166,036	128,300	166,036
	M10K memory blocks	140	270	397	557	140	270	397	557	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570	1,400	2,700	3,970	5,570	3,970	5,570
	MLAB memory (Kb)	138	231	480	621	138	231	480	621	480	621
	Variable-precision DSP blocks	36	84	87	112	36	84	87	112	87	112
	18 x 18 multipliers	72	168	174	224	72	168	174	224	174	224
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (ARM Cortex-A9)	Single or dual	Single or dual	Single or dual	Single or dual	Dual	Dual	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (MHz)	925	925	925	925	925	925	925	925	925	925
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	5	5	6	6	5	5	6	6	6	6
	PLLs (HPS)	3	3	3	3	3	3	3	3	3	3
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3									
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS									
	LVDS channels (receiver/transmitter)	37/32	37/32	72/72	72/72	37/32	37/32	72/72	72/72	72/72	72/72
	Transceiver count (3.125 Gbps)	–	–	–	–	6	6	9	9	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	9	9
	PCIe hard IP blocks (Gen1 x4)[4]	–	–	–	–	2	2	2	2	–	–
	PCIe hard IP blocks (Gen2 x1, x2, and x4, Gen1 x4)	–	–	–	–	–	–	–	–	2	2
	GPIOs (FPGA)	145	145	288	288	145	145	288	288	288	288
	GPIOs (HPS)	181	181	181	181	181	181	181	181	181	181
	Hard memory controllers[5] (FPGA)	1	1	1	1	1	1	1	1	1	1
	Hard memory controllers[5] (HPS)	1	1	1	1	1	1	1	1	1	1
	Memory devices supported	DDR3, DDR2, LPDDR2									
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count											
	U484 pin (19 mm, 0.8 mm pitch)	66, 151 0	66, 151 0	66, 151 0	66, 151 0						
	U672 pin (23 mm, 0.8 mm pitch)	145, 181 0	145, 181 0	145, 181 0	145, 181 0	145, 181 6	145, 181 6	145, 181 6	145, 181 6		
	F896 pin (31 mm, 1.0 mm pitch			288, 181 0	288, 181 0			288, 181 9	288, 181 9	288, 181 9	288, 181 9

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.
2. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
3. Automotive grade Cyclone V GT FPGAs include a 5 Gbps transceiver.
4. One PCIe hard IP block in U672 package.
5. With 16 and 32 bit ECC support.

129
4 — Values on top indicate available user I/O pins; values at the bottom indicate the 3.125 Gbps, 5 Gbps, or 6.144 Gbps transceiver count.

66, 151
0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 3.125 Gbps or 5 Gbps transceiver count.

Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

For SoCs: Pin migration is only possible if you use only up to 138 GPIOs.

Stratix IV GT FPGA Features

View device ordering codes on **page 44**.

		Maximum Resource Count for Stratix IV GT FPGAs (0.95 V)[1]					
		EP4S40G2	**EP4S40G5**	**EP4S100G2**	**EP4S100G3**	**EP4S100G4**	**EP4S100G5**
Resources	ALMs	91,200	212,480	91,200	116,480	141,440	212,480
	LEs (K)	228	531	228	291	354	531
	Registers[2]	182,400	424,960	182,400	232,960	282,880	424,960
	M9K memory blocks	1,235	1,280	1,235	936	1,248	1,280
	M144K memory blocks	22	64	22	36	48	64
	MLAB memory (Kb)	2,850	6,640	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	14,283	20,736	14,283	13,608	18,144	20,736
	18 x 18 multipliers	1,288	1,024	1,288	832	1,024	1,024
Architectural Features	Global clock networks	16					
	Regional clock networks	64	88	64	88	88	88
	Periphery clock networks	88	112	88	112	112	112
	PLLs	8	8	8	12	12	12
	Design security	✓					
	Others	Plug and play signal integrity, programmable power technology					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12					
	Emulated LVDS channels, 1,100 Mbps	192	256	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	46/46					
	Embedded DPA circuitry	✓					
	OCT	Series, parallel, and differential					
	Transceiver count[4] (11.3 Gbps/8.5 Gbps/6.5 Gbps)	12/12/12	12/12/12	24/0/12	24/8/16	24/8/16	32/0/16
	PCIe hard IP blocks	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR					

Notes:

1. Available in industrial temperatures only (0oC to 100oC).
2. The base core logic register count is shown. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50%.
3. 3.3 V compliant, requires a 3.0 V power supply.
4. The total transceiver count is the sum of the 11.3, 8.5, and 6.5 Gbps transceivers.

Stratix IV GX FPGA Features

View device ordering codes on **page 44**.

		Maximum Resource Count for Stratix IV GX FPGAs (0.9 V)						
		EP4SGX70	**EP4SGX110**	**EP4SGX180**	**EP4SGX230**	**EP4SGX290**	**EP4SGX360**	**EP4SGX530**
Resources	ALMs	29,040	42,240	70,300	91,200	116,480	141,440	212,480
	LEs (K)	73	106	176	228	291	354	531
	Registers[1]	58,080	84,480	140,600	182,400	232,960	282,880	424,960
	M9K memory blocks	462	660	950	1,235	936	1,248	1,280
	M144K memory blocks	16	16	20	22	36	48	64
	MLAB memory (Kb)	908	1,320	2,197	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	6,462	8,244	11,430	14,283	13,608	18,144	20,736
	18 x 18 multipliers	384	512	920	1,288	832	1,040[2]	1,024
Architectural Features	Global clock networks	16						
	Regional clock networks	64	64	64	64	88	88	88
	Periphery clock networks	56	56	88	88	88	88	112
	PLLs	4	4	8	8	12	12	12
	Design security	✓						
	Others	Plug and play integrity, programmable power technology						
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12						
	Emulated LVDS channels, 1,100 Mbps	128	128	192	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	56/56	88/88	88/88	98/98	98/98	98/98
	Embedded DPA circuitry	✓						
	OCT	Series, parallel, and differential						
	Transceiver count (8.5 Gbps/6.5 Gbps)[4]	16/8	16/8	24/12	24/12	32/16	32/16	32/16
	PCIe hard IP blocks	2	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR						

Notes:

1. The base core logic register count is shown. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50%.
2. The EP4SGX360N device has 1,024 18 x 18 multipliers.
3. 3.3 V compliant, requires a 3.0 V power supply.
4. The total transceiver count is the sum of 8.5 and 6.5 Gbps transceivers.

Stratix IV E FPGA Features

View device ordering codes on **page 44.**

		Maximum Resource Count for Stratix IV E FPGAs (0.9 V)			
		EP4SE230	**EP4SE360**	**EP4SE530**	**EP4SE820**
Resources	ALMs	91,200	141,440	212,480	325,220
	LEs (K)	228	354	531	813
	Registers[1]	182,400	282,880	424,960	650,440
	M9K memory blocks	1,235	1,248	1,280	1,610
	M144K memory blocks	22	48	64	60
	MLAB memory (Kb)	2,850	4,420	6,640	10,163
	Embedded memory (Kb)	14,283	18,144	20,736	23,130
	18 x 18 multipliers	1,288	1,040	1,024	960
Architectural Features	Global clock networks	16			
	Regional clock networks	64	88	88	88
	Periphery clock networks	88	88	112	132
	PLLs	4	12	12	12
	Design security	✓			
	Others	Programmable power technology			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12			
	Emulated LVDS channels, 1,100 Mbps	128	256	256	288
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	88/88	112/112	132/132
	Embedded DPA circuitry	✓			
	OCT	Series, parallel, and differential			
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR			

Notes:

1. Base core logic register count is shown. The ALM can support three registers when used in LUTREG mode, which can increase the total register count by an additional 50%.
2. 3.3 V compliant, requires a 3.0 V power supply.

Stratix IV FPGA Series Package and I/O Matrices

View device ordering codes on **page 44**.

		FBGA (F)[1]					
		780 pin 29 x 29 (mm) 1.0 mm pitch	**1,152 pin** 35 x 35 (mm) 1.0 mm pitch	**1,152 pin** 35 x 35 (mm) 1.0 mm pitch	**1,517 pin** 40 x 40 (mm) 1.0 mm pitch	**1,760 pin** 42.5 x 42.5 (mm) 1.0 mm pitch	**1,932 pin** 45 x 45 (mm) 1.0 mm pitch
Stratix IV GT FPGAs (0.95 V)	**EP4S40G2**				646 12+12+12		
	EP4S40G5				646[4] 12+12+12		
	EP4S100G2				646 24+0+12		
	EP4S100G3						769 24+8+16
	EP4S100G4						769 24+8+16
	EP4S100G5				646[4] 24+0+12		769 32+0+16
Stratix IV GX FPGAs (0.9 V)[2]	**EP4SGX70**	368 8+0		480 16+8			
	EP4SGX110	368 8+0	368 16+0	480 16+8			
	EP4SGX180	368 8+0	560 16+0	560 16+8	736 24+12		
	EP4SGX230	368 8+0	560 16+0	560 16+8	736 24+12		
	EP4SGX290	288[3] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
	EP4SGX360	288[3] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
	EP4SGX530			560[4] 16+8	736[4] 24+12	864 24+12	904 32+16
Stratix IV E FPGAs	**EP4SE820**		736[4]		960[4]	1,104	
	EP4SE530		736[4]		960[4]	960	
	EP4SE360	480[2]	736				
	EP4SE230	480					

Notes:

1. FineLine ball grid array.
2. I/O count does not include dedicated clock inputs that can be used as data inputs.
3. Hybrid package (flip chip) FBGA: 35 x 35 (mm) 1.0 mm pitch.
4. Hybrid package (flip chip) FBGA: 42.5 x 42.5 (mm) 1.0 mm pitch.

636 (12+12+12) Values on top indicate available user I/O pins; values on bottom indicate the sum of 11.3, 8.5, and 6.5 Gbps transceiver count.

636 (8+0) Values on top indicate available user I/O pins; values at the bottom indicate the sum of 8.5 and 6.5 Gbps transceiver count.

288 Number indicates available user I/O pins.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.
Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0 °C to 100 °C).

Arria II GZ FPGA Features

View device ordering codes on **page 44**.

		Maximum Resource Count for Arria II GZ FPGAs (0.9 V)		
		EP2AGZ225	**EP2AGZ300**	**EP2AGZ350**
Resources	ALMs	89,600	119,200	139,400
	LEs (K)	224	298	349
	Registers[1]	179,200	238,400	278,800
	M9K memory blocks	1,235	1,248	1,248
	M144K memory blocks	0	24	36
	MLAB memory (Kb)	2,850	4,420	4,420
	Embedded memory (Kb)	11,115	14,688	16,416
	18 x 18 multipliers	800	920	1,040
Architectural Features	Global clock networks	16		
	Regional clock networks	64	88	88
	Periphery clock networks	88		
	PLLs	8	8	8
	Design security	✓		
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0		
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 ((I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12		
	Emulated LVDS channels, 1,152 Mbps	184	184	184
	LVDS channels, 1,250 Mbps (receive/transmit)	Up to 86		
	Embedded DPA circuitry	✓		
	OCT	Series and differential		
	Transceiver count (6.375 Gbps)	Up to 24		
	PCIe hard IP blocks (Base specification, Rev 1.1, 2.0, etc.)	1		
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM 2, SDR		

Notes:
1. Base core logic register count is shown. The ALM can support three registers when used in LUTREG mode, which can increase the total register count by an additional 50%.

Arria II GX FPGA Features

View device ordering codes on **page 44**.

		Maximum Resource Count for Arria II GX FPGAs (0.9 V)					
		EP2AGX45	**EP2AGX65**	**EP2AGX95**	**EP2AGX125**	**EP2AGX190**	**EP2AGX260**
Resources	ALMs	18,050	25,300	37,470	49,640	76,120	102,600
	LEs (K)	43	60	89	118	118	244
	Registers[1]	36,100	50,600	74,940	99,280	152,240	205,200
	M9K memory blocks	319	495	612	730	840	950
	MLAB memory (Kb)	564	791	1,171	1,551	2,379	3,206
	Embedded memory (Kb)	2,871	4,455	5,508	6,570	7,560	8,550
	18 x 18 multipliers	232	312	448	576	656	736
Architectural Features	Global clock networks	16					
	Regional clock networks	48					
	Periphery clock networks	50	50	59	59	84	84
	PLLs	4	4	6	6	6	6
	Design security	✓					
	Others	Plug and play signal integrity					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12					
	Emulated LVDS channels, 945 Mbps	56	56	64	64	96	96
	LVDS channels, 1,250 Mbps (receive/transmit)	85/84	85/84	105/104	105/104	145/144	145/144
	Embedded DPA circuitry	✓					
	OCT	Series and differential					
	Transceiver count (6.375 Gbps)	8	8	12	12	16	16
	PCIe hard IP block (Gen1)	1					
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II					

Notes:

1. This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50%.

Arria II GZ and GX FPGA Series Package and I/O Matrices

View device ordering codes on **page 44**.

	Arria II GX FPGAs (0.9 V)			
	UBGA (U)[1]	FBGA (F)		
	358 pin 17 x 17 (mm) 0.8 mm pitch	**572 pin** 25 x 25 (mm) 1.0 mm pitch	**780 pin** 29 x 29 (mm) 1.0 mm pitch	**1,152 pin** 35 x 35 (mm) 1.0 mm pitch
EP2AGX45	156 4	252 8	364 8	
EP2AGX65	156 4	252 8	364 8	
EP2AGX95		260 8	372 12	452 12
EP2AGX125		260 8	372 12	452 12
EP2AGX190			372 12	612 16
EP2AGX260			372 12	612 16

Notes:

1. Ultra FineLine ball grid array.

726 / 24 Values on top indicate available user I/O pins; values at the bottom indicate the 6.375 Gbps transceiver count.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/Os pins may be less than the number stated in the table.

	Arria II GZ FPGAs (0.9 V)		
	Hybrid FBGA (H)	FBGA (F)	
	780 pin 33 x 33 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch
EP2AGZ225		554 16	734 24
EP2AGZ300	281 16	554 16	734 24
EP2AGZ350	281 16	554 16	734 24

636 / 12 Values on top indicate available user I/O pins; values at the bottom indicate the 6.375 Gbps transceiver count.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.

Cyclone IV GX FPGA Features

View device ordering codes on **page 44**.

		Maximum Resource Count for Cyclone IV GX FPGAs (1.2 V)						
		EP4CGX15	**EP4CGX22**	**EP4CGX30**	**EP4CGX50**	**EP4CGX75**	**EP4CGX110**	**EP4CGX150**
Resources	LEs (K)	14	21	29	50	74	109	150
	M9K memory blocks	60	84	120	278	462	666	720
	Embedded memory (Kb)	540	756	1,080	2,502	4,158	5,490	6,480
	18 x 18 multipliers	0	40	80	140	198	280	360
Architectural Features	Global clock networks	20	20	20	30	30	30	30
	PLLs	3	4	4	8	8	8	8
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12						
	Emulated LVDS channels	9	40	40	73	73	139	139
	LVDS channels, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59
	Transceiver count[1] (2.5 Gbps/3.125 Gbps)	2/0	2, 0 / 4, 0	4, 0 / 0, 4[2]	0, 8	0, 8	0, 8	0, 8
	PCIe hard IP blocks (Gen1)	1						
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR						

Notes:
1. Transceiver performance varies by product line and package offering.
2. EP4CGX30 supports 3.125 Gbps transceivers only in F484 package option.

Cyclone IV E FPGA Features

View device ordering codes on **page 44**.

		Maximum Resource Count for Cyclone IV E FPGAs								
		EP4CE6	**EP4CE10**	**EP4CE15**	**EP4CE22**	**EP4CE30**	**EP4CE40**	**EP4CE55**	**EP4CE75**	**EP4CE115**
Resources	LEs (K)	6	10	15	22	29	40	56	75	114
	M9K memory blocks	30	46	56	66	66	126	260	305	432
	Embedded memory (Kb)	270	414	504	594	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	15	23	56	66	66	116	154	200	266
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20	20
	PLLs	2	2	4	4	4	4	4	4	4
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3								
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12								
	LVDS channels	66	66	137	52	224	224	160	178	230
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR								

Cyclone IV GX and E FPGA Series Package and I/O Matrices

View device ordering codes on **page 44**.

	Cyclone IV GX FPGAs (1.2 V)					
	QFN (N)[1]	FBGA (F)				
	148 pin 11 x 11 (mm) 0.5 mm pitch	**169 pin** 14 x 14 (mm) 1.0 mm pitch	**324 pin** 19 x 19 (mm) 1.0 mm pitch	**484 pin** 23 x 23 (mm) 1.0 mm pitch	**672 pin** 27 x 27 (mm) 1.0 mm pitch	**896 pin** 31 x 31 (mm) 1.0 mm pitch
EP4CGX15	72 2	72 2				
EP4CGX22		72 2	150 4			
EP4CGX30		72 2	150 4	290 4		
EP4CGX50				290 4	310 8	
EP4CGX75				290 4	310 8	
EP4CGX110				270 4	393 8	475 8
EP4CGX150				270 4	393 8	475 8

Notes:

1. Quad flat pack, no lead.

636 / 12 Values on top indicate available user I/O pins; values at the bottom indicate the 2.5 Gbps or 3.125 Gbps transceiver count.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.

	Cyclone IV E FPGAs (1.0 V and 1.2 V)							
	EQFP (E)[1]	FBGA (F)				MBGA (M)	UBGA (U)	
	144 pin 22 x 22 (mm) 0.5 mm pitch	**256 pin** 17 x 17 (mm) 1.0 mm pitch	**324 pin** 19 x 19 (mm) 1.0 mm pitch	**484 pin** 23 x 23 (mm) 1.0 mm pitch	**780 pin** 29 x 29 (mm) 1.0 mm pitch	**164 pin** 8 x 8 (mm) 0.5 mm pitch	**256 pin** 14 x 14 (mm) 0.8 mm pitch	**484 pin** 19 x 19 (mm) 0.8 mm pitch
EP4CE6	91	179					179	
EP4CE10	91	179					179	
EP4CE15	81	165		343		74	165	
EP4CE22	79	153					153	
EP4CE30			193	328	532			
EP4CE40			193	328	532			328
EP4CE55				324	374			324
EP4CE75				292	426			292
EP4CE115				280	528			

Notes:

1. Enhanced thin quad flat pack.

636 Number indicates available user I/O pins.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.

Cyclone III FPGA Features

View device ordering codes on **page 44**.

		Maximum Resource Count for Cyclone III FPGAs (1.2 V)							
		EP3C5	**EP3C10**	**EP3C16**	**EP3C25**	**EP3C40**	**EP3C55**	**EP3C80**	**EP3C120**
Resources	LEs (K)	5	10	15	25	40	56	81	119
	M9K memory blocks	46	46	56	66	126	260	305	432
	Embedded memory (Kb)	414	414	504	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	23	23	56	66	126	156	244	288
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	PLLs	2	2	4	4	4	4	4	4
	Design security	–							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3							
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, LVPECL, SSTL-18 (1 and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), Differential HSTL							
	Emulated LVDS channels, 840 Mbps	66	66	136	79	223	159	177	229
	OCT	Series and differential							
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR							

Cyclone III LS FPGA Features

View device ordering codes on **page 44.**

		Maximum Resource Count for Cyclone III LS FPGAs (1.2 V)			
		EP3CLS70	**EP3CLS100**	**EP3CLS150**	**EP3CLS200**
Resources	LEs (K)	70	100	151	198
	M9K memory blocks	333	483	666	891
	Embedded memory (Kb)	2,997	4,347	5,994	8,019
	18 x 18 multipliers	200	276	320	396
Architectural Features	Global clock networks	20			
	PLLs	4			
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, LVPECL, SSTL-18 (1 and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), Differential HSTL			
	LVDS channels, 840 Mbps	169			
	OCT	Series and differential			
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR			

Cyclone III Series Package and I/O Matrices

View device ordering codes on **page 44.**

	Cyclone III FPGAs (1.2 V)								
	EQFP (E)	MBGA (M)[1]	PQFP (Q)[2]	FBGA (F)				UBGA (U)	
	144 pin 22 x 22 (mm) 0.5 mm pitch	164 pin 8 x 8 (mm) 0.5 mm pitch	240 pin 34.6 x 34.6 (mm) 0.5 mm pitch	256 pin 17 x 17 (mm) 1.0 mm pitch	324 pin 19 x 19 (mm) 1.0 mm pitch	484 pin 23 x 23 (mm) 1.0 mm pitch	780 pin 29 x 29 (mm) 1.0 mm pitch	256 pin 14 x 14 (mm) 0.8 mm pitch	484 pin 19 x 19 (mm) 0.8 mm pitch
EP3C5	94	106		182				182	
EP3C10	94	106		182				182	
EP3C16	84	92	160	168		346		168	346
EP3C25	82		148	156	215			156	
EP3C40			128		196	331	535		331
EP3C55						327	377		327
EP3C80						295	429		295
EP3C120						283	531		
EP3CLS70						294	429		294
EP3CLS100						294	429		294
EP3CLS150						226	429		
EP3CLS200						226	429		

Notes:
1. Micro FineLine BGA.
2. Plastic quad flat pack.

636 Number indicates available user I/O pins.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.

MAX V CPLD Features

View device ordering codes on **page 44**.

		MAX V CPLDs (1.8 V)						
		5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
Density and Speed	LEs	40	80	160	240	570	1270	2210
	Equivalent macrocells[1]	32	64	128	192	440	980	1700
	Pin-to-pin delay (ns)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
	User flash memory (Kb)	8						
	Logic convertible to memory[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Architectural Features	Internal oscillator	✓						
	Digital PLL[3]	✓						
	Fast power-on reset	✓						
	Boundary-scan JTAG	✓						
	JTAG ISP	✓						
	Fast input registers	✓						
	Programmable register power-up	✓						
	JTAG translator	✓						
	Real-time ISP	✓						
I/O Features	MultiVolt I/Os (V)	1.2, 1.5, 1.8, 2.5, 3.3					1.2, 1.5, 1.8, 2.5, 3.3, 5.0[4]	
	I/O power banks	2	2	2	2	2	4	4
	Maximum output enables	54	54	79	114	159	271	271
	LVTTL/LVCMOS	✓						
	LVDS outputs	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	32 bit, 66 MHz PCI compliant	–	–	–	–	–	✓[4]	✓[4]
	Schmitt triggers	✓						
	Programmable slew rate	✓						
	Programmable pull-up resistors	✓						
	Programmable GND pins	✓						
	Open-drain outputs	✓						
	Bus hold	✓						

Notes:

1. Typical equivalent macrocells.
2. Unused LEs can be converted to memory. The total number of available LE RAM bits depends on the memory mode, depth, and width configurations of the instantiated memory.
3. Optional IP core. Contact your Altera sales representative for availability.
4. An external resistor must be used for 5.0 V tolerance.

MAX II CPLD Features

View device ordering codes on **page 44**.

		MAX II CPLDs (3.3 V, 2.5 V, 1.8 V)			
		EPM240/Z	**EPM570/Z**	**EPM1270**	**EPM2210**
Density and Speed	Equivalent macrocells[1]	192	440	980	1,700
	Pin-to-pin delay (ns)	4.7, 7.5	5.4, 9.0	6.2	7.0
Architectural Features	User flash memory (Kb)	8			
	Boundary-scan JTAG	✓			
	JTAG ISP	✓			
	Fast input registers	✓			
	Programmable register power-up	✓			
	JTAG translator	✓			
	Real-time ISP	✓			
I/O Features	MultiVolt I/Os (V)	1.5, 1.8, 2.5, 3.3	1.5, 1.8, 2.5, 3.3	1.5, 1.8, 2.5, 3.3, 5.0[2]	1.5, 1.8, 2.5, 3.3, 5.0[2]
	I/O power banks	2	2	4	4
	Maximum output enables	80	160	212	272
	LVTTL/LVCMOS	✓			
	32 bit, 66 MHz PCI compliant	–	–	✓[2]	✓[2]
	Schmitt triggers	✓			
	Programmable slew rate	✓			
	Programmable pull-up resistors	✓			
	Programmable GND pins	✓			
	Open-drain outputs	✓			
	Bus hold	✓			

Notes:

1. Typical equivalent macrocells.
2. An external resistor must be used for 5 V tolerance.

MAX V and MAX II CPLD Series Package and I/O Matrices

View device ordering codes on **page 44**.

	MAX V CPLDs (1.8 V)[1]							
	EQFP (E)[2]	TQFP (T)[3]		MBGA (M)[4]			FBGA (F)	
	64 pin 7 x 7 (mm) 0.4 mm pitch	**100 pin** 14 x 14 (mm) 0.5 mm pitch	**144 pin** 20 x 20 (mm) 0.5 mm pitch	**64 pin** 4.5 x 4.5 (mm) 0.5 mm pitch	**68 pin** 5 x 5 (mm) 0.5 mm pitch	**100 pin** 6 x 6 (mm) 0.5 mm pitch	**256 pin** 17 x 17 (mm) 1.0 mm pitch	**324 pin** 19 x 19 (mm) 1.0 mm pitch
5M40Z	54			30				
5M80Z	54	79		30	52			
5M160Z	54	79			52	79		
5M240Z		79	114		52	79		
5M570Z		74	114			74	159	
5M1270Z			114				211	271
5M2210Z							203	271

	MAX II CPLDs (3.3 V, 2.5 V, 1.8 V)[1]								
	TQFP (T)		FBGA (F)			MBGA (M)			
	100 pin 16 x 16 (mm) 0.5 mm pitch	**144 pin** 22 x 22 (mm) 0.5 mm pitch	**100 pin** 11 x 11 (mm) 1.0 mm pitch	**256 pin** 17 x 17 (mm) 1.0 mm pitch	**324 pin** 19 x 19 (mm) 1.0 mm pitch	**68 pin** 5 x 5 (mm) 0.5 mm pitch	**100 pin** 6 x 6 (mm) 0.5 mm pitch	**144 pin** 7 x 7 (mm) 0.5 mm pitch	**256 pin** 11 x 11 (mm) 0.5 mm pitch
EPM240Z						54	80		
EPM570Z							76	116	160
EPM240	80		80				80		
EPM570	76	116	76	160			76		160
EPM1270		116		212					212
EPM2210				204	272				

Notes:

1. For temperature grades of specific packages (commercial, industrial, or extended temperatures), refer to Altera's online selector guide.
2. Enhanced quad flat pack.
3. Thin quad flat pack.
4. Micro FineLine BGA (0.5 mm).

636 Number indicates available user I/O pins.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.

Configuration Devices

www.altera.com/devices/common/serialcfg/scg-index.html

View device ordering codes on **page 45.**

The following information is an overview of our configuration devices. To determine the right configuration device for your FPGA, refer to our *Configuration Handbook* or the configuration chapter in the handbook of your selected FPGA.

Altera's serial configuration devices store the configuration file for our SRAM-based FPGAs. We designed our serial configuration devices to minimize board space while providing a dedicated FPGA configuration solution. Serial configuration devices are recommended for new designs. For information on additional configuration devices supporting older products, see our *Configuration Handbook*.

	EPCQ-L Serial Configuration Devices for Arria 10 FPGAs (1.8 V)
	FBGA
	24 pin 6 x 8 (mm) 1.0-mm pitch
EPCQL256	256
EPCQL512	512
EPCQL1024	1,024

Notes:

512 Number indicates memory size in megabits (Mb).

Vertical migration (same V_{cc}, GND, ISP, and input pins).

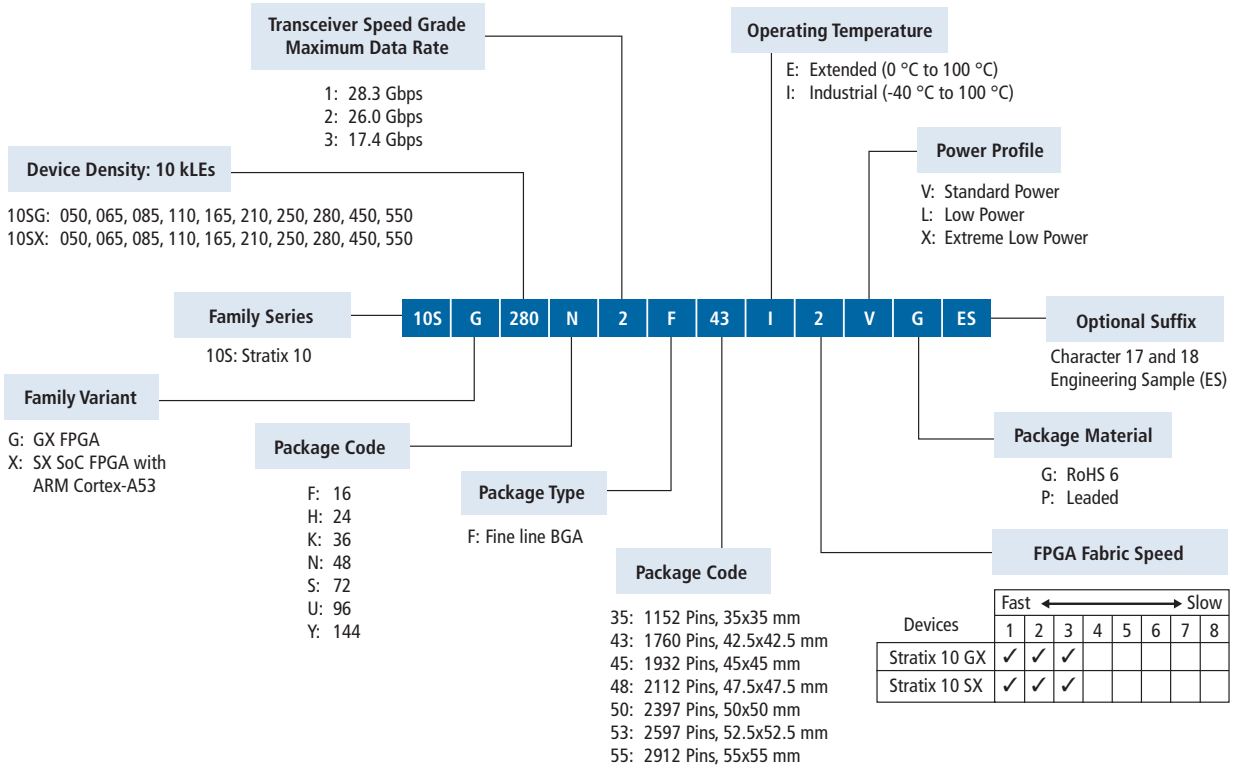
	EPCQ Serial Configuration Devices for 28 nm and Prior FPGAs (3.0–3.3 V)	
	SOIC	
	8 pin 4.9 x 6.0 (mm)	**16 pin** 10.3 x 10.3 (mm)
EPCQ16	16	
EPCQ32	32	
EPCQ64		64
EPCQ128		128
EPCQ256		256
EPCQ512		512

Notes:

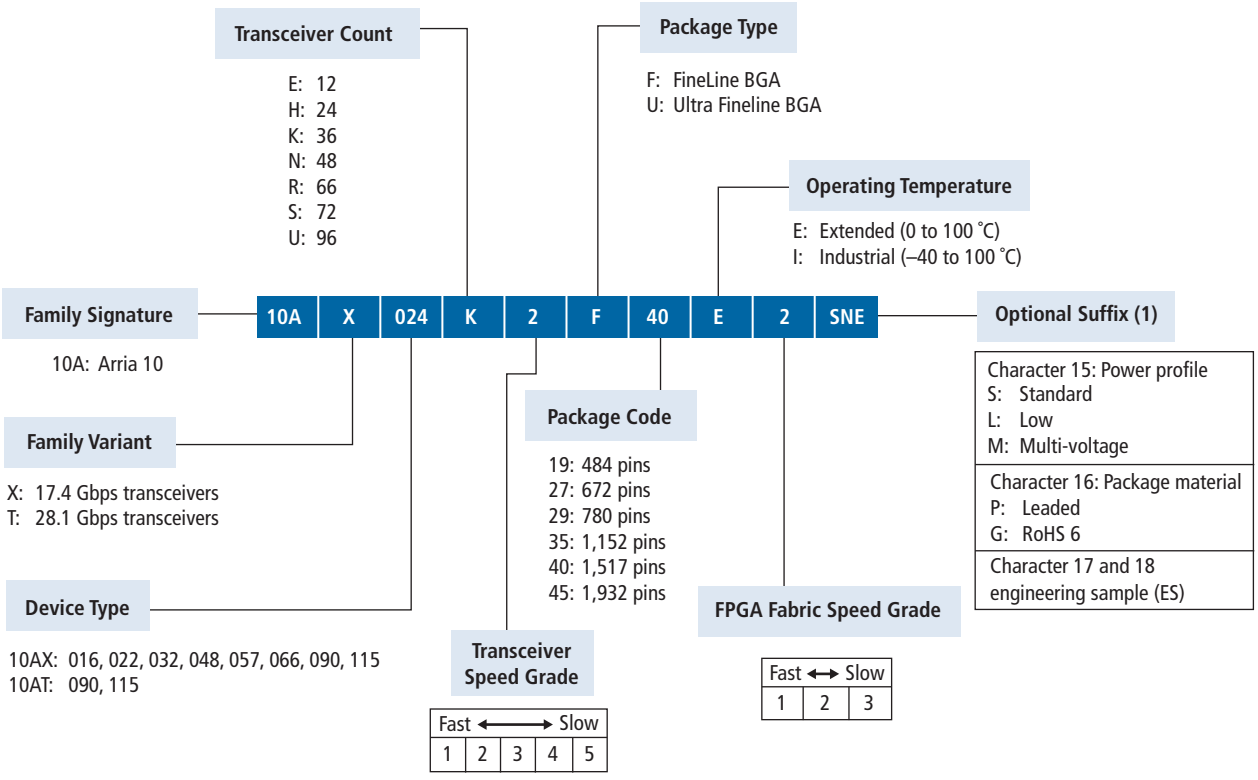
512 Number indicates memory size in megabits (Mb).

Vertical migration (same V_{cc}, GND, ISP, and input pins).

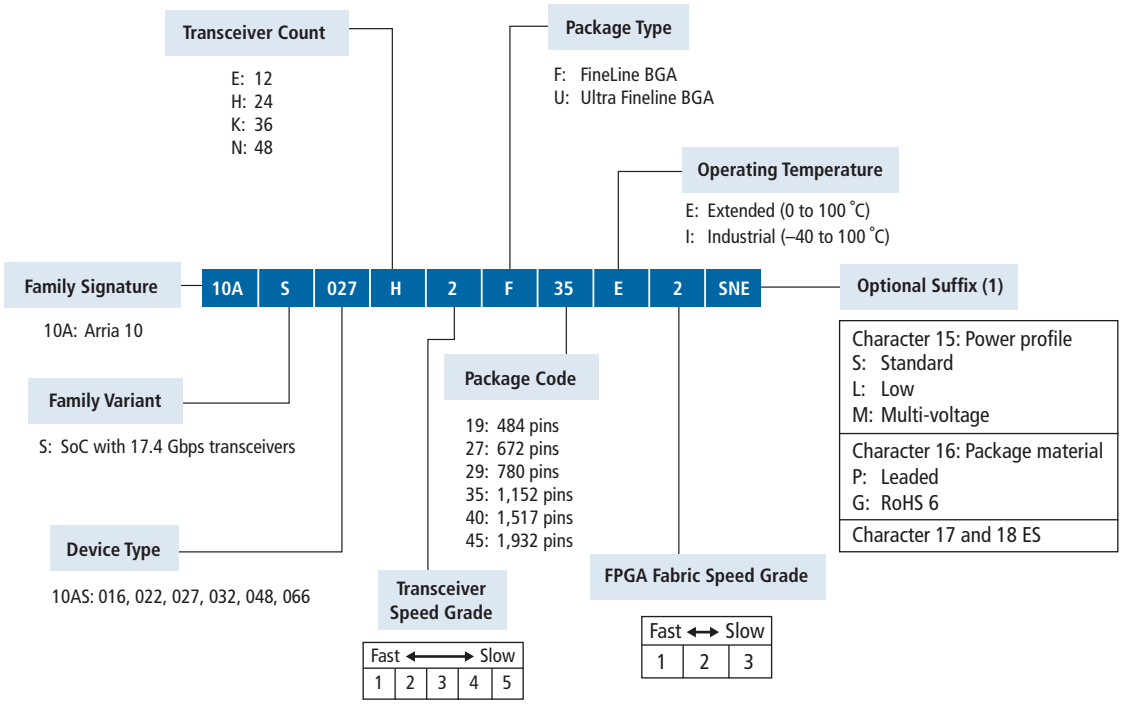
Ordering Information for Stratix 10 (GX/SX) Devices



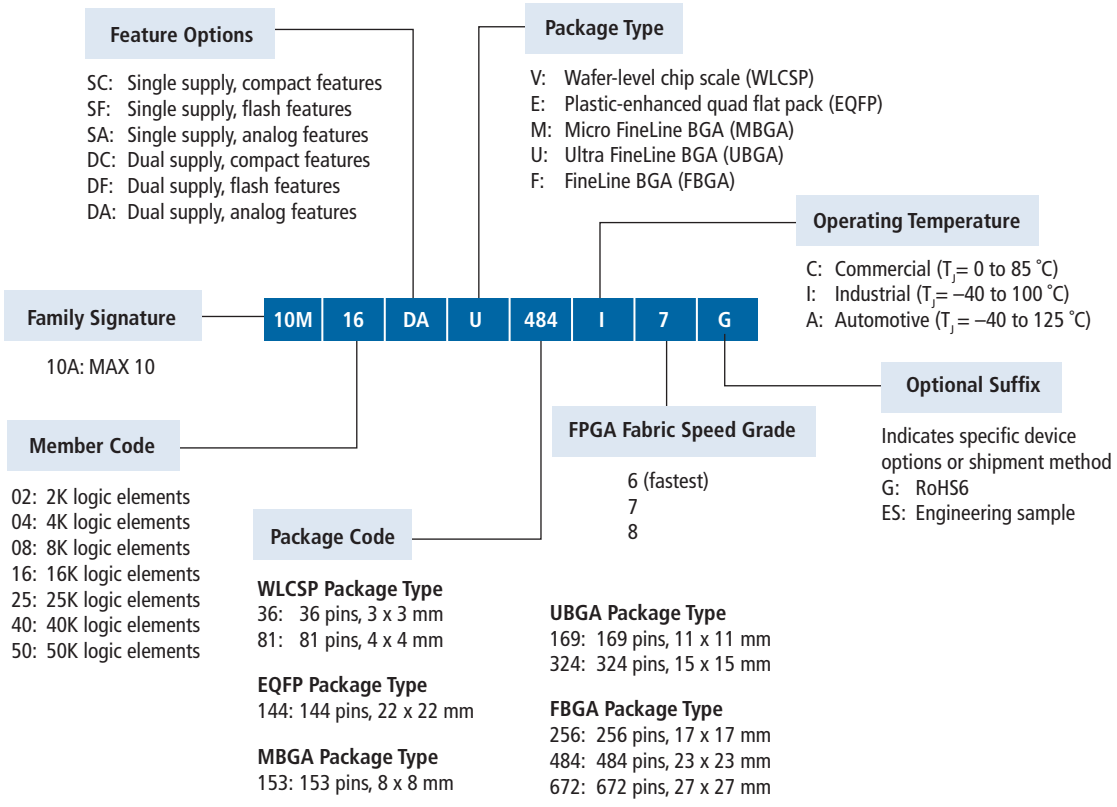
Ordering Information for Arria 10 (GX, GT) Devices



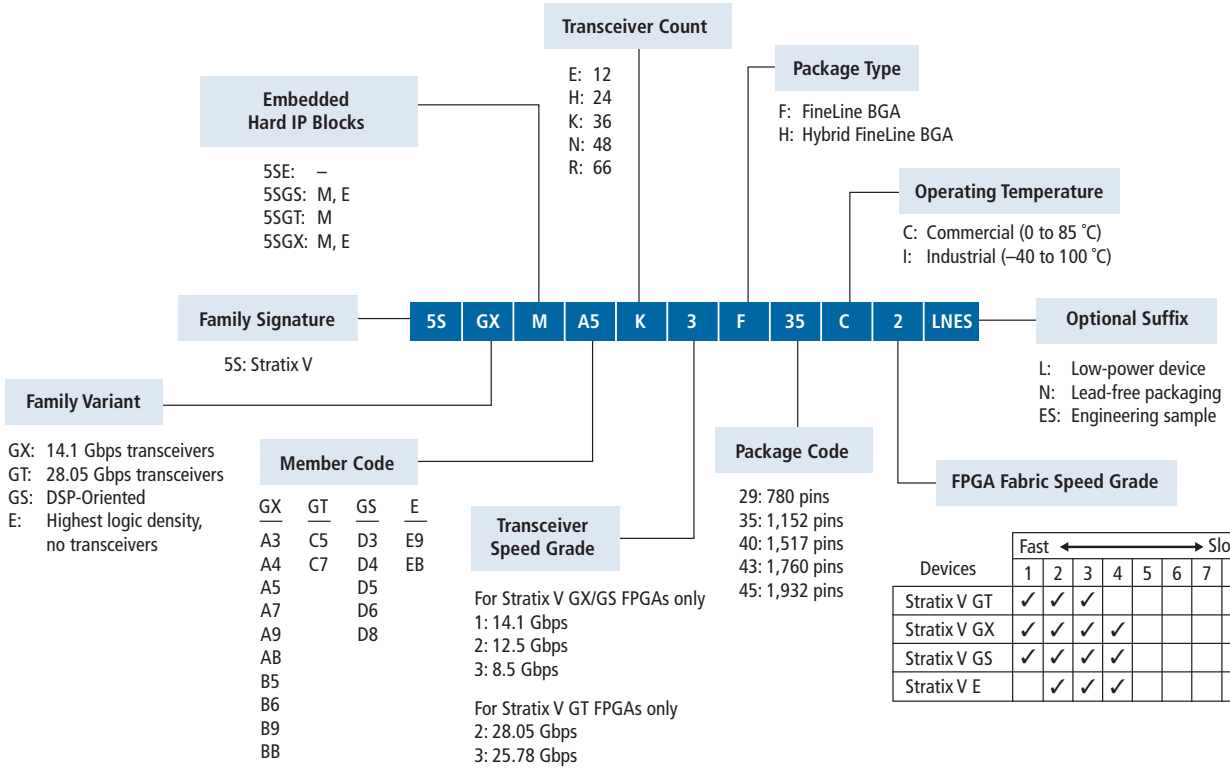
Ordering Information for Arria 10 (SX) SoCs



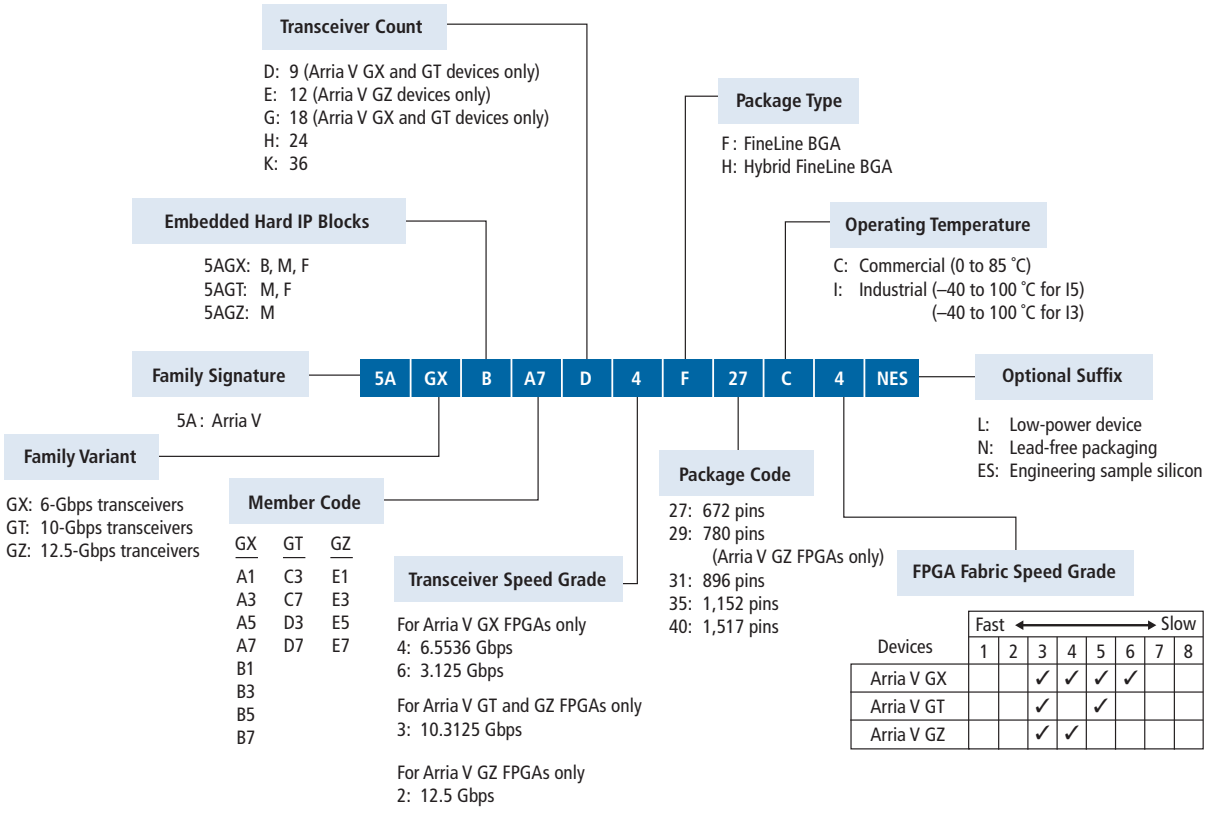
Ordering Information for MAX 10 Devices



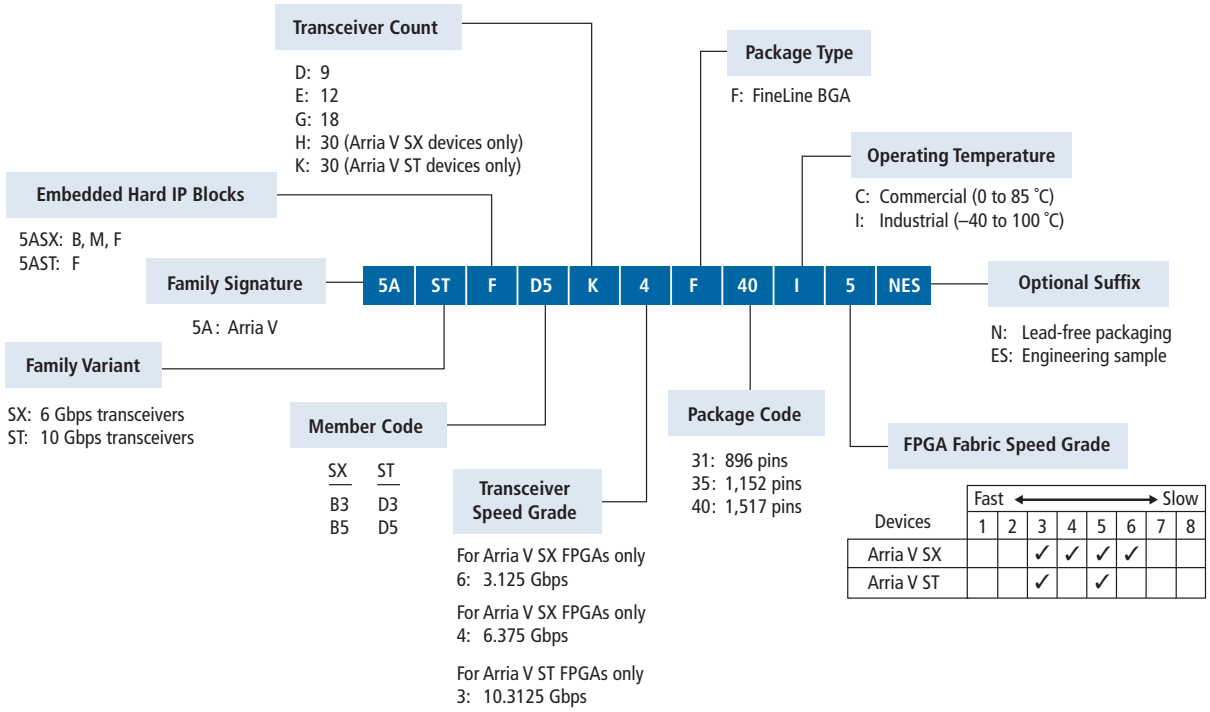
Ordering Information for Stratix V (GT, GX, GS, E) Devices



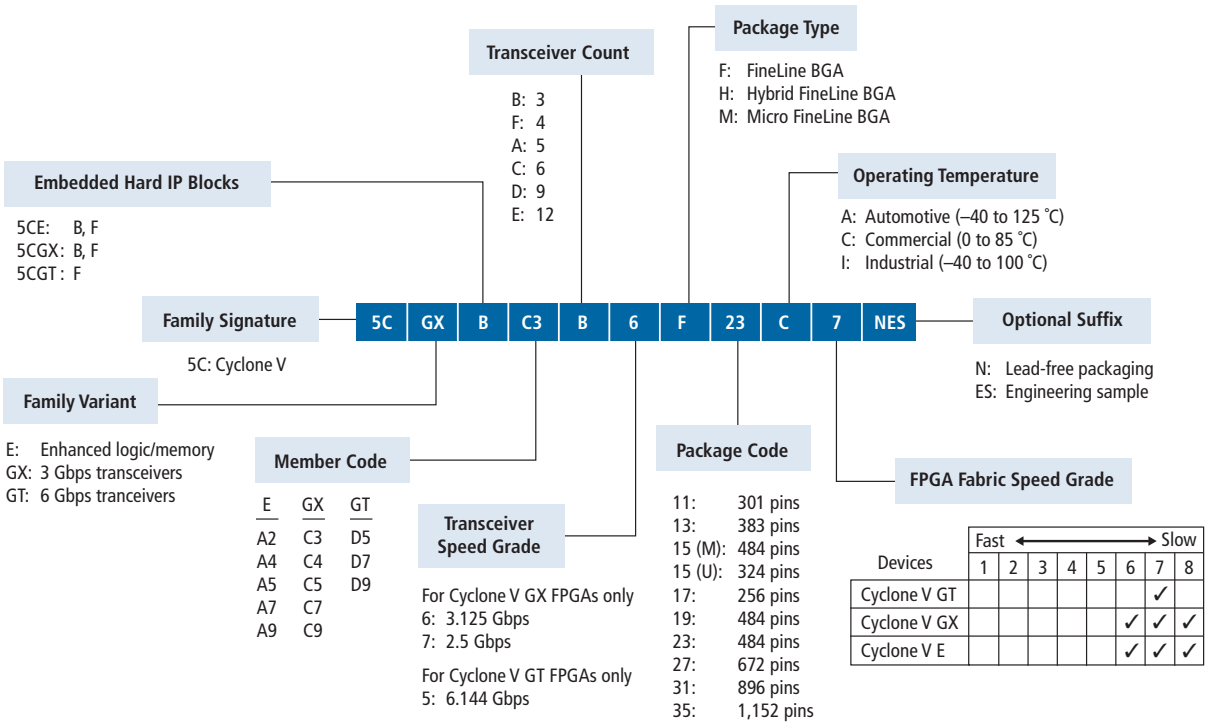
Ordering Information for Arria V (GT, GX, GZ) Devices



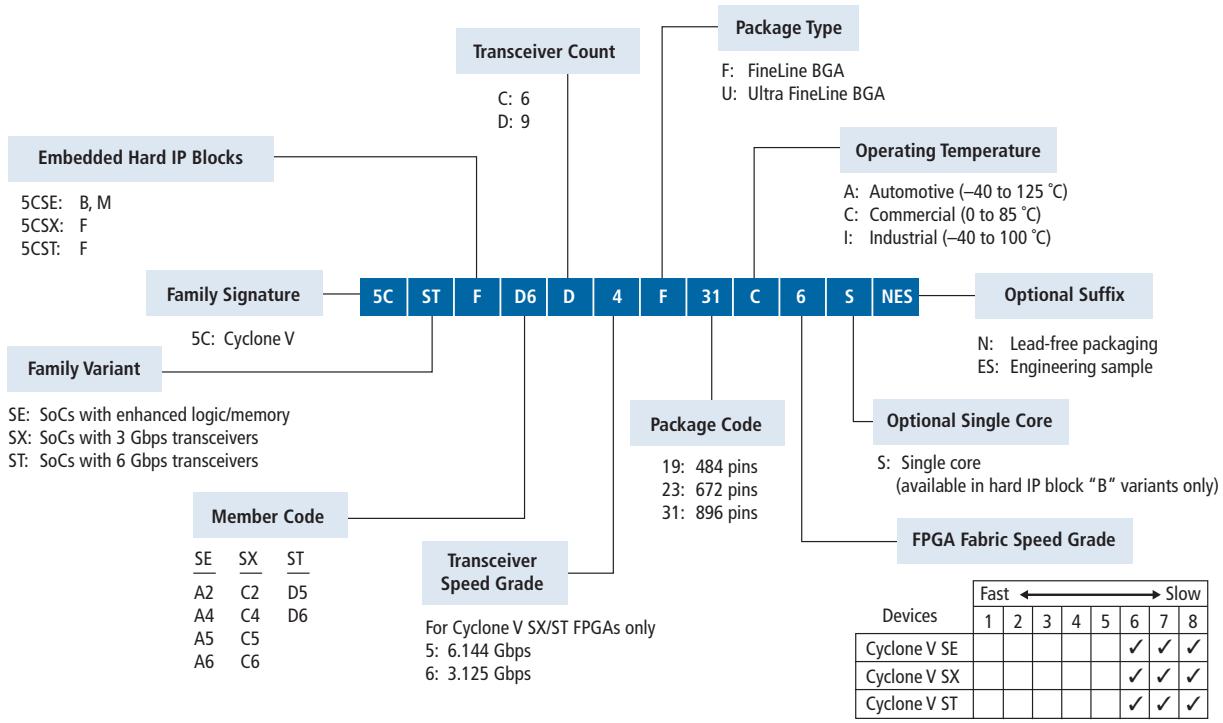
Ordering Information for Arria V (SX, ST) SoCs



Ordering Information for Cyclone V (E, GX, GT) Devices

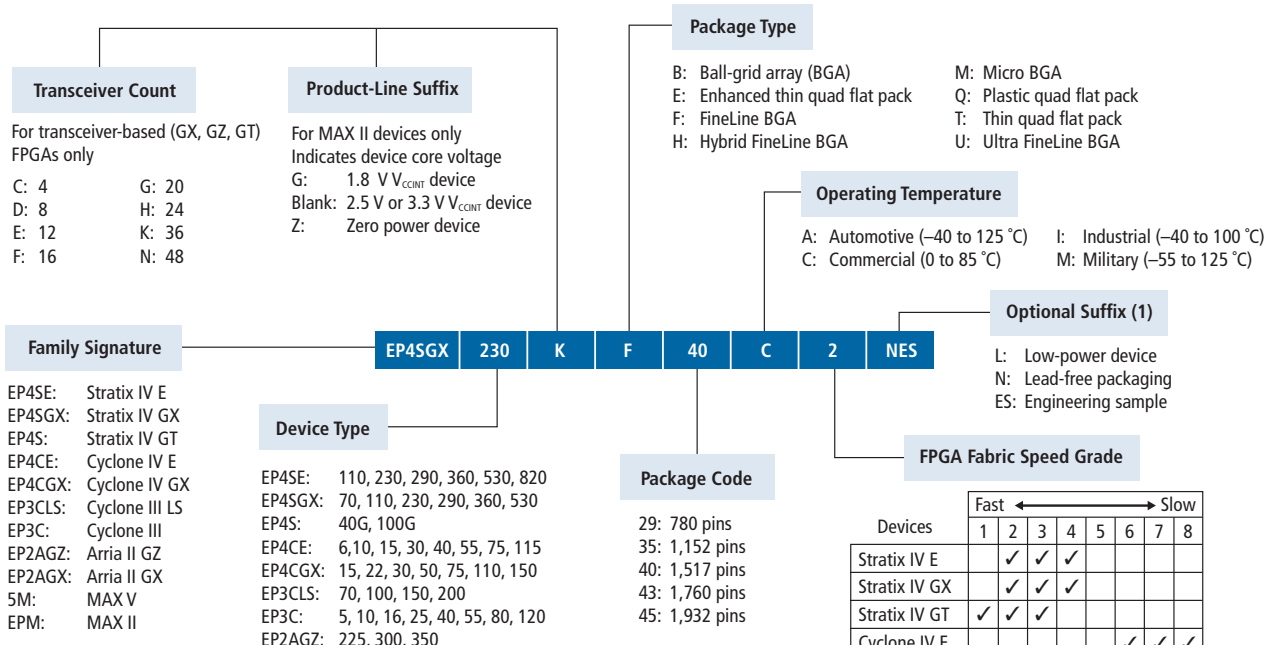


Ordering Information for Cyclone V (SE, SX, ST) SoCs



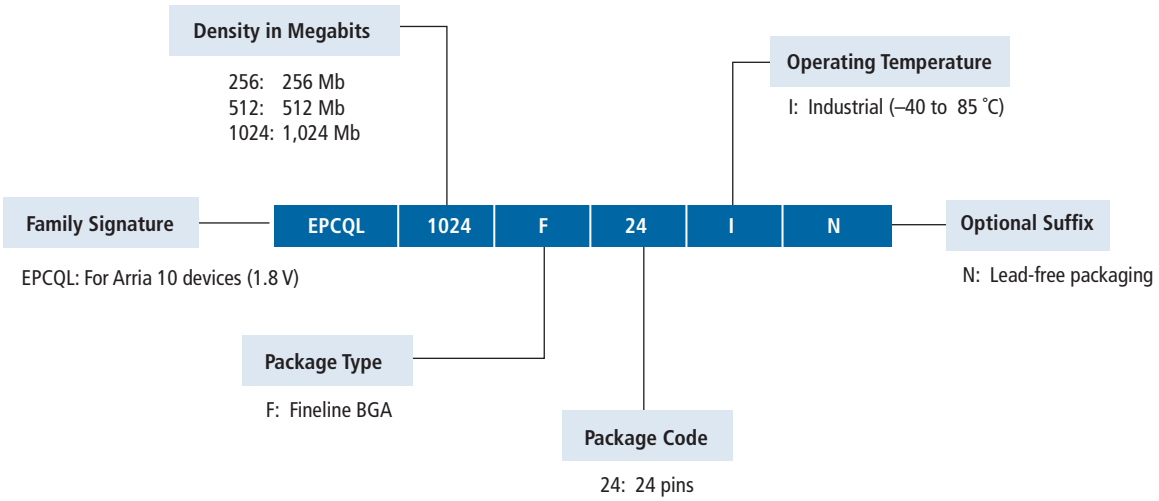
Devices	Fast ← 1	2	3	4	5	6	7	Slow → 8
Cyclone V SE						✓	✓	✓
Cyclone V SX						✓	✓	✓
Cyclone V ST						✓	✓	✓

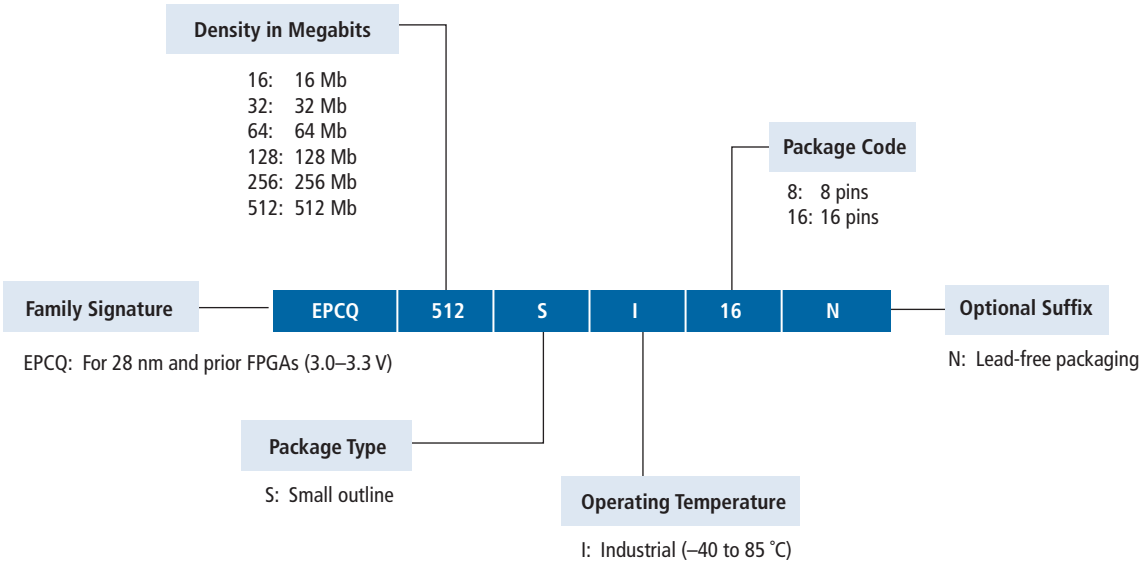
Ordering Information for Stratix IV (E, GX, GT), Cyclone IV (E, GX), Cyclone III, MAX V, and MAX II



Devices	Fast ← 1	2	3	4	5	6	7	Slow → 8
Stratix IV E		✓	✓	✓				
Stratix IV GX		✓	✓	✓				
Stratix IV GT	✓	✓	✓					
Cyclone IV E						✓	✓	✓
Cyclone IV GX						✓	✓	✓
Cyclone III LS							✓	✓
Cyclone III						✓	✓	✓
Arria II GZ			✓	✓				
Arria II GX			✓	✓	✓	✓		
MAX V				✓	✓			
MAX II			✓	✓	✓			

Ordering Information for Serial Configuration Devices





Enpirion Power Solutions

www.altera.com/power

Altera develops FPGAs and CPLDs using advanced process technologies that provide fast performance and high logic density. To meet demanding power requirements, Altera's Enpirion products deliver the industry's first family of power system-on-chip (PowerSoC) DC-DC converters featuring integrated inductors. They provide an industry-leading combination of high efficiency, small footprint, and low-noise performance.

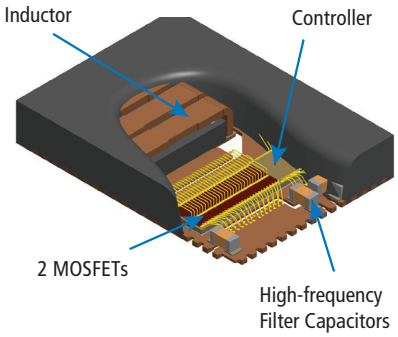
Powering Your Innovation with Enpirion PowerSoCs

Key Intellectual Property

- High-frequency power conversion
- Innovative magnetics engineering
- Advanced power packaging and construction

Integrated Power Management Systems

- Industry leading integrated PowerSoC DC-DC step-down converters



Meeting Your Toughest Power Challenges

- Maximize performance
- Reduce system power consumption
- Increase power density
- Increase system reliability
- Accelerate time to revenue

Achieve Unprecedented Power Density and Performance with Enpirion PowerSoC DC-DC Step-down Converters

Addressing today's and tomorrow's system power design challenges:

Highest Power Density and Smallest Footprint

Greatly minimizes the amount of PCB space and height profile required for point-of-load regulation compared to alternative discrete switching regulators and modules.

High Efficiency and Thermal Performance

Optimized with up to 96 percent efficiency. High-efficiency devices are industrial graded, from –40 to 85 °C ambient temperature and most solutions operate without load de-rating.

Lowest Component Count and Higher Reliability

PowerSoCs are specified, simulated, characterized, validated, and manufacturing-tested as a complete power system. Fewer components and tightly controlled IC manufacturing processes permit an unsurpassed 45,000-year mean time between failures (MTBF) reliability.

Ease of Design and Fastest Time to Market

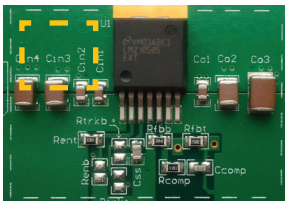
PowerSoCs with integrated inductor and compensation enable turnkey designs. Development requires fewer design steps with significantly less exposure to design iteration versus discrete switching regulators.

Fully Validated Power Solutions

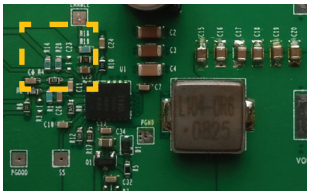
Fully validated PCB layout and design files enable customers nearly 100 percent first-pass success.

PowerSoC Comparison

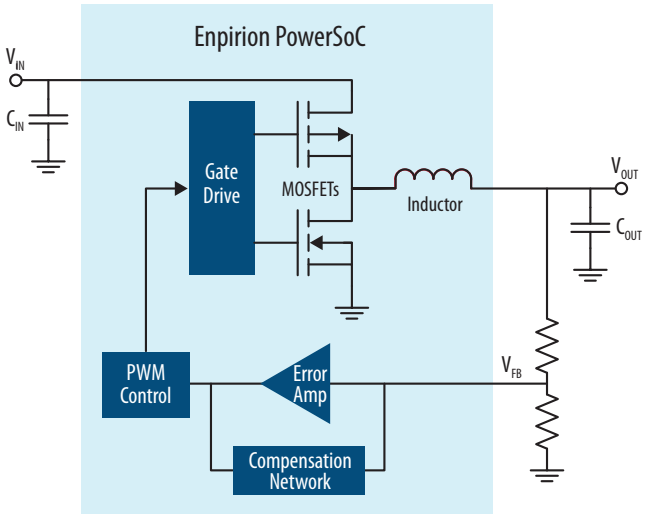
PowerSoC— 25% to 50% smaller footprint than alternative solutions

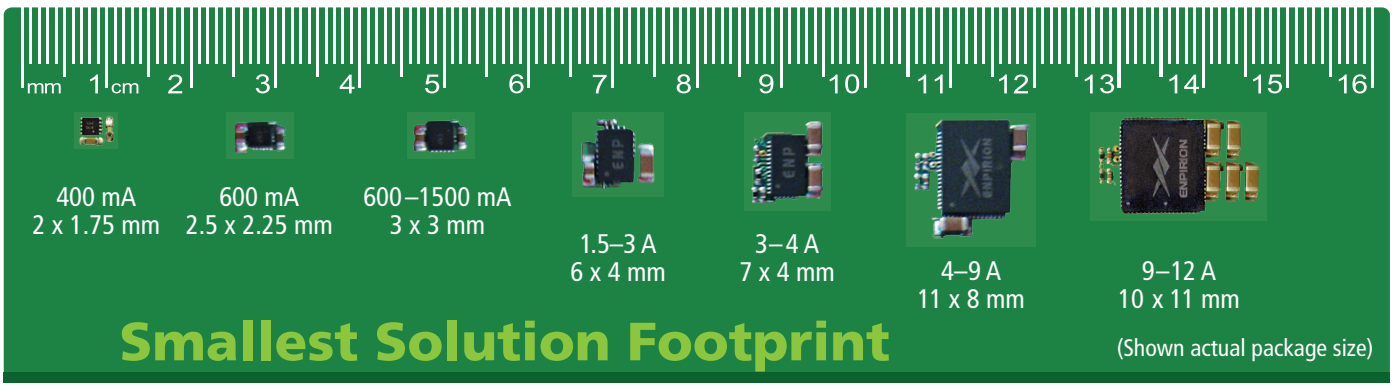


Competitor Module



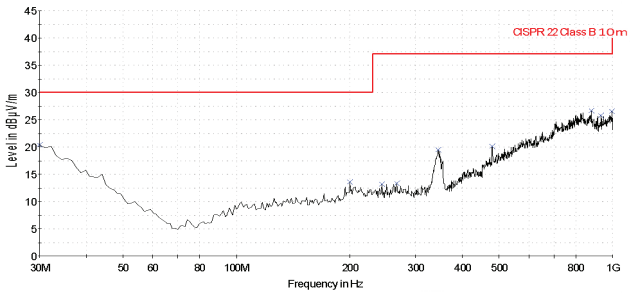
Competitor Discrete Regulator



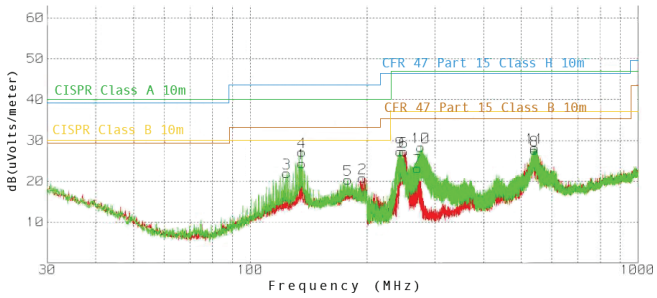


Low Radiated Noise

Enpirion Power Solutions

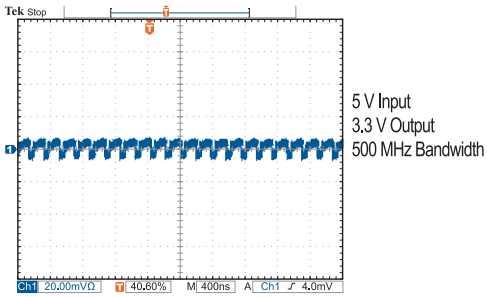


Competitor



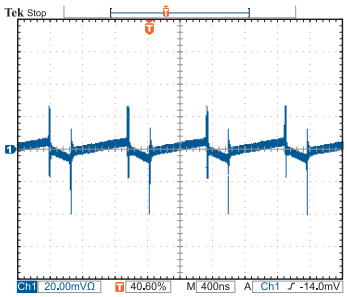
Low Ripple

Enpirion Power Solutions



5 V Input
3.3 V Output
500 MHz Bandwidth

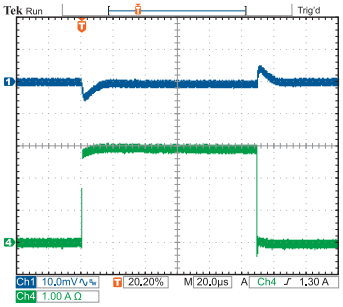
Competitor



5 V Input
3.3 V Output
500 MHz Bar

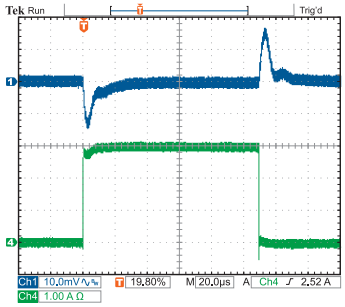
Fast Dynamic Response

Enpirion Power Solutions



5 V Input
3.3 V Output

Competitor



5 V Input
3.3 V Output

Featured PowerSoC Products

Part Number	I_{OUT} (A)	V_{IN} Range (VDC)	V_{OUT} Range (VDC)[1]	Pkg (pins)	Pkg Size (mm) L	W	H	Solution Size (mm^2)[3]	Resistor V_{OUT} Adjust	VID V_{OUT} Adjust	Power Good	Programmable Soft-Start	Margining	Input Sync	Output Sync	Parallel Capability	Automotive Grade Option
EP5348UI	0.4	2.5 – 5.5	0.60 – Note 1	uQFN14	2.0	1.75	0.9	21	•								
EP535[x]HUI[2]	0.6	2.4 – 5.5	1.80 – 3.3	uQFN16	2.5	2.25	1.1	14		3-pin							•
EP535[x]LUI[2]	0.6	2.4 – 5.5	0.60 – Note 1	uQFN16	2.5	2.25	1.1	14	•	3-pin							
EP53A[x]HQI[2]	1.0	2.4 – 5.5	1.80 – 3.3	QFN16	3.0	3.0	1.1	21		3-pin							•
EP53A[x]LQI[2]	1.0	2.4 – 5.5	0.60 – Note 1	QFN16	3.0	3.0	1.1	21	•	3-pin							
EN6310QI	1.0	2.7 – 5.5	0.60 – 3.3	QFN30	4.0	5.0	1.85	65	•		•	•					•
EP53F8QI	1.5	2.4 – 5.5	0.60 – Note 1	QFN16	3.0	3.0	1.1	40	•		•						
EN5319QI	1.5	2.4 – 5.5	0.60 – Note 1	QFN24	4.0	6.0	1.1	55	•		•						
EN5329QI	2.0	2.4 – 5.5	0.60 – Note 1	QFN24	4.0	6.0	1.1	55	•		•						
EN5339QI	3.0	2.4 – 5.5	0.60 – Note 1	QFN24	4.0	6.0	1.1	55	•		•						
EN6337QI	3.0	2.5 – 6.6	0.75 – Note 1	QFN38	4.0	7.0	1.85	75	•		•	•		•			•
EN6347QI	4.0	2.5 – 6.6	0.75 – Note 1	QFN38	4.0	7.0	1.85	75	•		•	•		•			•
EN2342QI	4.0	4.5 – 14.0	0.75 – 5.0	QFN68	8.0	11.0	3.0	200	•		•	•		•	•		
EN5364QI	6.0	2.4 – 6.6	0.60 – Note 1	QFN68	8.0	11.0	1.85	160	•		•	•	•	•	•	•	
EN5367QI	6.0	2.5 – 5.5	0.60 – Note 1	QFN54	10.0	5.5	3.0	160	•		•	•		•		•	
EN6360QI	8.0	2.5 – 6.6	0.60 – Note 1	QFN68	8.0	11.0	3.0	190	•		•	•		•	•	•	•
EN5394QI	9.0	2.4 – 6.6	0.60 – Note 1	QFN68	8.0	11.0	1.85	190	•		•	•	•	•	•	•	
EN63A0QI	12.0	2.5 – 6.6	0.60 – Note 1	QFN76	10.0	11.0	3.0	225	•		•	•		•	•	•	•
EM1130P01QI	30.0	4.5 – 14.5	0.70 – 3.3	QFN120	11.0	17.0	5.0	500	•	PMBus	•	•	•	•	•	•	

Notes:

1. Maximum $V_{OUT} = V_{IN} - V_{DROPOUT}$ where $V_{DROPOUT} = R_{DROPOUT}$ x Load Current. Reference device datasheet to calculate $V_{DROPOUT}$. Typical $V_{DROPOUT} = 0.4$ V.
2. [x] = "8" for PWM only; "7" for Light Load Mode.
3. Size estimate for single-sided PCB including all suggested external components. Smaller size may be possible with double-sided PCB design.

Definitions:

- Qualified to industrial (I) ambient temperature range: -40 to 85 °C.
- VID: Output voltage programming using Voltage ID code pins.
- Margining: The ability to force V_{OUT} out of regulation by a selectable percentage (via 2 pins).
- Input/Output Sync: The ability to control frequency of the regulator(s) to reduce input/output voltage ripple.

For a complete list of Enpirion power products, please visit **www.altera.com/power.**

Featured Products for FPGA Applications

Altera offers a range of verified power solutions that cover FPGA power requirements.

Max I_{LOAD} (A)	Solution	Description	V_{IN} Range (V)	V_{OUT} Range (V)[1]	Core Power[2]	Low Noise[3]
160	EC7401QI and ET4040QI	4-phase pulse-width modulation (PWM) controller and 40 A powertrain	4.5 – 14	0.6 – 5.0	•	
40	ED8101P0xQI and ET4040QI	Single-phase digital controller with PMBus and 40 A powertrain	4.5 – 14	0.6 – 5.0	•	
40	ED8106N0xQI and ET4040QI	Single-phase digital controller and 40 A powertrain	4.5 – 14	0.6 – 5.0	•	
30	EM1130P01QI	Highly integrated, PMBus-compliant 30 A digital PowerSoC, parallel capability	4.5 – 14.5	0.7 – 3.3	•	
12	EN63A0QI	High-efficiency 12 A PowerSoC, parallel capability	2.5 – 6.6	0.6 – V_{IN} - $V_{DROPOUT}$	•	•
8	EN6360QI	High-efficiency 8 A PowerSoC, parallel capability	2.5 – 6.6	0.6 – V_{IN} - $V_{DROPOUT}$	•	•
6	EN5367QI	6 A PowerSoC	2.5 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
4	EN2342QI	4 A PowerSoC, pin compatible with EN2360QI	4.5 – 14	0.75 – 5.0	•	•
4	EN6347QI	High-efficiency 4 A PowerSoC	2.5 – 6.6	0.75 – V_{IN} - $V_{DROPOUT}$	•	•
3	EN6337QI	High-efficiency 3 A PowerSoC	2.5 – 6.6	0.75 – V_{IN} - $V_{DROPOUT}$	•	•
3	EN5339QI	3 A PowerSoC; pin compatible with EN5329/19QI	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
2	ER2120QI	2 A switching regulator with integrated MOSFETs	5.0 – 14	0.6 – 12	•	
2	EN5329QI	2 A PowerSoC; pin compatible with EN5339/19QI	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
1.5	EN5319QI	1.5 A PowerSoC; pin compatible with EN5339/29QI	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
1	ER3110DI	1 A switching regulator with integrated MOSFETs	3.0 – 36	0.6 – 12	•	
1	EN6310QI	High-efficiency 1 A PowerSoC	2.7 – 5.5	0.6 – 3.3	•	•
1	EP53A8xQI	Ultra small 1A PowerSoC	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
1	EY1501DI	1 A linear regulator	2.2 – 6	0.8 – 5	•	•
0.6	EP5358xQI	Ultra small 0.6 A PowerSoC	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
0.5	ER3105QI	0.5 A switching regulator with integrated MOSFETs	3.0 – 36	0.6 – 34	•	
0.15	EY1603TI	150 mA low IQ linear regulator	6.0 – 40	2.5 – 12	•	•
0.05	EY1602SI	50 mA low IQ linear regulator	6.0 – 40	2.5 – 12	•	•

Special Function Products	
Product	**Description**
ES1010QI	12 V power distribution hot swap controller
ES1030QI	Four-channel power rail sequencer

Notes:
1. Reference device datasheet for $V_{DROPOUT}$ value.
2. Meets accuracy, ripple, and transient requirements for FPGA core rails.
3. Low-output voltage ripple and meets CISPR 22 Class B emissions standard.

Quartus II Design Software

www.altera.com/products/software

The Quartus II software is number one in performance and productivity for FPGA, CPLD, and SoC designs, providing the fastest path to convert your concept into reality. The Quartus II software also supports many third-party tools for synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

	Quartus II Software Design Flow		
	Quartus II Software Key Features	Availability	
		Subscription Edition	Web Edition (Free)
Design Entry	Cyclone FPGA and MAX device support	✓	✓
	Arria and Stratix device support	✓	✓[1]
	Cyclone and Arria SoC support	✓	✓
	Multiprocessor support (faster compile time support)	✓	✓[2]
	IP Base Suite (includes licenses for 9 popular IP cores)	✓	Available for purchase
	Qsys (next-generation system-integration tool)	✓	✓
	Rapid Recompile (faster compile for small design changes)	✓	
	Incremental compile (performance preservation and team-based design)	✓	
Functional Simulation	ModelSim®-Altera Starter Edition software	✓	✓
	ModelSim-Altera Edition software	✓[3]	✓[3]
Synthesis	Quartus II Integrated Synthesis (synthesis tool)	✓	✓
Placement and Routing	Fitter (placement and routing tool)	✓	✓
Timing and Power Verification	TimeQuest tool (static timing analysis)	✓	✓
	PowerPlay tool and optimization (power analysis)	✓	✓
In-System Debug	SignalTap™ II Logic Analyzer (embedded logic analyzer)[2]	✓	✓[2]
	Transceiver toolkit (transceiver interface and verification tool)	✓	
	Transceiver Configuration Console (dynamically programmed transceiver settings)	✓	
	Operating System (OS) Support	Availability	
		Subscription Edition	Web Edition (Free)
	Windows/Linux 64 bit support	✓	✓

Notes:
1. The only Arria II FPGA supported is the EP2AGX45 device.
2. Available with TalkBack feature enabled.
3. Requires an additional license.

Quartus II Design Software

	Quartus II Design Software Features Summary	
Design Flow Methodology	Incremental compilation[1]	Improves design timing closure and reduces design compilation times up to 70 percent. Supports team-based design.
	Pin planner	Eases the process of assigning and managing pin assignments for high-density and high-pin-count designs.
	Qsys (replaces SOPC Builder)	Automates system development by integrating IP functions and subsystems (collection of IP functions) using a hierarchical approach and a high-performance interconnect based on a network-on-a-chip architecture.
	Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Altera and from Altera's third-party IP partners.
	Parallel development in ASICs[1]	Allows for FPGA prototypes to be designed in parallel using the same design software and IP.
	Scripting support	Supports command-line operation and Tcl scripting, as well as graphical user interface (GUI) design.
	Rapid Recompile[1]	Maximizes your productivity by reducing your compilation time by 50 percent on average (for a small design change after a full compile). Improves design timing preservation.
Performance and Timing Closure Methodology	Physical synthesis	Uses post placement and routing delay knowledge of a design to improve performance.
	Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Quartus II software settings to find optimal results.
	Extensive cross-probing	Provides support for cross-probing between verification tools and design source files.
	Optimization advisors	Provides design-specific advice to improve performance, resource usage, and power consumption.
	Chip planner	Reduces verification time while maintaining timing closure by enabling small, post placement and routing design changes to be implemented in minutes.
Verification	TimeQuest timing analyzer	Provides native Synopsys® Design Constraint (SDC) support and allows you to create, manage, and analyze complex timing constraints and quickly perform advanced timing verification.
	SignalTap II embedded logic analyzer[2]	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
	System Console	Enables you to easily debug your FPGA in real time using read and write transactions. It also enables you to quickly create a GUI to help monitor and send data into your FPGA.
	PowerPlay technology	Enables you to analyze and optimize both dynamic and static power consumption accurately.
Third-Party Support	EDA partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification. To see a complete list of partners, visit www.altera.com/eda-partners.

Notes:
1. Included in Subscription Edition only.
2. Available with Talkback feature enabled in Web Edition.

Getting Started Steps

Step 1: Download the free Web Edition

www.altera.com/download

Step 2: Get oriented with the Quartus II software interactive tutorial

After installation, open the interactive tutorial on the welcome screen.

Step 3: Sign up for training

www.altera.com/training

Quartus II Design Software

Purchase Quartus II software and increase your productivity today.

Pricing	Description
$2,995 (SW-QUARTUS-SE-FIX) Renewal $2,495 (SWR-QUARTUS-SE-FIX)	Fixed-node license: subscription for one year—Windows only.
$3,995 (SW-QUARTUS-SE-FLT) Renewal $2,495 (SWR-QUARTUS-SE-FLT) Add seat $3,995 (SW-QUARTUS-SE-ADD)	Floating-node license: subscription for one year—Windows/Linux.

ModelSim-Altera Edition Software	
$945 (SW-MODELSIM-AE) Renewal $945 (SWR-MODELSIM-AE)	ModelSim-Altera Edition software is available as a $945 option for both Quartus II Subscription Edition and Web Edition software. It is 33 percent faster than Starter Edition with no line limitation.
ModelSim-Altera Starter Edition Software	
Free	Free for both Quartus II Subscription Edition and Web Edition software with a 10,000 executable line limitation. ModelSim-Altera Starter Edition software is recommended for simulating small FPGA designs.

Altera SDK for OpenCL

www.altera.com/opencl

The Altera SDK for OpenCL[1] allows you to implement applications in FPGAs easily by abstracting away the complexities of FPGA design. Software programmers can write hardware-accelerated kernel functions in OpenCL C, an ANSI C-based language with additional OpenCL constructs to extract parallelism. Using the FPGA as an accelerator provides significant advantages over using a CPU or GPU: with an FPGA, you use customized small scalar or large vector processing units or a deep hardware pipeline to create a completely custom accelerator at the lowest possible power.

Altera SDK for OpenCL Software Features Summary	
Altera Offline Compiler (AOC)	• GCC-based model compiler of OpenCL kernel code
Altera OpenCL Utility (AOCL)	• Diagnostics for board installation • Flash or program FPGA image • Install board drivers (typically PCIe)
Altera SDK for OpenCL Licensing	• Purchase a one-year perpetual license ($995)[2] • Purchase a one-year renewal license ($895) • Fixed-node and floating-node licenses available • 60-day evaluation license available on request
Operating System	• Microsoft 64 bit Windows 7 • Red Hat Enterprise 64 bit Linux (RHEL) 6.x
Memory Requirements	• Computer equipped with at least 16 GB RAM

Notes:

1. Product is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at **www.khronos.org/conformance.**
2. The OpenCL license allows you to use the Quartus II software from the OpenCL software but with restricted functionality. The full Quartus II Subscription Edition license is required to access the full functionality of the Quartus II software.

SoC Embedded Design Suite

www.altera.com/soc-eds

The Altera SoC Embedded Design Suite (EDS) is a comprehensive tool suite for embedded software development on Altera SoCs. It comprises development tools, utility programs, and design examples to jump-start firmware and application software development. The SoC EDS includes an exclusive offering of the ARM DS-5 Altera Edition Toolkit.

	SoC Embedded Design Suite		
	SoC EDS Key Features	Availability	
		Web Edition (Free)	Subscription Edition
DS-5 Altera Edition Features	Linux application debugging over Ethernet	✓	✓
	Debugging over USB-Blaster™ II cable · Board bring-up · Device driver development · Operating system (OS) porting · Bare-metal programming · ARM CoreSight trace support		✓
	Debugging over DSTREAM · Board bring-up · Device driver development · Operating system (OS) porting · Bare-metal programming · ARM CoreSight trace support		✓
	FPGA-adaptive debugging · Auto peripheral register discovery · Cross-triggering between CPU and FPGA domains · ARM CoreSight trace supportvc · Access to System Trace Module (STM) events		✓
	Streamline Performance Analyzer support	Limited	✓
Compiler Tools	Linaro Compiler	✓	✓
	Sourcery CodeBench Lite ARM EABI GCC		✓
	ARM Compiler 5		✓
Libraries	Hardware API	✓	✓
Other Tools	Quartus II Programmer	✓	✓
	SignalTap II Logic Analyzer	✓	✓
	Altera Boot Disk Utility	✓	✓
	Device Tree Generator	✓	✓
Design Examples	Golden system reference designs for SoC development kits	✓	✓
	Device-wide asymmetric multiprocessing	✓	✓
	Triple Speed Ethernet (TSE) with Modular Scatter-Gather Direct Memory Access (mSG-DMA)	✓	✓
	PCIe Root Port with Message Signal Interrupts (MSI)	✓	✓
Host OS Support	Windows 7 64 bit	✓	✓
	Windows 7 32 bit	Not supported	Not supported
	Red Hat Linux 5/6 64 bit	32 bit libraries are required	32 bit libraries are required
SoC Embedded Design Suite	Pricing	Free	$995 for Standalone License. Included free with Altera SoC FPGA Development Kits.

Nios II Processor Embedded Design Suite

Altera's Nios II processor, the world's most versatile processor according to Gartner Research, is the most widely used soft processor in the FPGA industry. This soft processor delivers unprecedented flexibility for your cost-sensitive, real-time, safety-critical (DO-254), and applications processing needs. All Altera FPGA families support the Nios II processor.

Nios II EDS Contents
Nios II Software Build Tools for Eclipse (Nios II SBT for Eclipse), for software development · Based on Eclipse IDE · New project wizards · Software templates · Source navigator and editor
Compiler for C and C++ (GNU)
Software Debugger/Profiler
Flash Programmer
Embedded Software · Hardware Abstration Layer (HAL) · MicroC/OS-II RTOS · NicheStack TCP/IP Network Stack—Nios II Edition · Newlib ANSI-C standard library · Simple file system
Other Altera Command-Line Tools and Utilities
Design Examples

Hardware Development Tools

- Quartus II design software
- Qsys system integration tool
- SignalTap II embedded logic analyzer plug-in for Nios II processor
- System Console for low-level debugging of Qsys systems

Licensing

Getting started with the Nios II processor is now easier than ever. Not only is the Nios II EDS free, but the Nios II economy core IP is also free.

Licenses for the Nios II standard and fast core IP are available for stand-alone IP (IP-NIOS) or as part of the Embedded IP Suite (IPS-EMBEDDED). These royalty-free licenses never expire and allow you to target your processor design to any Altera FPGA. The Embedded IP Suite is a value bundle that contains licenses of the Nios II processor IP core, DDR1/2/3 Memory Controller IP cores, Triple-Speed Ethernet MAC IP core and 16550 - compatible UART IOP core. Both Nios II Classic and Gen2 processors are included in these licenses.

Development Kits

Go to **page 67** for information about embedded development kits.

Nios II EDS: What You Get for Free!

The Nios II Embedded Design Suite (EDS) provides all the tools and software you need to develop code for the Nios II processor and Nios II Gen2 processors.

With the Nios II EDS you can:

- **Develop software with Nios II SBT for Eclipse:** Based on industry-standard Eclipse, the Nios II SBT is an integrated development environment for editing, compiling, debugging software code, and flash programming.
- **Manage board support packages (BSPs):** The Nios II EDS makes managing your BSP easier than ever. Nios II EDS automatically adds device drivers for Altera-provided IP to your BSP. The BSP Editor provides full control over your build options.
- **Get a free software network stack:** The Nios II EDS includes NicheStack TCP/IP Network Stack - Nios II Edition—a commercial-grade network stack software—for free.
- **Evaluate a RTOS:** The Nios II EDS contains an evaluation version of the popular Micrium MicroC/OS-II RTOS. Product licenses are sold separately by Micrium.

Join the Nios II Community!

Be one of the thousands of Nios II developers who visit the Altera Wiki, Altera Forum, and the Rocketboards.org website. Altera Wiki and the Rocketboards.org website have hundreds of design examples and design tips from Nios II developers all over the world. Join ongoing discussions on the Nios II section of the Altera Forum to learn more about Linux, hardware, and software development for the Nios II processor.

Visit the following websites:

www.alterawiki.com

www.alteraforum.com

www.rocketboards.org

SoC Operating System Support

Altera and our ecosystem partners offer comprehensive operating system support for Altera SoC development boards.

Operating System	Company	Source
Abassi	Code Time Technologies	Code Time
Android	Fujisoft	Fujisoft
AUTOSAR MCAL	Altera	Altera
Carrier Grade Edition 7 (CGE7)	MontaVista	MontaVista
DEOS	DDC-I	DDC-I
eCosPro	eCosCentric	eCosCentric
eT-Kernel	eSOL	eSOL
FreeRTOS	FreeRTOS.org	FreeRTOS.org
INTEGRITY	Green Hills Software	Green Hills Software
Linux	Open Source	www.rocketboards.org
Nucleus	Mentor Graphics	Mentor Graphics
OSE	Enea	Enea
QNX Neutrino	QNX	QNX
RTEMS	RTEMS.org	RTEMS.org
ThreadX	Express Logic	Express Logic
uC/OS-II, uC/OS-III	Micrium	Micriμm
uC3 (Japanese)	eForce	eForce
VxWorks	Wind River	Wind River
Wind River Linux	Wind River	Wind River
Windows Embedded Compact 7	Microsoft	Adeneo Embedded

More Information

For the latest on OS support for Altera SoCs, visit **www.altera.com/products/soc/ecosystem.html**

Nios II Processor Operating System Support

Altera and our ecosystem partners offer comprehensive operating system support for the Nios II processor.

OS	Availability
ChibiOS/RT	Now through www.emb4fun.com
eCos	Now through www.ecoscentric.com
eCos (Zylin)	Now through www.opensource.zylin.com
embOS	Now through www.segger.com
EUROS	Now through www.euros-embedded.com
FreeRTOS	Now through www.freertos.org
Linux	Now through www.windriver.com
Linux	Now through www.rocketboards.org
oSCAN	Now through www.vector.com
TargetOS	Now through www. blunkmicro.com
ThreadX	Now through www.threadx.com
Toppers	Now through www.toppers.jp
µC/OS-II, µC/OS-III	Now through www.micrium.com

Summary of Nios II Soft Processors			
Category	**Processor**	**Vendor**	**Description**
Power- and cost-optimized processing	Nios II economy core	Altera	With unique, real-time hardware features such as custom instructions, ability to use FPGA hardware to accelerate a function, vectored interrupt controller, and tightly coupled memory, as well as support for industry-leading RTOSs, the Nios II processor meets both your hard and soft real-time requirements, and offers a versatile solution for real-time processing.
Real-time processing	Nios II standard and fast core[1]	Altera	
Applications processing	Nios II fast core	Altera	A simple configuration option adds a memory management unit to the Nios II fast processor core to support embedded Linux. Both open-source and commercially supported versions of Linux for Nios II processors are available.
Safety-critical processing	Nios II SC	HCELL	Certify your design for DO-254 compliance by using the Nios II Safety Critical core along with the DO-254 compliance design services offered by HCELL.

Notes:
1. With the Nios II Gen2 product the standard core is not available as a pre-configured option, however the Gen2 fast core can be configured in Qsys to have the same feature set as the standard core.

Getting Started

To learn more about Altera's portfolio of customizable processors and how you can get started, visit **www.altera.com/nios.**

Nios II Processor

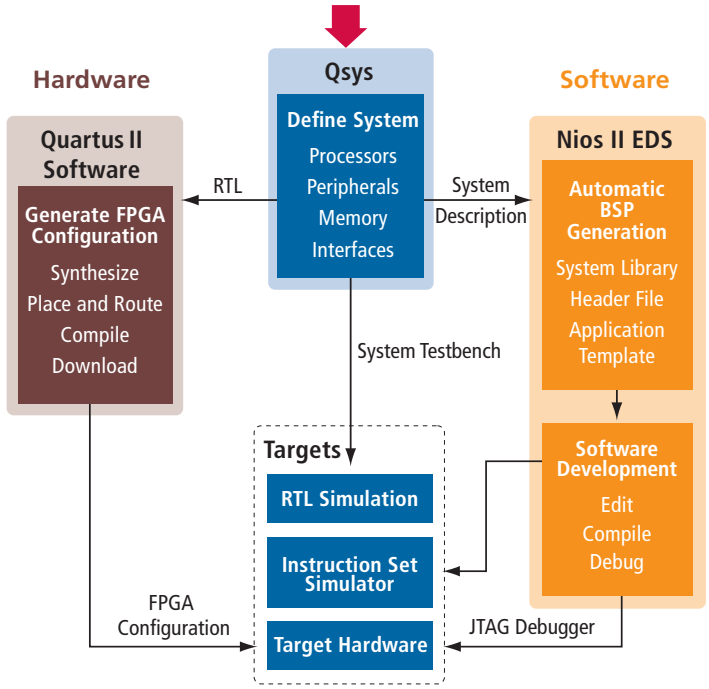
In any of Altera's FPGAs, the Nios II Classic and Nios II Gen2 processors offer a custom system solution that has the flexibility of software and the performance of hardware. Through its innovative design, the Nios II processor leverages the logic resources of the device to provide unprecedented hard and soft real-time capabilities.

You can also use the Nios II processor together with the ARM processor in Altera SoCs to create effective multi-processor systems.

With the Nios II processor you can:

- Lower overall system cost and complexity by integrating external processors into the FPGA.
- Scale performance with multiple processors, custom instructions (hardware acceleration of a software function), or co-processor modules (hardware accelerator next to the soft processor).
- Target any Stratix, Arria, Cyclone, MAX 10 FPGA, or the FPGA portion of the Arria V or Cyclone V SoCs.
- Eliminate the risk of processor and ASSP device obsolescence.
- Take advantage of the free Nios II economy core, the free Nios II Embedded Design Suite (EDS), and the free NicheStack TCP/IP Network Stack - Nios II Edition software to get started today.

Nios II Processor Development Flow



Nios II Classic and Gen2 Processors

Nios II Gen2 processors are binary compatible improved versions of the Nios II Classic cores. Improvements include optional 32 bit address range, full ECC support, peripheral memory address region, and improved performance on some arithmetic instructions.

Altera's Customizable Processor Portfolio

Performance and Feature Set Summary of Key Processors Supported on Altera Devices					
Category	**Cost- and Power-Sensitive Processors**	**Real-Time Processor**		**Applications Processors**	
Features	**Nios II Economy**	**Nios II Standard**	**Nios II Fast**	**28 nm[1] Dual-Core ARM Cortex-A9**	**20 nm[2] Dual-Core ARM Cortex-A9**
Maximum frequency (MHz)[3]	370 (Stratix V)	300 (Stratix V)	350 (Stratix V)	925 MHz (Cyclone V SoC) 1.05 GHz (Arria V SoC)	1.5 GHz (Arria 10 -1 speed grade)
Maximum performance (MIPS[4] at MHz) Stratix series	56 (at 370 MHz)	192 (at 300 MHz)	396 (at 350 MHz)	–	–
Maximum performance (MIPS[4] at MHz) Arria series	38 (at 250 MHz)	115 (at 180 MHz)	203 (at 180 MHz)	2,625 MIPS per core at 1.05 GHz	3,750 MIPS per core at 1.5 GHz
Maximum performance (MIPS[4] at MHz) Cyclone series	32 (at 210 MHz)	96 (at 150 MHz)	203 (at 180 MHz)	2,313 MIPS per core at 925 MHz	–
Maximum performance efficiency (MIPS[4] per MHz)	0.15	0.64	1.13	2.5	2.5
16/32 bit instruction set support	32	32	32	16 and 32	16 and 32
Level 1 instruction cache	–	Configurable	Configurable	32 KB	32 KB
Level 1 data cache	–	–	Configurable	32 KB	32 KB
Level 2 cache	–	–	–	512 KB	512 KB
Memory management unit	–	–	Configurable	✓	✓
Floating-point unit	–	FPCI[5]	FPCI[5]	Dual precision	Dual precision
Vectored interrupt controller	–	✓	✓	–	–
Tightly coupled memory	–	Configurable	Configurable	–	–
Custom instruction interface	Up to 256	Up to 256	Up to 256	–	–
Equivalent LEs	600	1,200	1,800 – 3,200	HPS	HPS

Notes:
1. Altera 28 nm SoCs comprise Cyclone V SoCs and Arria V SoCs.
2. Altera 20 nm SoCs comprise Arria 10 SoCs.
3. Maximum performance measurements measured on Stratix V FPGAs.
4. Dhrystone 2.1 benchmark.
5. Floating-point custom instructions.

Altera and Partner Functions

www.altera.com/ip

For a complete list of IP functions from Altera and its partners, please visit www.altera.com/ip.

	Product Name	Vendor Name
DSP	**Arithmetic**	
	Floating Point Megafunctions	Altera
	Floating Point Arithmetic Co-Processor	Digital Core Design
	Floating Point Mathematics Unit	Digital Core Design
	Floating Point Pipelined Multiplier Unit	Digital Core Design
	Error Detection/Correction	
	Reed-Solomon Encoder/Decoder II[1]	Altera
	Viterbi Compiler, High-Speed Parallel Decoder	Altera
	Viterbi Compiler, Low-Speed/ Hybrid Serial Decoder	Altera
	Turbo Convolutional Decoder	TurboConcept
	WiMAX CTC Decoder	TurboConcept
	3GPP/LTE CTC Decoder	TurboConcept
	Turbo Product Code Decoder	TurboConcept
	Filters and Transforms	
	Fast Fourier Transform (FFT)/ Inverse FFT (IFFT)	Altera
	Cascaded Integrator Comb (CIC) Compiler	Altera
	Finite Impulse Response (FIR) Compiler II	Altera
	Modulation/Demodulation	
	Numerically Controlled Oscillator Compiler	Altera
	ATSC and Multi-Channel ATSC 8-VSB Modulators	Commsonic
	DVB-T Modulator	Commsonic
	DVB-S2 Modulator	Commsonic
	Multi-Channel Cable (QAM) Modulator	Commsonic

	Product Name	Vendor Name
DSP (Continued)	**Video and Image Processing**	
	Video and Image Processing Suite[1]	Altera
	JPEG Decoder and Encoder	Barco Silex
	JPEG 2000 Sub-Frame Latency Encoder and Decoder	Barco Silex
	Multi-Channel JPEG 2000 Encoder and Decoder Cores	Barco Silex
	JPEG CODEC	CAST, Inc.
	JPEG Encoders and Decoders	CAST, Inc.
	Lossless JPEG Encoder and Decoder	CAST, Inc.
	JPEG 2000 Encoder	CAST, Inc.
	JPEG Extended Encoder	CAST, Inc.
	H.264 AVC High Profile and Main Profile Video Encoders	CAST, Inc.
	H.264 Encoders	Jointwave Group LLC
	H.264 Baseline Profile Video Encoder	CAST, Inc.
	Video Processor and Deinterlacer with Line-Doubled Output	Crucial IP, Inc.
	Video Rotation Function	Crucial IP, Inc.
	Video Scaler with Shrink and Zoom Support	Crucial IP, Inc.
	Video Scaler with Up Converstion to 4K	Crucial IP, Inc.
	Additional Functions	
	Multi-Purpose Advanced Encryption Standard (AES) Crypto Engine	Barco Silex
	DES/3DES Encoder/Decoder	Barco Silex
	Hashing IP Core	Barco Silex
	Public Key Crypto Engine	Barco Silex
	SHA-1	CAST, Inc.
	SHA-256	CAST, Inc.
	AES CODECs	CAST, Inc.

Notes:
1. Qsys-compliant licensed core.

Altera and Partner Functions

	Product Name	Vendor Name
Embedded Processors	**32 bit/16 bit**	
	Nios II (Classic/Gen2) Embedded Processors[1]	Altera
	ARM Cortex-A9 MPCore Processor	Altera
	Hard IP in SoCs	Altera
	ARM Cortex-M1[1]	ARM
	BA22 32 bit Deeply Embedded Processor	CAST, Inc.
	BA22 32 bit Embedded Processor	CAST, Inc.
	V1 ColdFire[1]	Freescale
	8 bit	
	R8051XC2 Microcontroller	CAST, Inc.
	DP8051 Pipelined High-Performance 8 bit Microcontroller	Digital Core Design
	DP8051XP Pipelined, High-Performance 8 bit Microcontroller	Digital Core Design
	DF6811E 8 bit Fast Microcontroller	Digital Core Design
	DFPIC1655X 8 bit RISC Microcontroller	Digital Core Design
Interface and Protocols	**Communication**	
	Optical Transport Network (OTN) Framers/Deframers	Altera
	SFI-5.1	Altera
	SONET/Synchronous Digital Hierarchy (SDH) Framer/Deframer	Aliathon
	SONET/SDH Mapper/Demapper	Aliathon
	SDN CodeChips	Arrive Technologies
	SONET/SDH CodeChips	Arrive Technologies
	Ethernet	
	10 Gbps Ethernet Media Access Controller (MAC)[1] with 1588	Altera
	Triple-Speed Ethernet (10/100/1000 Mbps) MAC and PHY[1] with 1588	Altera
	10GBASE-R PHY	Altera
	10G Base-X (XAUI) PHY	Altera
	40G Ethernet MAC and PHY with 1588	Altera

	Product Name	Vendor Name
Interface and Protocols (Continued)	**Ethernet (Continued)**	
	100G Ethernet MAC and PHY with 1588	Altera
	10GBASE-KR PHY	Altera
	1G/10Gb Ethernet PHY	Altera
	Carrier Ethernet CodeChips	Arrive Technologies
	Pseudowire CodeChips	Arrive Technologies
	Gigabit Ethernet MAC[1]	IFI
	High-Performance Gigabit Ethernet MAC[1]	IFI
	10G RTP Video over IP	Macnica Americas
	10G MAC Lite	Macnica Americas
	10/100/1000 Ethernet MAC with SGMII	MorethanIP
	10 Gigabit Ethernet MAC and Physical Coding Sub-Layer (PCS) MAC and PCS	MorethanIP
	10 Gigabit Reduced XAUI PCS Core	MorethanIP
	SPAUI MAC Core	MorethanIP
	20 Gigabit DXAUI PCS Core	MorethanIP
	QSGMII PCS Core	MorethanIP
	2.5 Gbps Ethernet MAC	MorethanIP
	High Speed	
	RapidIO®[1] Gen1, Gen2	Altera
	RapidIO Gen3	Mobiveil
	Common Public Radio Interface (CPRI)	Altera
	Interlaken	Altera
	Interlaken Look-Aside	Altera
	SerialLite II/III	Altera
	SATA 1.0/SATA 2.0	Intelliprop, Inc.
	QuickPath Interconnect (QPI)	Intel Corporation
	RapidIO Controller	Mobiveil, Inc.
	RapidIO to AXI Bridge Controller	Mobiveil, Inc.
	Infiniband Link Layer and Target Channel Adapter Cores	Polybus
	HyperTransport™ 3.0	University of Heidelberg

Notes:
1. Qsys-compliant licensed core.

Altera and Partner Functions

	Product Name	Vendor Name
Interface and Protocols (Continued)	**PCI**	
	PCIe Gen1 x1[1], x4[1], x8 Controller (Soft IP)	Altera
	PCIe Gen1, Gen2, Gen3 Core x1, x2, x4, and x8 (Hardened IP)	Altera
	PCIe Endpoint Controller x1, x4	CAST, Inc.
	PCIe x8 Endpoint Controller	CAST, Inc.
	PCI 32/64 bit PCI Master Target 33/66 MHz Controllers	CAST, Inc.
	PCI Multifunction Master/ Target Interface	CAST, Inc.
	PCIe Express Cores	Northwest Logic, Inc.
	PCI Express Multiport Transparent Switch	Mobiveil, Inc.
	PCI Express Hybrid Controller	Mobiveil, Inc.
	PCI Express to AXI Bridge Controller	Mobiveil, Inc.
	PCI-X Core	Northwest Logic, Inc.
	PCI Core	Northwest Logic, Inc.
	XpressRICH3 PCIe, Gen1, Gen2, and Gen3	ReFLEX CES
	PCI and PCI-X Master/ Target Cores 32/64 bit	ReFLEX CES
	Serial	
	Serial Peripheral Interface (SPI)/ Avalon® Master Bridge[2]	Altera
	UART[2]	Altera
	JTAG UART[2]	Altera
	16550 UART	Altera

	Product Name	Vendor Name
Interface and Protocols (Continued)	**Serial (Continued)**	
	JTAG/Avalon Master Bridge[2]	Altera
	C_CAN[1]	Bosch
	CAN 2.0/FD [1]	CAST, Inc.
	Local Interconnect Network (LIN) Controller	CAST, Inc.
	SPI Master/Slave	CAST, Inc.
	H16450S UART	CAST, Inc.
	H16550S UART	CAST, Inc.
	H16750S UART	CAST, Inc.
	MD5 Message-Digest	CAST, Inc.
	Smart Card Reader	CAST, Inc.
	DI2CM I^2C Bus Interface-Master	Digital Core Design
	DI2CSB I^2C Bus Interface-Slave	Digital Core Design
	D16550 UART with 16-Byte FIFO	Digital Core Design
	DSPI Serial Peripheral Interface Master/Slave	Digital Core Design
	Secure Digital (SD)/MMC SPI	El Camino GmbH
	Secure Digital I/O (SDIO)/SD Memory/Slave Controller	Eureka Technology, Inc.
	UART	Eureka Technology, Inc.
	SDIO/SD Memory/ MMC Host Controller	Eureka Technology, Inc.
	Nios II Advanced CAN[1]	IFI
	MediaLB Device Interface[1]	IFI
	I^2C Master/Slave/PIO Controller	Microtronix, Inc.

Notes:

1. Qsys-compliant licensed core.
2. Qsys component (no license required).

Altera and Partner Functions

	Product Name	Vendor Name
Interface and Protocols (Continued)	I²C Master and Slave	SLS
	PS2 Interface	SLS
	USB High-Speed Function Controller[1]	SLS
	USB Full-/Low-Speed Function Controller[1]	SLS
	SD Host Controller[1]	SLS
	USB 3.0 SuperSpeed Device Controller	SLS
	Audio and Video	
	Character LCD[2]	Altera
	Pixel Converter (BGR0 to BGR)[2]	Altera
	Video Sync Generator[2]	Altera
	SD/HD/3G-HD Serial Digital Interface (SDI)	Altera
	DisplayPort	Altera
	HDMI	Altera
	DisplayPort	Bitec
	V-by-One HS	Bitec
	Video LVDS Serializer/Deserializer (SERDES) Transmitter/Receiver	Microtronic, Inc
	I2S Audio CODEC[1]	SLS
Memories and Memory Controllers	**DMA**	
	Scatter-Gather DMA Controller[2]	Altera
	DMA Controller[2]	Altera
	Flash	
	CompactFlash (True IDE)[2]	Altera
	EPCS Serial Flash Controller[2]	Altera
	Flash Memory[2]	Altera
	NAND Flash Controller	Eureka Technology, Inc.
	ISA/PC Card/PCMCIA/ CompactFlash Host Adapter	Eureka Technology, Inc.
	Universal NVM Express Controller (UNEX)	Mobiveil, Inc.
	ONFI Controller	SLS
	CompactFlash Interface[1]	SLS

	Product Name	Vendor Name
Memories and Memory Controllers (Continued)	**SDRAM**	
	DDR/DDR2 and DDR3/DDR4 SDRAM Controllers[1]	Altera
	LPDDR2 SDRAM Controller	Altera
	RLDRAM 2 Controller	Altera
	Streaming Multi-Port SDRAM Memory Controller	Microtronix, Inc.
	HyperDrive Multi-Port DDR2 Memory Controller	Microtronix, Inc.
	Avalon Multi-Port SDRAM Memory Controller[1]	Microtronix, Inc.
	DDR and DDR2 SDRAM Controllers	Northwest Logic, Inc.
	RLDRAM II and III Controllers	Northwest Logic, Inc.
	Mobile DDR SDRAM Controller	Northwest Logic, Inc.
	Mobile SDR SDRAM Controller	Northwest Logic, Inc.
	SDR SDRAM Controller	Northwest Logic, Inc.
	LPDDR2/3 Controllers	Northwest Logic, Inc.
	SRAM	
	SSRAM (Cypress CY7C1380C)[2]	Altera
	QDR II/II+/II+Xtreme/IV SRAM Controller	Altera

Notes:

1. Qsys-compliant licensed core.
2. Qsys component (no license required).

Transceiver Protocols

www.altera.com/datarates

Altera device transceivers support the protocols listed in the following table. For details about the data rates, please visit **www.altera.com/datarates.**

Protocols/ Interface Standards	Supported Devices															
	Stratix Series FPGAs						Arria Series FPGAs							Cyclone Series FPGAs		
	10 GX/SX	V GX/GS	V GT	IV GX	IV GT	II GX	10 GX/SX	10 GT	V GX	V GT/ST	V GZ	II GX	II GZ	V GX/SX	V GT/ST	IV GX
Basic (proprietary)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CEI-6G-SR/LR	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
CEI-11G-SR	✓	✓	✓	–	✓	–	✓	✓	–	–	–	–	–	–	–	–
CEI-28G-VSR	✓	–	✓	–	–	–	–	✓	–	–	–	–	–	–	–	–
SFP+/SFF-8431	✓	✓	✓	–	✓	–	✓	✓	–	–	✓	–	–	–	–	–
XFI	✓	✓	✓	–	✓	–	✓	✓	–	✓	–	–	–	–	–	–
XFP	✓	✓	✓	–	–	–	✓	✓	–	–	✓	–	–	–	–	–
1000BASE-X (GbE)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
10GBASE-R	✓	✓	✓	–	✓	–	✓	✓	–	✓	✓	–	–	–	–	–
10GBASE-KR	✓	✓	✓	–	–	–	✓	✓	–	–	✓	–	–	–	–	–
ASI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	✓	✓	–	–	–
CPRI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CAUI/XLAUI	✓	✓	✓	–	✓	–	✓	✓	–	–	✓	–	–	–	–	–
CAUI-4	✓	–	✓	–	–	–	–	✓	–	–	–	–	–	–	–	–
DisplayPort	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	✓	✓	✓
Fibre Channel	✓	✓	✓	✓	✓	✓	✓	✓	–	✓	✓	–	–	–	–	–
GPON	✓	✓	✓	✓	✓	–	✓	✓	✓	✓	✓	✓	✓	–	–	–
G.709 OTU-2	✓	✓	✓	–	✓	–	✓	✓	✓	✓	–	–	–	✓	✓	✓
OTN with FEC	✓	✓	✓	–	✓	–	✓	✓	–	–	–	–	–	–	–	–
HiGig	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–
High-Definition Multimedia Interface (HDMI)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Transceiver Protocols

Protocols	Supported Devices															
	Stratix Series FPGAs						Arria Series FPGAs							Cyclone Series FPGAs		
	10 GX/SX	V GX/GS	V GT	IV GX	IV GT	II GX	10 GX/SX	10 GT	V GX	V GT/ST	V GZ	II GX	II GZ	V GX/SX	V GT/ST	IV GX
JESD204 A/B	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HMC[1]	✓	–	–	–	–	–	✓	✓	–	–	–	–	–	–	–	–
HyperTransport	✓	✓	✓	✓	✓	–	✓	✓	✓	✓	✓	–	–	–	–	–
InfiniBand	✓	✓	✓	–	–	–	✓	✓	–	–	✓	–	–	–	–	–
Interlaken	✓	✓	✓	✓	✓	–	✓	✓	✓	✓	✓	–	–	–	–	–
Interlaken Look-Aside	✓	✓	✓	–	–	–	✓	✓	✓	✓	✓	–	–	–	–	–
MoSys	✓	✓	–	–	–	–	✓	✓	–	–	–	–	–	–	–	–
OBSAI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI Express	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RXAUI/DXAUI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
SGMII/QSGMII	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
QPI	✓	✓	✓	–	–	–	✓	✓	–	–	✓	–	–	–	–	–
SAS/SATA	✓	✓	✓	✓	✓	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SerialLite II	✓	✓	✓	✓	✓	–	✓	✓	✓	✓	–	✓	✓	–	–	–
SerialLite III	✓	✓	✓	–	–	–	✓	✓	–	–	✓	–	–	–	–	–
SDI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SFI-5.1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
SFI-S/SFI-5.2	✓	✓	✓	–	✓	–	✓	✓	–	–	✓	–	–	–	–	–
RapidIO	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SPAUI	✓	✓	✓	✓	✓	✓	✓	✓	–	–	✓	–	–	–	–	–
SONET/SDH	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–
XAUI (10GBASE-X)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
V-by-One	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–	✓

Notes:

1. Contact Altera for more details on HMC support.

Altera and Partner Development Kits

www.altera.com/devkits

Altera development kits provide a complete, high-quality design environment for engineers. These kits help simplify the design process and reduce time-to-market. Development kits include software, reference designs, cables, and programming hardware.

Altera and partner development kits are listed below. For more details about these development kits or other older development kits that are available, check out our online development kits page at **www.altera.com/devkits**.

Product and Vendor Name	Description
Arria 10 FPGA Kits	
Arria 10 FPGA Development Kit **Altera** NEW	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to an Arria 10 GX FPGA. This kit includes the PCIe x8 form factor, two FMC connectors for expandability, Ethernet, USB, and SDIs. The board includes one connector for plugging in DRAM and SRAM daughtercards. Supported daughtercard formats include DDR4 x72 SDRAM, DDR3 x72 SDRAM, RLDRAM 3 x36, and QDR IV x36 SRAM. This board also includes SMA connectors for transceiver output, clock output, and clock input. Several programmable oscillators are available and other user interfaces include user pushbuttons, dipswitches, bi-color user LEDs, an LCD display, power, and temperature measurement circuitry.
Arria 10 FPGA Signal Integrity Kit **Altera** NEW	This kit enables a thorough evaluation of transceiver signal integrity and device interoperability. Features include five full-duplex 28 Gbps transceiver channels with edge launch connectors, one 14 Gbps backplane connector (from Amphenol), and ten full-duplex 12.5 Gbps transceiver channels with a Samtec Bullseye connector. This board also includes several programmable clock oscillators, user pushbuttons, dipswitches, user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, Ethernet, an embedded USB-Blaster™ II, and JTAG interfaces.
MAX 10 FPGA Kits	
MAX 10 FPGA Development Kit **Altera** NEW	This kit offers a comprehensive general-purpose development platform for many markets and applications, such as industrial and automotive. This fully featured development kit includes a 10M50DAF484C6G device, DDR3 memory, 2X 1 GbE, high-speed mezzanine card (HSMC) connector, quad serial peripheral interface, 16 bit digital-to-analog converter (DAC), flash memory, and 2X Digilent Pmod™ Compatible headers.
MAX 10 FPGA Evaluation Kit **Altera** NEW	The 10M08 evaluation board provides a cost-effective entry point to MAX 10 FPGA design. The card comes complete with an Arduino header socket, which lets you connect a wide variety of daughtercards. Other features include a MAX 10 10M08SAE144C8G device, Arduino shield expansion, access to 80 I/O through-holes, and a prototyping area.
BeMicro Max 10 FPGA Evaluation Kit **Arrow** NEW	The BeMicro Max 10 FPGA evaluation kit is an entry-level kit from Arrow that includes a 10M08DAF484C8G device. The kit retains the 80-pin edge connector interface used on previous BeMicro kits. The BeMicro Max 10 FPGA evaluation kit includes a variety of peripherals, such an accelerometer, DAC, temperature sensor, thermal resistor, photo resistor, LEDs, pushbuttons, and several different options for expansion connectivity, including 2X Digilent Pmod™ Compatible headers and 2X 40-pin prototype headers.
DECA MAX 10 FPGA Evaluation Kit **Arrow** NEW	DECA is a full-featured evaluation kit featuring a 10M50DAF484C6G device. The kit includes a BeagleBone-compatible header for further I/O expansion, a variety of sensors (gesture/humidity/temperature/CMOS), MIPI CSI-2 camera interface, LEDs, pushbuttons, and an on-board USB-Blaster II cable.
Mpression Odyssey MAX 10 FPGA IoT Evaluation Kit **Macnica** NEW	The Macnica MAX 10 FPGA evaluation kit connects and controls your FPGA design via Bluetooth using the Mpression Odyssey Smartphone application. This kit also includes a10M08U169C8G device, SDRAM, Arduino shield expansion capability, and Bluetooth SMART connectivity module.

Altera and Partner Development Kits

Product and Vendor Name	Description
Stratix V FPGA Kits	
Stratix V Advanced Systems Development Kit **Altera**	This kit is a complete systems design environment that includes both the hardware and software needed to begin architecture development and system design using Stratix V FPGAs. The PCIe-based form factor utilizes a x16 edge connector, and includes high memory bandwidth to DDR3, QDR II+, and serial memory. Multiple high-speed protocols are accessible through FMC and HSMC connections.
Stratix V GX FPGA Development Kit **Altera**	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix V GX FPGA. This kit includes the PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, and SDI interfaces. Memory includes one x72 DDR3 SDRAM, one x18 QDR II+ SRAM, and flash memory. This kit also includes two SMA connectors for a differential transceiver output. Several programmable oscillators are available and other user interfaces include three user pushbuttons, eight dipswitches, eight bi-color user LEDs, an LCD display, and power and temperature measurement circuitry.
Transceiver Signal Integrity Development Kit, Stratix V GX Edition **Altera**	This kit enables a thorough evaluation of transceiver signal integrity and device interoperability. Features include seven full-duplex transceiver channels with SMA connectors, two 14G backplane connectors (from Amphenol and Molex), four programmable clock oscillators, four user pushbuttons, eight dipswitches, eight user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, and Ethernet, an embedded USB-Blaster download cable, and JTAG interfaces.
Transceiver Signal Integrity Development Kit, Stratix V GT Edition **Altera**	The Altera Stratix V GT Transceiver Signal Integrity (SI) Development Kit provides a platform for electrical compliance testing and interoperability analysis. The accessibility to multiple channels allows for real-world analysis as implemented in the system with transceiver channels available through SMA and popular backplane connectors. This development kit can be used for evaluation of transceiver link performance up to 28 Gbps, generation and checking pseudo-random binary sequence (PRBS) patterns via an easy-to-use GUI that does not require the Quartus II software, access advanced equalization to fine-tune link settings for optimal bit error ratio (BER), jitter analysis, and verifying physical media attachment (PMA) interoperability with Stratix V GT FPGAs for targeted protocols, such as CEI-25/28G, CEI-11G, PCIe Gen 3.0, 10GBASE-KR, 10 Gigabit Ethernet, XAUI, CEI-6G, Serial RapidIO, HD-SDI, and others. You can use the built-in high speed backplane connectors to evaluate custom backplane performance and evaluate link BER.
100G Development Kit, Stratix V GX Edition **Altera**	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through four x18 QDR II and four x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 11.3 Gbps, and verify PMA compliance to standards, such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCIe (Gen1, Gen2, and Gen3), and other major standards. This kit can also validate interoperability between optical modules, such as small form factor pluggable (SFP), SFP+, quad small form factor pluggable (QSFP), and c form factor pluggable (CFP).
DSP Development Kit, Stratix V Edition **Altera**	The DSP Development Kit, Stratix V Edition provides a complete design environment that includes all the hardware and software you need to begin developing DSP intensive FPGA designs immediately. The development kit is RoHS-compliant. You can use this development kit to develop and test PCIe designs at data rates up to Gen3, develop and test memory subsystems for DDR3 SDRAM or QDR II SRAM memories, and use the HSMC connectors to interface to one of over 35 different HSMCs provided by Altera partners, supporting protocols such as Serial RapidIO, 10 Gbps Ethernet, SONET, Common Public Radio Interface (CPRI), OBSAI, and others.
S5-6U-VPX (S56X) **BittWare**	This rugged 6U VPX card is based on Altera's Stratix V GX or GS FPGAs. When combined with BittWare's Anemone FPGA coprocessor, the ARM Cortex-A8 control processor, and the ATLANTiS FrameWork FPGA development kit, it creates a flexible and efficient solution for high-performance signal processing and data acquisition. The board provides a configurable 48-port multi-gigabit transceiver interface supporting a variety of protocols, including Serial RapidIO, PCIe, and 10GbE. Additional I/O interfaces include Ethernet, RS-232, JTAG, and LVDS. The board features up to 8 GB of DDR3 SDRAM as well as flash memory for booting the FPGAs. Two VITA 57-compliant FMC sites provide additional flexibility for enhancing the board's I/O and processing capabilities.

Altera and Partner Development Kits

Product and Vendor Name	Description
Stratix V FPGA Kits (continued)	
S5-PCIe-HQ (S5PH-Q) **BittWare**	This half-length PCIe x8 card is based on Altera's Stratix V GX or GS FPGA and is a versatile and efficient solution for high-performance network processing, signal processing, and data acquisition. Combining it with BittWare's Anemone coprocessor and ATLANTiS FrameWork enhances productivity and portability, and allows even greater processing efficiency. Over 16 GB of onboard memory includes DDR3 SDRAM and QDR II/II+ SRAM. Two front-panel QSFP+ cages provide additional flexibility for serial I/O, allowing two 40GbE interfaces (or eight 10GbE), direct to the FPGA for reduced latency, making it ideal for high-frequency trading and networking applications.
S5-PCIe (S5PE) **BittWare**	This PCIe x8 card is based on Altera's Stratix V GX or GS FPGA and is designed for high-performance network processing, signal processing, and data acquisition. Combining it with BittWare's Anemone coprocessor and ATLANTiS FrameWork enhances productivity and portability and allows even greater processing efficiency. The board provides up to 32 GB of DDR3 SDRAM with optional ECC. An optional VITA 57 FMC site provides additional flexibility for enhancing the board's I/O and processing capabilities, making it ideal for analog I/O and processing. The board also has the option of two front-panel QSFP+ cages for serial I/O, which support 10G per lane direct to the FPGA for reduced latency, making it ideal forhigh-frequency trading and networking applications. It is also available with A/D and D/A conversion options.
ProcHILs **GiDel**	This kit is based on Altera's Stratix V and Stratix IV FPGA. This development kit provides a state-of-the-art Hardware in the Loop acceleration tool for running Simulink designs on Altera FPGAs. ProcHILs can automatically translate Simulink designs built using Altera's DSP Builder into FPGA code and run this code under Simulink. The generated code is compatible with the Proc board installed on the target PC and has the synchronization code needed to communicate with Simulink via PCIe.
ProceV **GiDel**	This half-length PCIe x8 card is based on Altera's Stratix V GX or GS FPGA and is a versatile and efficient solution for high-performance network processing, signal processing, and data acquisition. Combining it with GiDEL's PROCWizard software and data management IP cores enhances productivity and portability, and allows even greater processing efficiency. The platform features 16+ GB of onboard memory that includes DDR3 SDRAM and SRAM. Typical sustainable throughput is 8,000 GBps for internal memories and 25+ GBps for onboard memory. Networking capabilities include one CXP connector cage suitable for 100GbE Ethernet (100GBASE-CR10, 100GBASE-SR10), 3×40 GbE, or single Infiniband 12×QDR link, two SFP+ cage suitable for 10 GbE, and Optical Transport Network. Additional I/O interfaces, 2× high-speed inter-board connectors (up to 12×14.1 Gbps full duplex GPIO) for board-to-board and proprietary daughterboards connectivity.
ProcFG **GiDel**	This kit is based on Altera's Stratix V GX and Stratix IV E FPGA. It is used for development of vision algorithms, machine vision, and medical imaging applications. ProcFG combines high-speed acquisition and powerful FPGA processing with selective on-the-fly region of interest (ROI) offloading for convenient processing on standard PCs. The ProcFG captures all incoming image data or dynamically targets and extracts ROIs based on real-time FPGA analysis of the incoming data, and supports acquisition from both line and area scan cameras.
Arria V FPGA and SoC Kits	
Arria V GX FPGA Development Kit, Arria V GX Edition **Altera**	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to an Arria V GX FPGA. This kit includes two Arria V 5AGXFB3H6F40C6N FPGAs, the PCIe x8 form factor, two HSMC connectors, one FPGA mezzanine card (FMC) connector, 1,152 MB 72 bit DDR3 SDRAM, 4 MB 36 bit QDR II+ SRAM, flash memory, and two additional 32 bit DDR3 SDRAM devices. This kit also includes SMA connectors and a bull's-eye connector for differential transceiver I/Os.
Arria V GX Starter Kit, Arria V GX Edition **Altera**	This kit provides a low-cost platform for developing transceiver I/O-based Arria V GX FPGA designs. This kit includes the PCIe x8 form factor, one HSMC connector, a 32 bit DDR3 SDRAM device, one-channel high-speed transceiver input and output connected to SMAs, HDMI output, SDI input and output, 16x2 LCD display, and flash memory.
Arria V SoC Development Kit and SoC Embedded Design Suite **Altera**	The Altera Arria V SoC Development Kit offers a quick and simple approach to develop custom ARM processor-based SoC designs. Altera's midrange, transceiver-based Arria V FPGA fabric provides the highest bandwidth with the lowest total power for midrange applications such as remote radio units, 10G/40G line cards, medical imaging, broadcast studio equipment, and the acceleration of image- and video-processing applications. This development kit includes the SoC Embedded Design Suite software development tools. The development board has PCIe Gen2 x4 lanes (endpoint or rootport), two FMC expansion headers, dual Ethernet PHYs, and various DRAM and flash memories.

Altera and Partner Development Kits

Product and Vendor Name	Description
Cyclone V FPGA and SoC Kits	
Cyclone V E FPGA Development Kits **Altera**	The Cyclone V E Development Kit offers a comprehensive general-purpose development platform for many markets and applications, including industrial, networking, military, and medical applications. The kit features an Altera Cyclone V device and a multitude of onboard resources including multiple banks of DDR3 and LPDDR2 memory, LCD character display, LEDs, user switches, USB, and RJ-45 connectors. The Cyclone V E FPGA Development Kit gives industrial equipment designers greater flexibility in implementing real-time Ethernet communications with industrial Ethernet IP cores.
Cyclone V GT FPGA Development Kit **Altera**	This kit can be used to prototype Cyclone V GT FPGA or Cyclone V GX FPGA applications. It offers a quick and simple way to develop low-cost and low-power system-level designs and achieve rapid results. This kit supports a myriad of functionalities, such as FPGA prototyping, FPGA power measurement, transceiver I/O performance up to 5 Gbps, PCIe Gen2 x4 (at 5 Gbps per lane), endpoint or rootport support.
Cyclone V SoC Development Kit **Altera**	The Altera Cyclone V SoC Development Kit offers a quick and simple approach to develop custom ARM processor-based SoC designs accompanied by Altera's low-power, low-cost Cyclone V FPGA fabric. This kit supports a wide range of functions, such as processor and FPGA prototyping and power measurement, industrial networking protocols, motor control applications, acceleration of image- and video-processing applications, PCIe x4 lane with ~1,000 MBps transfer rate (endpoint or rootport).
Cyclone V GX Development Kit **Terasic Technologies**	The Cyclone V GX Starter Kit offers a robust hardware design platform based on Altera's Cyclone V GX FPGA. This kit is optimized for the lowest cost and power requirement for transceiver applications with industry-leading programmable logic for ultimate design flexibility. The Cyclone V Starter Kit development board includes hardware, such as Arduino Header, on-board USB-Blaster circuit, audio and video capabilities, and an on-board HSMC connector with high-speed transceivers that allows for an even greater array of hardware setups.
MAX V CPLD Kits	
MAX V CPLD Development Kit **Altera**	This low-cost platform will help you quickly begin developing low-cost, low-power CPLD designs. Use this kit as a stand-alone board or combined with a wide variety of daughtercards that are available from third parties.
Stratix IV FPGA Kits	
Stratix IV GX FPGA Development Kit **Altera**	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix IV GX FPGA. This kit includes the PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, SDI, and HDMI interfaces. Memory includes one x64 DDR3 SDRAM, one x16 DDR3 SDRAM, two x18 QDR II+ SRAM, flash, and SSRAM. This kit also includes two SMA connectors for a differential transceiver output. Several oscillators are available at 156.25 MHz, 155.52 MHz, 125 MHz, 100 MHz, and 50 MHz. Other user interfaces include six user pushbuttons, eight dipswitches, eight user LEDs, 7-segment LCD display, and power and temperature measurement circuitry.
Stratix IV GX FPGA Development Kit, 530 Edition **Altera**	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix IV GX FPGA. This kit includes the PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, SDI, and HDMI interfaces. Memory includes one x64 DDR3 SDRAM, one x16 DDR3 SDRAM, two x18 QDR II+ SRAM, flash, and SSRAM. This kit also includes two SMA connectors for a differential transceiver output. Several oscillators are available at 156.25 MHz, 155.52 MHz, 125 MHz, 100 MHz, and 50 MHz. Other user interfaces include six user pushbuttons, eight dipswitches, eight user LEDs, 7- segment LCD display, and power and temperature measurement circuitry.
Stratix IV E FPGA Development Kit **Altera**	This kit allows rapid and early development of designs for high-performance Stratix IV FPGAs. The development board provides general I/Os that connect to onboard switches and indicators, and to the included two-line LCD and 128 x 64 graphics display. The board also has non-volatile and volatile memories (64 MB flash, 4 MB pseudo-SRAM, 36 Mb QDR II SRAM, 128 MB DDR2 DIMM, and 16 MB DDR2 device), HSMC, and 10/100/1000 Ethernet interfaces. The kit is delivered with Quartus II software and all of the cables that are required to use the board straight out of the box.
100G Development Kit, Stratix IV GT Edition **Altera**	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through four x18 QDR II and four x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 11.3 Gbps, verify PMA compliance to standards, such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCIe (Gen1, Gen2, and Gen3), and other major standards. This kit can also validate interoperability between optical modules, such as SFP, SFP+, QSFP, and CFP.
Transceiver Signal Integrity Kit, Stratix IV GX Edition **Altera**	This kit features eight full-duplex transceiver channels with SMA connectors, 156.25 MHz, 155.52 MHz, 125 MHz, 100 MHz, and 50 MHz clock oscillators, six user pushbuttons, eight dipswitches, eight user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, and Ethernet, USB, and JTAG ports.

Altera and Partner Development Kits

Product and Vendor Name	Description
Stratix IV FPGA Kits (continued)	
Transceiver Signal Integrity Development Kit, Stratix IV GT Edition **Altera**	This kit enables a thorough evaluation of transceiver interoperability and SERDES signal integrity by allowing you to evaluate transceiver performance up to 11.3 Gbps. You can generate and check PRBS patterns via a simple-to-use GUI, change differential output voltage (VOD), pre-emphasis, and equalization settings to optimize transceiver performance for your channel, perform jitter analysis, verify PMA compliance to 40G/100G Ethernet, Interlaken, CEI-6G/11G, PCIe (Gen1, Gen2, and Gen3), Serial RapidIO, and other major standards, and validate interoperability between optical modules.
S4-3U-VPX (S43X) **BittWare**	This commercial or rugged 3U VPX card is based on Altera's Stratix IV GX FPGA that is designed specifically for serial I/O-based applications, creating a completely flexible, reconfigurable VPX board. BittWare's ATLANTiS FrameWork and the FINe Host/Control Bridge greatly simplify application development and integration of this powerful board.The board provides a configurable 25-port SERDES interface supporting a variety of protocols, including Serial RapidIO, PCIe, and 10GbE. The board also features 10/100/1000 Ethernet, and up to 4 GB of DDR3 SDRAM. The VITA 57-compliant FMC site provides enhanced flexibility, which supports 10 SERDES, 60 LVDS pairs, and 6 clocks.
SP/D4-AMC (D4AM) **BittWare**	This board features the I/O processing power of two Altera Stratix IV FPGAs and is a mid- or full-size, single-width AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AMC bays, and used in MicroTCA systems. An Altera Stratix IV GX FPGA paired with a Stratix IV E FPGA makes the D4AM an extremely high-density, flexible board. The FPGAs are connected by two full-duplex 2 GBps lanes of parallel I/O for data sharing. Each FPGA supports BittWare's ATLANTiS FrameWork to greatly simplify application development and integration. A VITA 57-compliant FMC site provides enhanced flexibility, which connects directly to the Stratix IV E FPGA for LVDS and to the Stratix IV GX FPGA for SERDES. The board also provides an IPMI system management interface and a configurable 18-port AMC SERDES interface supporting a variety of protocols. Onboard memory includes up to 1 GB of DDR3 SDRAM and 128 MB of flash memory, and Ethernet is available via the AMC front and rear panels. It is also available with A/D and D/A conversion options.
SP/S4-AMC (S4AM) **BittWare**	This board is based on Altera's Stratix IV FPGA and is a mid- or full-size, single-width AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AMC bays, and used in MicroTCA systems. The S4AM features a high-density, low-power Altera Stratix IV GX FPGA designed specifically for serial I/O-based applications, creating a completely flexible, reconfigurable AMC. Providing enhanced flexibility is the VITA 57-compliant FMC site, which features 8 SERDES, 80 LVDS pairs, and 6 clocks directly to the FPGA. BittWare's ATLANTiS FrameWork, in conjunction with the FINe III Host/Control Bridge, greatly simplifies application development and integration of this powerful board. The board also provides an IPMI system management interface, a configurable 15-port AMC SERDES interface supporting a variety of protocols, and a front panel 4x SERDES interface supporting CPRI and OBSAI. Additionally, the board features 10/100 Ethernet, GbE, two banks of DDR3 SDRAM, two banks of QDR II+ SRAM, and flash memory for booting the FPGAs and FINe. It is also available with A/D and D/A conversion options.
4S-XMC (4SXM) **BittWare**	This is a single-width switched mezzanine card (XMC), designed to provide powerful FPGA processing and high-speed serial I/O capabilities to VME, VXS, VPX, cPCI, AdvancedTCA, or PCIe carrier boards. The 4SXM features a high-density, low-power Altera Stratix IV GX FPGA, which was designed specifically for serial I/O-based applications and is PCI-SIG® compliant for PCIe Gen1 and Gen2. Four SFP compact optical transceivers are available on the front panel. There are 8 multi-gigabit serial lanes supporting PCIe, Serial RapidIO, and 10GbE available via the board's rear panel, as well as 44 general-purpose digital I/O signals. The 4SXM also provides QDR II+ SRAM and flash memory.
PROCe IV **GiDel**	This Altera-based PCIe x4 platform is ideal for high-speed data acquisition, algorithmic acceleration, IP validation, and verification of small SoCs. This board has five levels of memory structure (8.5 GB+) with maximum sustainable throughput of 4,693 GBps for internal memories and 12 GBps for DRAM.
PROC104 **GiDel**	This is a PCIe/104 standard Altera-based platform incorporating compact, self-stacking, and rugged industrial-standard connectors. This powerful platform is ideal for high-performance FPGA development and deployment across a range of size, weight, and power-constrained (SWaP-constrained) application areas, including signal intelligence, image processing, software-defined radio, and autonomous modules, or vehicles. The PROC104 can be hosted via 4-lane PCIe and is stackable. The board's high-speed performance coupled with memory and add-on daughterboards' flexible architecture enable the system to meet almost any computational needs. In addition to 512 MB onboard memory, two SODIMM sockets provide up to 8 GB of memory.

Altera and Partner Development Kits

Product and Vendor Name	Description
Stratix IV FPGA Kits (continued)	
PROCStar IV **GiDel**	This full-length PCIe x8 card is based on Altera's Stratix IV E FPGAs. It provides a high-capacity, high-speed FPGA-based platform fortified with high throughput and massive memory resulting in a powerful and highly flexible system. The performance, memory, and add-on daughterboards' flexible architecture enable the system to meet almost any computation needs. In addition to 2 GB onboard memory, 8 SODIMM sockets provide up to 32 GB of memory or additional connectivity and logic. The largest FPGA-based supercomputer at the National Science Foundation Center for High-Performance Reconfigurable Computing (NSF CHREC) center houses 100 of these cards (400 Altera FPGAs) and is used for Bio-RC, HFT, data mining, and seismic analysis applications.
ProcSoC3-4S system **GiDel**	ProcSoC Verification System provides scalability of multiple interconnected FPGA modules, enabling verification of SoC designs from 6 million to 360 million equivalent ASIC gates. Each ProcSoC module itself is a modular and scalable SoC verification system. Fast GbE connection combined with GiDEL's development tools enable it to run the target software or regression suites via remote servers connected to the SoC/ASIC design. The remote operation is performed at near actual system speed allowing for hardware-software integration and co-verification. Two chassis configurations are available, ProcSoC3 and ProcSoC10, capable of supporting up to 3 or 10 PROC12M boards, respectively. Each ProcSoC system can prototype a single SoC or be partitioned to prototype multiple designs in parallel. The ProcSoC's unique interconnectivity topology enables any FPGA to connect directly to any other FPGA in the system even in large systems.
Stratix IV GX/GT 40G/ 100G Interlaken **HiTech Global**	This board integrates the most fundamental electrical and optical interfaces for building 200G subsystems. It implements CAUI and Interlaken high-speed serial interfaces, industry-leading, high-speed DDR3 SDRAM and QDR II+ SRAM interfaces, and high-speed parallel interconnect for NetLogic knowledge-based processors (KBPs). The modular design enables expansion to support legacy and emerging optical modules.
Xpress GX4 Kit **ReFLEX CES**	This kit provides a complete hardware and software environment for Altera Stratix IV GX FPGAs. It is built around a PCI form factor card compliant with PCI-SIG and targets the development of designs using PCIe Gen1 or Gen2.
Single-FPGA (Tile) Prototyping Solution **Polaris Design Systems**	This single-FPGA prototyping board can accommodate up to 15 million gate designs. It has a single Stratix IV FPGA and 18 Mb of SRAM. The board can be used either in a rack-mountable system or as a stand-alone unit.
Multi-FPGA (Logic) Prototyping Solution **Polaris Design Systems**	This multi-FPGA prototyping board can accommodate up to 30 million gate designs. The board has three Stratix IV FPGAs, SRAM, and 2 GB of DDR3 SDRAM (expandable to 8 GB). The board can be used either in a rack-mountable system or as a stand-alone unit.
DN7002k10MEG **The Dini Group**	This complete logic emulation system allows you to prototype SoC logic and memory designs. It can operate as a stand-alone system, or be hosted via a USB interface. A single system, configured with two Stratix IV EP4SE820 FPGAs, can emulate up to 13 million gates. All FPGA resources are available for the target application. Each FPGA position can use any available speed grade.
DN7406k10PCIe-8T **The Dini Group**	This complete logic prototyping system allows you to prototype logic and memory designs. The DN7406k-10PCIe-8T is hosted in an eight-lane PCIe Gen1 bus, but can be used as a stand-alone system configured via USB or CompactFlash. A single board configured with six Altera Stratix IV EP4SE820 FPGAs can emulate up to 31 million gates. All of the FPGA resources are available for your application, and any combination of speed grades can be used.
DN7020k10 **The Dini Group**	This complete logic prototyping system gives ASIC and IP designers a vehicle to prototype logic and memory designs using up to 20 Stratix III or Stratix IV devices.
DN7006K10PCIe-8T **The Dini Group**	This complete logic prototyping system with a dedicated PCIe interface gives ASIC and IP designers a vehicle to prototype logic and memory designs using up to six Stratix III or Stratix IV devices.

Altera and Partner Development Kits

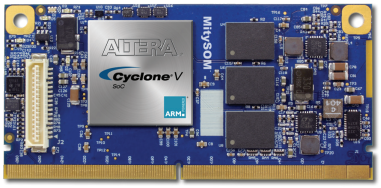
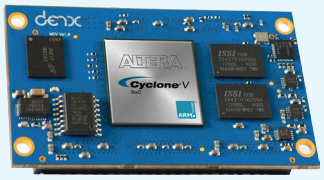
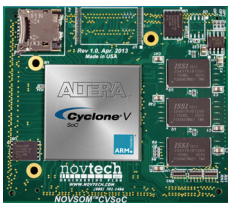
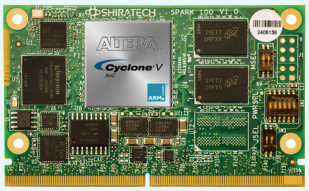
Product and Vendor Name	Description
Cyclone IV FPGA Kits	
Cyclone IV GX FPGA Development Kit **Altera**	This kit provides a comprehensive design environment that allows you to quickly develop low-cost and low-power FPGA system-level designs. This kit includes the PCIe short card form factor, two HSMC connectors, and a 10/100/1000 Mbps Ethernet interface. Onboard memory includes 128 MB DDR2 SDRAM, 64 MB flash, and 4 MB SSRAM. This kit also includes SMA connectors, and 50 MHz, 100 MHz, and 125 MHz clock oscillators, as well as user interfaces including pushbuttons, LEDs, and a 7-segment LCD display.
Cyclone IV GX Transceiver Starter Kit **Altera**	This kit provides a low-cost platform for developing transceiver I/O-based FPGA designs. It includes the complete hardware and software you need to develop your FPGA design for cost-sensitive applications. You can measure the FPGA's power consumption, test the signal quality of the FPGA transceiver I/Os (up to 2.5 Gbps), and develop and test PCIe Gen1 designs.
BeMicro SDK **Arrow**	This Arrow BeMicro SDK enables a quick and easy evaluation of soft core processors for both embedded software developers and hardware engineers. The kit builds on the success of the original BeMicro evaluation kit by adding features, such as Mobile DDR memory, Ethernet, and even the option of using a file system by slotting in a micro-SD card. The BeMicro SDK connects to a PC via a USB connection, which is used for power, programming, and debugging. Arrow has a number of reference designs and pre-built software templates that can be downloaded for this kit that highlight the benefits of building embedded systems in FPGAs.
Industrial Networking Kit **Terasic Technologies**	The Industrial Networking Kit (INK) offers a comprehensive development platform for industrial automation and applications. The kit consists of the DE2-115 board featuring the Altera Cyclone IV device and dual 10/100/1000-Mbps Ethernet, 128 MB SDRAM, 8 MB flash memory, 2 MB SRAM, HSMC and GPIO connectors, USB 2.0, an SD card slot, switches and buttons, LEDs, 16x2 display, audio and video, and VGA-out. The kit also includes an Industrial Communications Board (ICB-HSMC) that supports RS-485, RS-232, CAN, and additional I/O expansion.
DE2-115 Development and Education Board **Terasic Technologies**	This board is part of the DE2 educational development board series and features the Cyclone IV E EP4CE115 FPGA. The DE2-115 offers an optimal balance of low cost, low power, and a rich supply of logic, memory and DSP capabilities, as well as interfaces to support mainstream protocols including GbE. A HSMC connector is provided to support additional functionality and connectivity via HSMC daughtercards and cables.
MAX II CPLD Kits	
MAX II/MAX IIZ Development Kit **System Level Solutions**	This board provides a hardware platform for designing and developing simple and low-end systems based on Altera MAX II or MAX IIZ devices. The board features a MAX II or MAX IIZ EPM240T100Cx or EPM240ZM100Cx device with 240 LEs and 8,192 bits of user flash memory (UFM). The board also supports vertical migration into EPM570T100Cx devices with 570 LEs and 8,192 bits of UFM.
MAX II Micro **Terasic Technologies**	This kit, equipped with the largest Altera MAX II CPLD and an onboard USB-Blaster cable, functions as a development and education board for CPLD designs. This kit also includes reference designs with source code.

SoC System on Modules

www.altera.com/soms

System on modules (SoMs) provide a compact, pre-configured memory and software solution perfect for prototyping, proof-of-concept and initial system production. SoMs enable you to focus on your IP, algorithms, and human/mechanical interfaces rather than fundamentals of the SoC and electrical system and software bring-up. In some cases, SoMs can also make sense for full system production.

The following Altera SoC-based SoMs are available now from Altera Design Services Network (DSN) partners:

Partner	SoM	Altera SoC	Main Memory[1]	Module Image
Critical Link	MitySOM-5CSX	Cyclone V SoC	Up to 2 GB DDR3 with ECC	
DENX Computer Systems	MCV	Cyclone V SoC	1 GB DDR3 SDRAM	
EXOR International	uS02 microSOM™	Cyclone V SoC	1 GB DDR3 SDRAM	
iWave Systems	Qseven Module	Cyclone V SoC	512 MB DDR3 SDRAM with ECC	
NovTech	NOVSOM CV	Cyclone V SoC	Up to 2 GB DDR3 SDRAM with ECC	
Shiratech	Spark-100	Cyclone V SoC	1 GB to 4 GB with ECC	

Notes:

1. Processor main memory only. Additional FPGA, flash memory, eMMC, microSD, SD/MMC, and EEPROM memory may be provided but is not shown in this table. Consult SoM vendor specifications for complete memory details.

For more information about Altera SoC system on modules, visit **www.altera.com/soms.**

Training Overview

www.altera.com/training

We offer an extensive curriculum of classes to deepen your expertise. Our classes are beneficial whether you're new to FPGA, CPLD, and SoC design, or are an advanced user wanting an update on the latest tools, tips, and tricks. Our training paths are delivered in three ways:

- Instructor-led training, typically lasting one to two days, involves in-person instruction with hands-on exercises from an Altera or Altera partner subject matter expert. Fees vary.
- Virtual classrooms, involving live instructor-taught training over the Web, allow you to benefit from the interactivity with an instructor from the comfort of your home or office. Classes are taught in 4.5-hour sessions across consecutive days.
- Online training, typically 30 minutes long, features pre-recorded presentations and demonstrations. Online classes are free and can be taken at any time.

To help you decide which courses might be most useful to you, we've grouped classes into specific curricula. Curricula paths include Altera Fundamentals, I/O Interfaces, Embedded Hardware, Software Development, DSP, and more.

Learn more about our training program or sign up for classes at www.altera.com/training. Start sharpening your competitive edge today!

Instructor-Led, Virtual, and Online Classes

www.altera.com/training

Altera Instructor-Led and Virtual Classroom Courses
Virtual Classroom Courses Denoted with a *
(All Courses Are One Day in Length Unless Otherwise Noted)

Course Category	General Description	Course Titles
Design languages	Attain the skills needed to design with Verilog HDL and VHDL for programmable logic	• Introduction to VHDL* • Advanced VHDL Design Techniques* • Introduction to Verilog HDL* • Advanced Verilog HDL Design Techniques*
Quartus II software	Acquire design entry, compilation, programming, verification, and optimization skills by learning how to use both basic and advanced features of Quartus II software	• The Quartus II Software Design Series: Foundation* • The Quartus II Software Debug and Analysis Tools • The Quartus II Software Design Series: Timing Analysis* • Advanced Timing Analysis with TimeQuest* • Timing Closure with the Quartus II Software* • Design Optimization Using Quartus II Incremental Compilation* • Partial Reconfiguration with Altera FPGAs
Software development	Accelerate algorithm performance with Open Computing Language (OpenCL) by offloading to an FPGA	• Parallel Computing with OpenCL Workshop* • Optimizing OpenCL for Altera FPGAs*
System integration	Build hierarchical systems by integrating IP and custom logic	• Introduction to the Qsys System Integration Tool* • Advanced Qsys System Integration Tool Methodologies*
Embedded system design	Learn to design an ARM-based or Nios II processor system in an Altera FPGA	• Designing with the Nios II Processor • Developing Software for the Nios II Processor • Designing with an ARM-based SoC • Developing Software for an ARM-based SoC
Memory interfaces	Implement interfaces to external memory	• Implementing, Simulating, and Debugging External Memory Interfaces*
System design	Solve DSP and video system design challenges using Altera technology	• Designing with DSP Builder Advanced Blockset* • Video Design Framework Workshop
Connectivity design	Build high-speed, gigabit interfaces using embedded transceivers found in leading-edge FPGA families	• Building Gigabit Interfaces in Generation 10 Devices • Building Gigabit Interfaces in 28 nm Devices • Creating PCI Express Links Using FPGAs
Timing Analysis and Timing Closure	Learn the latest methodology and techniques to analyze and close timing on your design	• Designing with the Quartus II Software: Timing Analysis* • Advanced Timing Analysis with TimeQuest* • Timing Closure with the Quartus II Software* • Performance Optimization with the Stratix 10 HyperFlex Architecture** • Advanced Optimization with the Stratix 10 HyperFlex Architecture** **Please contact custrain@altera.com for information about this class

Online Training

Altera Free Online Training Courses (Courses Are Approximately 30 Minutes Long)		
Course Category	**Course Titles**	**Languages**
Getting started	Read Me First!	English, Chinese, and Japanese
	Basics of Programmable Logic	English, Chinese, and Japanese
	How to Begin a Simple FPGA Design	English, Chinese, and Japanese
	Become an FPGA Designer in 4 Hours	English only
Design languages	VHDL Basics	English, Chinese, and Japanese
	Verilog HDL Basics	English, Chinese, and Japanese
	SystemVerilog with the Quartus II Software	English, Chinese, and Japanese
	Best HDL Design Practices for Timing Closure	English, Chinese, and Japanese
Software overview and design entry	Using the Quartus II Software: An Introduction	English, Chinese, and Japanese
	The Quartus II Software Interactive Tutorial	English only
	The Quartus II Software Design Series: Foundation (note: this training is similar to the instructor-led course of the same name)	English, Chinese, and Japanese
	Setting Up Floating Licenses	English only
	Synplify Pro Tips and Tricks	English only
	Synplify Synthesis Techniques with the Quartus II Software	English only
	Using Quartus II Software: Schematic Design	English and Chinese
	Introduction to Incremental Compilation	English, Chinese, and Japanese
	Advanced I/O System Design	English and Chinese
	Managing Metastability with the Quartus II Software	English only
	Partial Reconfiguration	English and Chinese
Verification and debugging	Overview of Mentor Graphics ModelSim Software	English and Japanese
	SignalTap II Embedded Logic Analyzer: Getting Started	English, Chinese, and Japanese
	Using Quartus II Software: Chip Planner	English only
	Debugging and Communicating with an FPGA Using the Virtual JTAG Megafunction	English only
	System Console	English and Chinese
	Debugging JTAG Chain Integrity	English only
	Power Analysis and Optimization	English and Chinese
	Resource Optimization	English and Chinese

Online Training

Altera Free Online Training Courses (Courses Are Approximately One Hour Long)		
Course Category	**Course Titles**	**Languages**
Timing analysis and closure	TimeQuest Timing Analyzer	English, Chinese, and Japanese
	Timing Closure Using Quartus II Advisors and Design Space Explorer	English and Chinese
	Timing Closure Using Quartus II Physical Synthesis Optimizations	English and Chinese
	Timing Closure Using TimeQuest Custom Reporting	English only
	Design Evaluation for Timing Closure	English and Chinese
	Good High-Speed Design Practices	English only
	Constraining Source Synchronous Interfaces	English and Chinese
	Constraining Double Data Rate Source Synchronous Interfaces	English, Chinese, and Japanese
Memory interfaces	Using High-Performance Memory Interfaces in Altera FPGAs	English and Chinese
	Introduction to Memory Interfaces IP in Generation 10 Devices	English and Japanese
	Integrating Memory Interfaces IP in Generation 10 Devices	English and Japanese
	On-Chip Debugging of Memory Interfaces IP in Generation 10 Devices	English and Japanese
	Verifying Memory Interfaces IP in Generation 10 Devices	English and Japanese
Connectivity design	Transceiver Basics	English, Chinese, and Japanese
	Transceiver Reconfiguration in Altera 28 nm Devices	English only
	Generation 10 Transceiver Clocking	English only
	Generation 10 Transceiver Reconfiguration	English only
	Building a Generation 10 Transceiver PHY Layer	English only
	Advanced Signal Conditioning for Stratix IV and Stratix V Receivers	English only
	Getting Started with Altera's 28 nm PCI Express Solutions	English only
	Getting Started with Altera's 40 nm PCI Express Solutions	English and Japanese
	Custom Protocol Design in Altera 28 nm Devices	English and Chinese
	Introduction to Altera's 10/100/1000 Mb Ethernet Solutions	English and Chinese
	Introduction to Altera's 10 Gb Ethernet Solutions	English only
System design	Introduction to Qsys	English and Japanese
	Creating a System Design with Qsys	English and Japanese
	Advanced System Design Using Qsys	English only
	Custom IP Development Using Avalon and AXI Interfaces	English, Chinese, and Japanese
	Designing with DSP Builder Advanced Blockset: An Overview	English and Chinese
	High-Performance Floating-Point Processing with FPGAs	English only
	Building Video Systems	English and Chinese
	Implementing Video Systems	English only
	Creating Reusable Design Blocks: Introduction to IP Reuse	English only
	Creating Reusable Design Blocks: IP Design & Implementation	English only
	Creating Reusable Design Blocks: IP Integration with the Quartus II Software	English only
	FIR Compiler II	English only
	Avalon Verification Suite	English and Chinese

Online Training

Altera Free Online Training Courses (Courses Are Approximately One Hour Long)		
Course Category	**Course Titles**	**Languages**
OpenCL	Introduction to Parallel Computing with OpenCL	English, Japanese, and Chinese
	Writing OpenCL Programs for Altera FPGAs	English, Japanese, and Chinese
	Running OpenCL on Altera FPGAs	English, Japanese, and Chinese
	OpenCL: Single-Threaded vs. Multi-Threaded Kernels	English only
	Building Custom Platforms for Altera SDK for OpenCL	English only
Embedded system design	Designing with the Nios II Processor and Qsys - Day 1	Japanese only
	Developing Software for the Nios II Processor: Tools Overview	English and Chinese
	Developing Software for the Nios II Processor: Design Flow	English and Chinese
	Hardware Design Flow for an ARM-Based SoC	English, Chinese, and Japanese
	Software Design Flow for an ARM-Based SoC	English, Chinese, and Japanese
	SoC Hardware Overview: Flash Controllers and Interface Protocols	English only
	SoC Hardware Overview: Interconnect and Memory	English only
	SoC Hardware Overview: System Management, Debug, and General Purpose Peripherals	English only
	SoC Hardware Overview: the Microprocessor Unit	English only
	Using the Nios II Processor	English, Chinese, and Japanese
	Developing Software for the Nios II Processor: Nios II Software Build Tools for Eclipse	English and Japanese
	Nios II Software Build Tools for Eclipse and BSP Editor (Quartus II Software 10.0 Update)	English only
	Developing Software for the Nios II Processor: HAL Primer	English, Chinese, and Japanese
	Developing Software for the Nios II Processor: MMU and MPU	English and Chinese
	Lauterbach Debug Tools	English only
	Introduction to Graphics	English only
Device-specific training	Configuring Altera FPGAs	English and Chinese
	Integrating an Analog to Digital Converter in MAX 10 Devices	English only
	Introduction to Analog to Digital Conversion in MAX 10 Devices	English only
	Using the ADC Toolkit in MAX 10 Devices	English only
Scripting	Command-Line Scripting	English only
	Introduction to Tcl	English and Chinese
	Quartus II Software Tcl Scripting	English, Chinese, and Japanese

Glossary

Below is a glossary of helpful terms to bring you up to speed on Altera devices.

Term	Definition
Adaptive logic module (ALM)	Logic building block, used by some Altera devices, which provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two combinational adaptive LUTs (ALUTs).
Configuration via Protocol (CvP)	CvP is a configuration method that enables you to configure the FPGA using industry-standard protocols. Currently CvP supports the PCIe protocol.
Embedded hard IP blocks	These metal-programmable hard IP blocks deliver up to 14M ASIC gates or up to 700K additional LEs to harden standard or logic-intensive applications.
Equivalent LE	Device density represented as a comparable amount of LEs, which uses the 4-input LUT as a basis.
Fractional phase-locked loops (fractional PLLs)	A phase-locked loop (PLL) in the core fabric, fractional PLLs provide increased flexibility as an additional clocking source for the transceiver, replacing external VCXOs.
Global clock networks	Global clocks can drive throughout the entire device, serving as low-skew clock sources for functional blocks such as ALMs, DSP blocks, TriMatrix memory blocks, and PLLs. See regional clocks and periphery clocks for more clock network information.
Hard processor system (HPS)	This processor system is a hardened component within the SoC, that comprises a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and multiport memory controllers.
Logic element (LE)	This logic building block, used by some Altera devices, includes a 4-input LUT, a programmable register, and a carry chain connection. See device handbooks for more information.
Macrocells	Similar to LEs, this is the measure of density in MAX series CPLDs.
Memory logic array blocks (MLABs)	MLABs are dual-purpose blocks, configurable as regular logic array blocks or as memory blocks.
On-chip termination (OCT)	Support for driver impedance matching and series termination, which eliminates the need for external resistors, improves signal integrity, and simplifies board design. On-chip series, parallel, and differential termination resistors are configurable via the Quartus II software.
Periphery clocks (PCLKs)	PCLKs are a collection of individual clock networks driven from the periphery of the device. PCLKs can be used instead of general-purpose routing to drive signals into and out of the device.
Plug and play signal integrity	This capability, consisting of Altera's adaptive dispersion engine and hot socketing, lets you change the position of backplane cards on the fly, without having to manually configure your backplane equalization settings.
Programmable power technology	This feature automatically optimizes logic, DSP, and memory blocks for the lowest power at the required performance. Only the blocks with critical-path logic need to be in high-performance mode; all others are in low-power mode.
Real-time in-system programming (ISP)	This capability allows you to program a MAX II and MAX V device while the device is still in operation. The new design only replaces the existing design when there is a power cycle to the device, so can perform in-field updates to the MAX II and MAX V device at any time without affecting the operation of the whole system.
Regional clocks	Regional clocks are device quadrant-oriented and provide the lowest clock delay and skew for logic contained within a single device quadrant.
System on a chip (SoC)	An SoC is an embedded system that consists of a processor, peripherals, and custom hardware integrated on a single device.
Variable-precision blocks	These integrated blocks provide native support for signal processing of varying precisions—for example, 9 x 9, 27 x 27, and 18 x 36—in a sum or independent mode.

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