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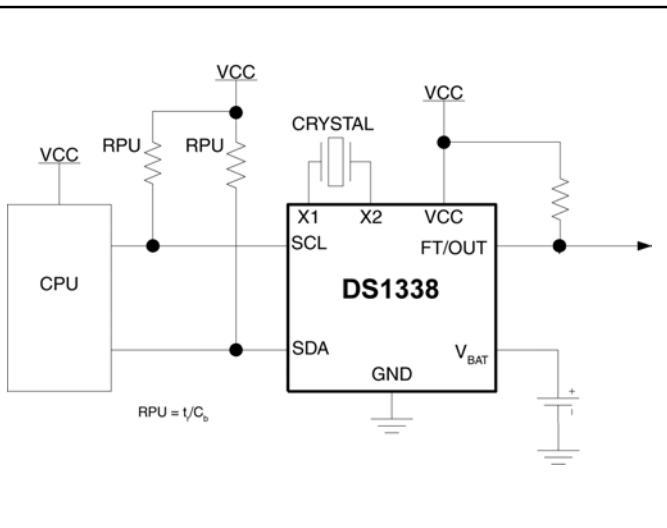
### GENERAL DESCRIPTION

The DS1338 serial real-time clock (RTC) is a low-power, full binary-coded decimal (BCD) clock/calendar plus 56 Bytes of NV SRAM. Address and data are transferred serially through a 2-wire bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1338 has a built-in power-sense circuit that detects power failures and automatically switches to the battery supply.

### APPLICATIONS

Handhelds (GPS, POS Terminal)  
 Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)  
 Office Equipment (Fax/Printer, Copier)  
 Medical (Glucometer, Medicine Dispenser)  
 Telecommunications (Router, Switcher, Server)  
 Other (Utility Meter, Vending Machine, Thermostat, Modem)

### TYPICAL OPERATING CIRCUIT



**Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: [www.maxim-ic.com/errata](http://www.maxim-ic.com/errata).

### FEATURES

- RTC Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
- 56-Byte Battery-Backed NV RAM for Data Storage
- 2-Wire Serial Interface
- Programmable Square-Wave Output Signal
- Automatic Power-Fail Detect and Switch Circuitry
- Consumes Less than 500nA in Battery-Backup Mode with Oscillator Running
- Recognized by Underwriters Laboratory (UL)

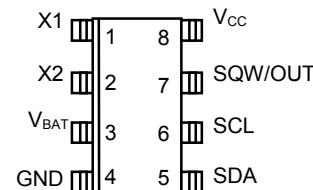
### ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS1338Z-18	-40°C to +85°C	8 SO (150mil)	DS1338-18
DS1338Z-3	-40°C to +85°C	8 SO (150mil)	DS1338-3
DS1338Z-33	-40°C to +85°C	8 SO (150mil)	DS1338-33
DS1338U-18	-40°C to +85°C	8 µSOP	1338 rr-18
DS1338U-3	-40°C to +85°C	8 µSOP	1338 rr-3
DS1338U-33	-40°C to +85°C	8 µSOP	1338 rr-33

rr = revision level

### PIN CONFIGURATION

#### TOP VIEW



[SO, µSOP](#)

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

## RECOMMENDED DC OPERATING CONDITIONS

( $V_{CC} = V_{CC\ MIN}$  to  $V_{CC\ MAX}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC}$	DS1338-18	1.71	1.8	1.89	V
		DS1338-3	2.7	3.0	3.3	
		DS1338-33	3.0	3.3	3.63	
Logic 1	$V_{IH}$	(Note 2)	0.7 $V_{CC}$	$V_{CC} + 0.3$		
Logic 0	$V_{IL}$	(Note 2)	-0.3	0.3 $V_{CC}$		
Power-Fail Voltage	$V_{PF}$	DS1338-18	1.51	1.62	1.71	V
		DS1338-3	2.45	2.59	2.70	
		DS1338-33	2.70	2.82	2.97	
$V_{BAT}$ Battery Voltage	$V_{BAT}$	(Note 2)	1.3	3.0	3.7	V

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = V_{CC\ MIN}$  to  $V_{CC\ MAX}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{BAT}$ Battery Voltage	$V_{BAT}$	(Note 2)	1.3	3.7		V
Input Leakage	$I_{LI}$	(Note 3)		1		$\mu\text{A}$
I/O Leakage	$I_{LO}$	(Note 4)		1		$\mu\text{A}$
SDA Logic 0 Output	$I_{OLSDA}$	$V_{CC} > 2\text{V}; V_{OL} = 0.4\text{V}$		3.0		mA
		$V_{CC} < 2\text{V}; V_{OL} = 0.2\text{V}_{CC}$		3.0		
SQW/OUT Logic 0 Output	$I_{OLSQW}$	$V_{CC} > 2\text{V}; V_{OL} = 0.4\text{V}$		3.0		mA
		$1.71\text{V} < V_{CC} < 2\text{V}; V_{OL} = 0.2\text{V}_{CC}$		3.0		
		$1.3\text{V} < V_{CC} < 1.71\text{V}; V_{OL} = 0.2\text{V}_{CC}$		250		$\mu\text{A}$
Active Supply Current (Note 5)	$I_{CCA}$	DS1338-18	75	150		$\mu\text{A}$
		DS1338-3	110	200		
		DS1338-33	120	200		
Standby Current (Note 6)	$I_{CCS}$	DS1338-18	60	100		$\mu\text{A}$
		DS1338-3	80	125		
		DS1338-33	85	125		
$V_{BAT}$ Leakage Current ( $V_{CC}$ Active)	$I_{BATLKG}$		25	100		nA

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 0V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Oscillator Current (OSC ON); $V_{BAT} = 3.7V$ , SQW/OUT OFF (Note 7)	$I_{BATOSC1}$		400	1200	nA
Oscillator Current (OSC ON); $V_{BAT} = 3.7V$ , SQW/OUT ON (32kHz) (Note 7)	$I_{BATOSC2}$		570	1400	nA
$V_{BAT}$ Data-Retention Current; $V_{BAT} = 3.7V$ (Oscillator Off, $V_{CC} = 0.0V$ )	$I_{BATDAT}$		10	100	nA

## CRYSTAL SPECIFICATIONS\*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	$f_0$		32.768		kHz
Series Resistance	ESR			45	$k\Omega$
Load Capacitance	$C_L$		12.5		pF

\*The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks for additional specifications.

## AC ELECTRICAL CHARACTERISTICS

( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) (Note 1)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SCL Clock Frequency	$f_{\text{SCL}}$	Fast mode	100	400		kHz
		Standard mode		100		
Bus Free Time Between STOP and START Condition	$t_{\text{BUF}}$	Fast mode	1.3			$\mu\text{s}$
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 8)	$t_{\text{HD:STA}}$	Fast mode	0.6			$\mu\text{s}$
		Standard mode	4.0			
LOW Period of SCL Clock	$t_{\text{LOW}}$	Fast mode	1.3			$\mu\text{s}$
		Standard mode	4.7			
HIGH Period of SCL Clock	$t_{\text{HIGH}}$	Fast mode	0.6			$\mu\text{s}$
		Standard mode	4.0			
Setup Time for Repeated START Condition	$t_{\text{SU:STA}}$	Fast mode	0.6			$\mu\text{s}$
		Standard mode	4.7			
Data Hold Time (Notes 9, 10)	$t_{\text{HD:DAT}}$	Fast mode	0	0.9		$\mu\text{s}$
		Standard mode	0			
Data Setup Time (Note 11)	$t_{\text{SU:DAT}}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 12)	$t_{\text{R}}$	Fast mode	$20 + 0.1C_B$	300		ns
		Standard mode		1000		
Fall Time of Both SDA and SCL Signals (Note 12)	$t_{\text{F}}$	Fast mode	$20 + 0.1C_B$	300		ns
		Standard mode		300		
Setup Time for STOP Condition	$t_{\text{SU:STO}}$	Fast mode	0.6			$\mu\text{s}$
		Standard mode	4.0			
Capacitive Load for Each Bus Line (Note 12)	$C_B$			400		pF
I/O Capacitance	$C_{\text{I/O}}$			10		pF
Oscillator Stop Flag (OSF) Delay (Note 13)	$t_{\text{OSF}}$			100		ms

## POWER-UP/POWER-DOWN CHARACTERISTICS

( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Recovery at Power-Up (Note 14)	$t_{\text{REC}}$			2	ms
$V_{\text{CC}}$ Fall Time; $V_{\text{PF}(\text{MAX})}$ to $V_{\text{PF}(\text{MIN})}$	$t_{\text{VCCF}}$	300			$\mu\text{s}$
$V_{\text{CC}}$ Rise Time; $V_{\text{PF}(\text{MIN})}$ to $V_{\text{PF}(\text{MAX})}$	$t_{\text{VCCR}}$	0			$\mu\text{s}$

**Note 1:** Limits at  $-40^\circ\text{C}$  are guaranteed by design and not production tested.

**Note 2:** All voltages are referenced to ground.

**Note 3:** SCL only.

**Note 4:** SDA and SQW/OUT.

**Note 5:**  $I_{\text{CCA}}$ —SCL clocking at max frequency = 400kHz.

**Note 6:** Specified with 2-wire bus inactive.

**Note 7:** Measured with a 32.768kHz crystal attached to X1 and X2.

**Note 8:** After this period, the first clock pulse is generated.

**Note 9:** A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the  $V_{\text{IHMIN}}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

**Note 10:** The maximum  $t_{\text{HD:DAT}}$  has only to be met if the device does not stretch the LOW period ( $t_{\text{LOW}}$ ) of the SCL signal.

**Note 11:** A fast mode device can be used in a standard mode system, but the requirement  $t_{\text{SU:DAT}} \geq 250\text{ns}$  must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{\text{R MAX}} + t_{\text{SU:DAT}} = 1000 + 250 = 1250\text{ns}$  before the SCL line is released.

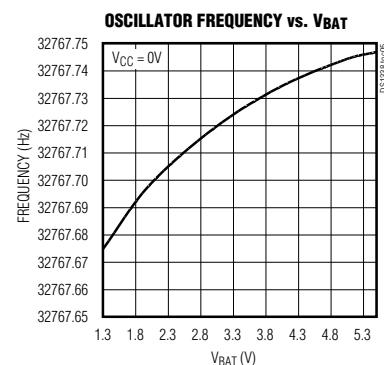
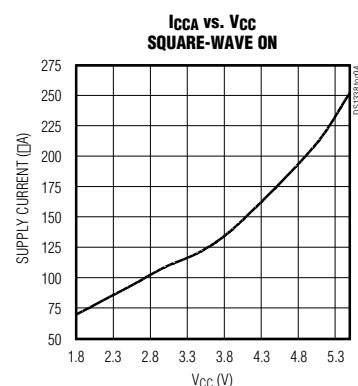
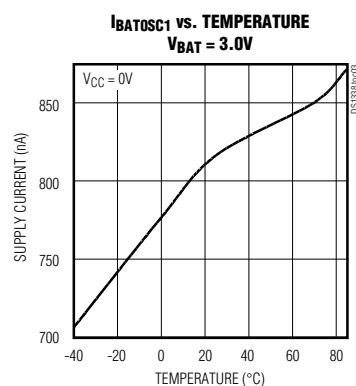
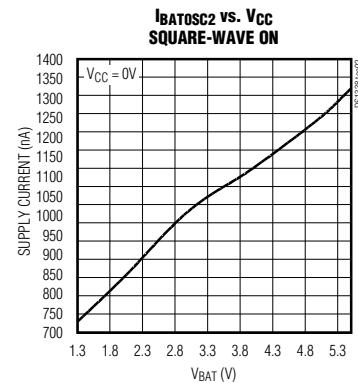
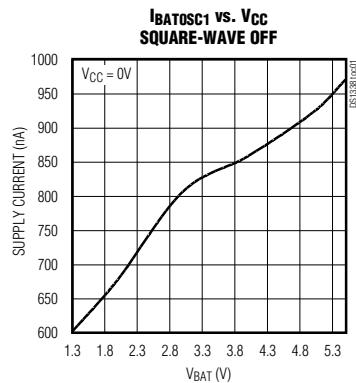
**Note 12:**  $C_B$ —total capacitance of one bus line in pF.

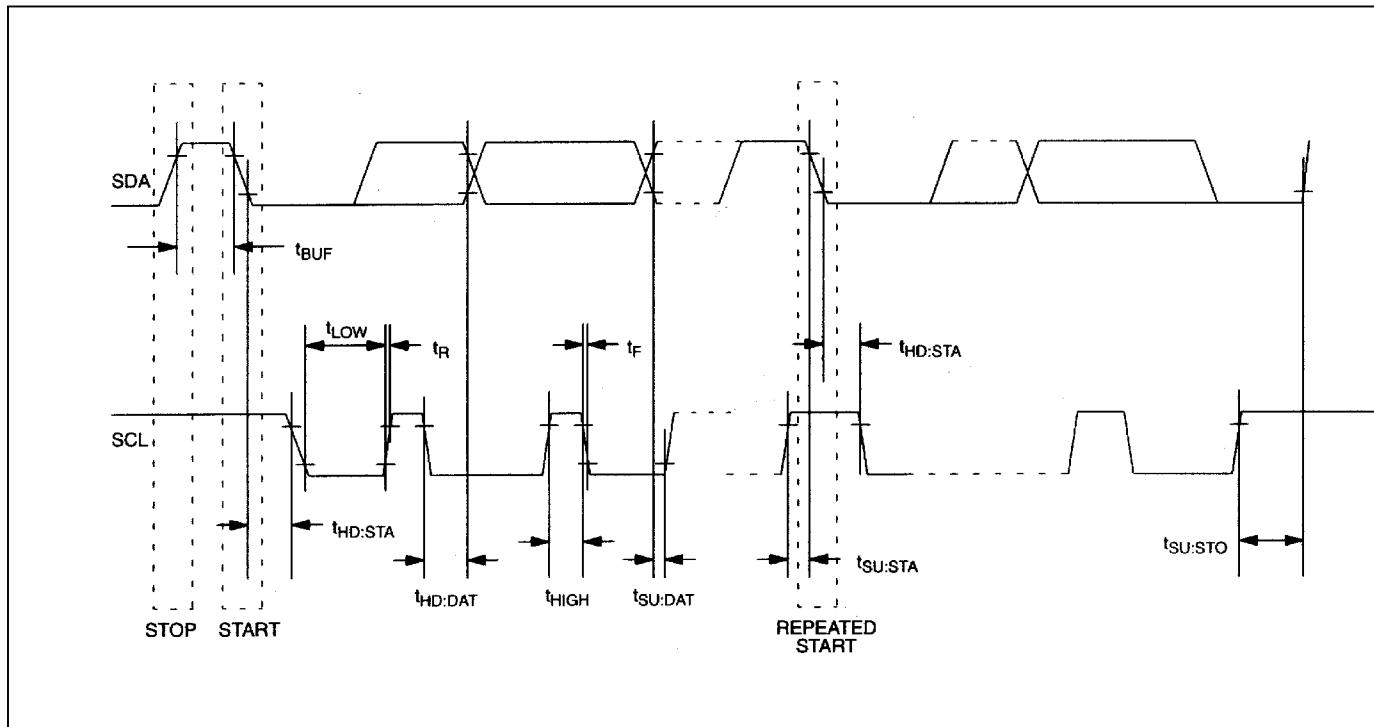
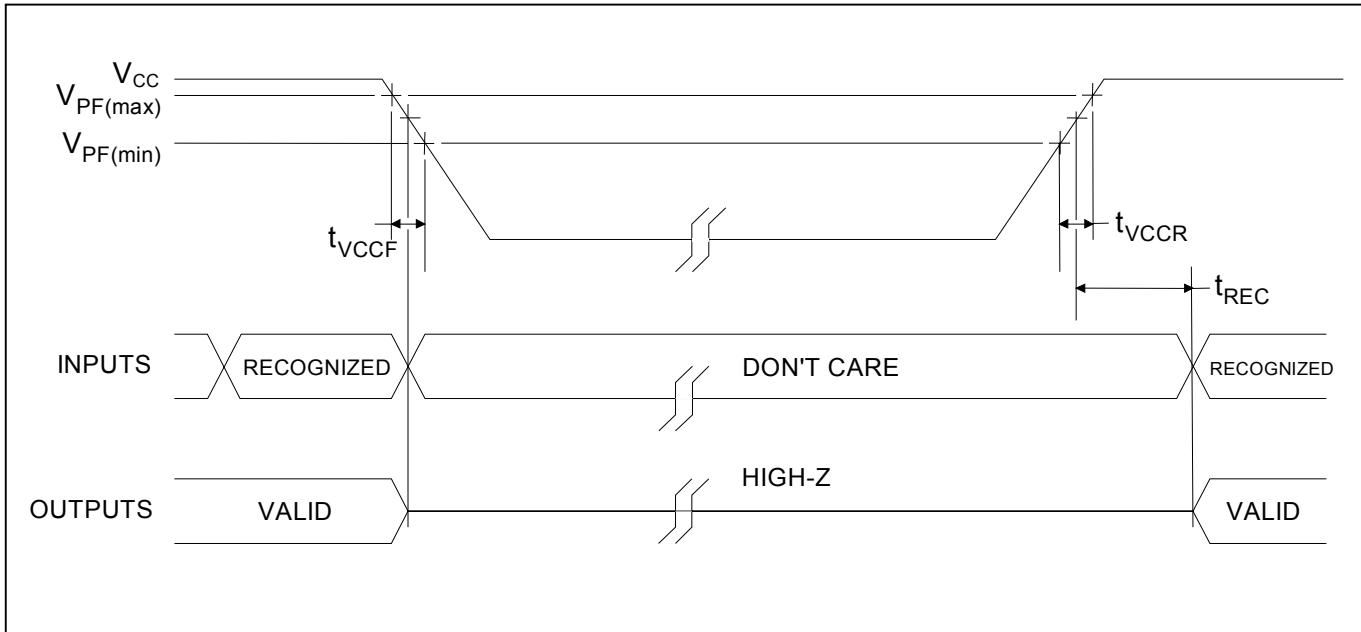
**Note 13:** The parameter  $t_{\text{OSF}}$  is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of  $0.0\text{V} \leq V_{\text{CC}} \leq V_{\text{CC MAX}}$  and  $1.3\text{V} \leq V_{\text{BAT}} \leq 3.7\text{V}$ .

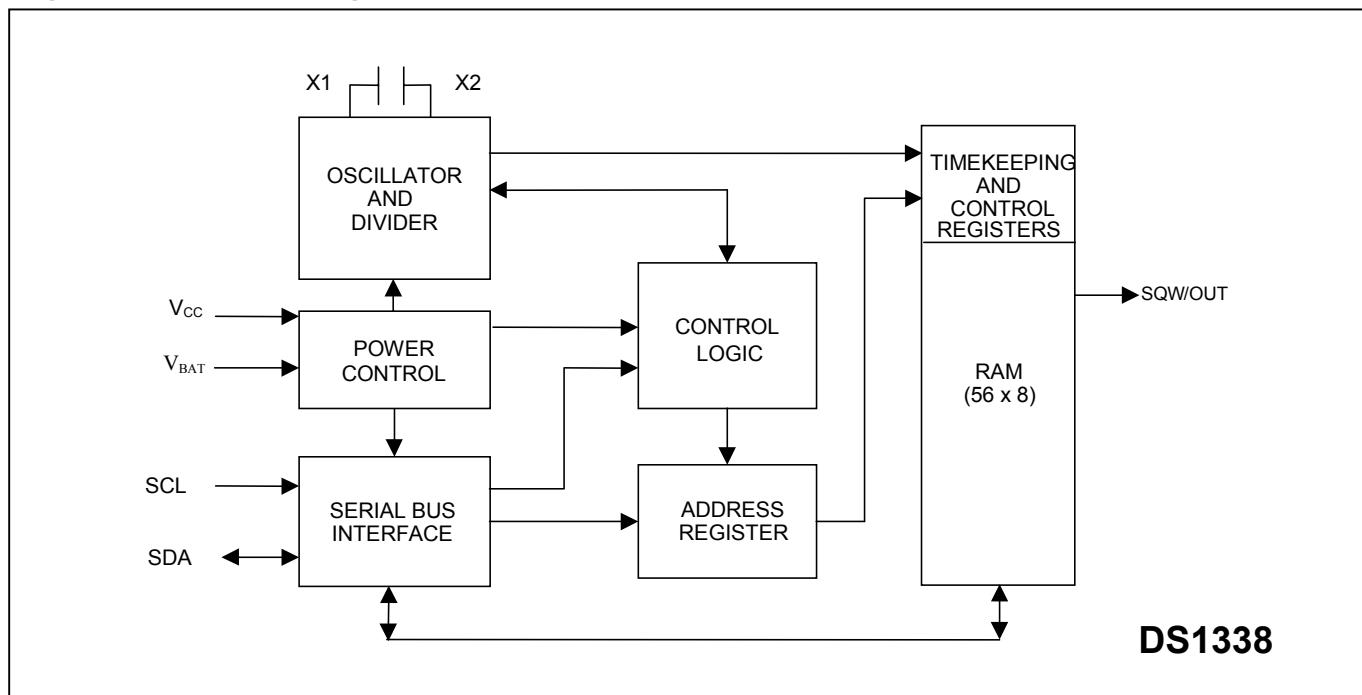
**Note 14:** This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

## TYPICAL OPERATING CHARACTERISTICS

( $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



**Figure 1. Timing Diagram****Figure 2. Power-Up/Power-Down Timing**

**Figure 3. Block Diagram**

## PIN DESCRIPTION

PIN	NAME	FUNCTION
1	X1	32.768kHz Crystal Connections. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance ( $C_L$ ) of 12.5pF. Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1. An external 32.768kHz oscillator can also drive the DS1338. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.  <i>Note: For more information about crystal selection and crystal layout considerations, refer to Application Note 58: Crystal Considerations with Dallas Real-Time Clocks.</i>
2	X2	
3	$V_{BAT}$	+3V Battery Input. Backup supply input for any standard 3V lithium cell or other energy source. Battery voltage must be held between the minimum and maximum limits for proper operation. If a backup supply is not required, $V_{BAT}$ must be grounded.
4	GND	Ground. DC power is provided to the device on these pins. $V_{CC}$ is the primary power input. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and $V_{CC}$ is below $V_{PF}$ , reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.
5	SDA	Serial Data. Input/output pin for the 2-wire serial interface. It is open drain and requires an external pullup resistor.
6	SCL	Serial Clock. Used to synchronize data movement on the serial interface
7	SQW/OUT	Square-Wave/Output Driver. When enabled and the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). It is open drain and requires an external pullup resistor. Operates with either $V_{CC}$ or $V_{BAT}$ applied.
8	$V_{CC}$	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and $V_{CC}$ is below $V_{PF}$ , reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

## Detailed Description

The DS1338 serial RTC is a low-power, full BCD clock/calendar plus 56 Bytes of NV SRAM. Address and data are transferred serially through a 2-wire bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1338 has a built-in power-sense circuit that detects power failures and automatically switches to the battery supply.

## Operation

The DS1338 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when  $V_{CC}$  is greater than  $V_{PF}$ . However, when  $V_{CC}$  falls below  $V_{PF}$ , the internal clock registers are blocked from any access. If  $V_{PF}$  is less than  $V_{BAT}$ , the device power is switched from  $V_{CC}$  to  $V_{BAT}$  when  $V_{CC}$  drops below  $V_{PF}$ . If  $V_{PF}$  is greater than  $V_{BAT}$ , the device power is switched from  $V_{CC}$  to  $V_{BAT}$  when  $V_{CC}$  drops below  $V_{BAT}$ . The registers are maintained from the  $V_{BAT}$  source until  $V_{CC}$  is returned to nominal levels. The block diagram (Figure 3) shows the main elements of the DS1338.

An enable bit in the seconds register controls the oscillator. Oscillator start-up times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long start-up times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within 1 second.

## RTC and RAM Address Map

Figure 5 shows the address map for the RTC and RAM registers. The RTC registers and control register are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multibyte access, when the register pointer reaches 3Fh (the end of RAM space) it wraps around to location 00h (the beginning of the clock space). On a 2-wire START, STOP, or register pointer incrementing to location 00h, the current time and date is transferred to a second set of registers. The time and date in the secondary registers are read in a multibyte data transfer, while the clock continues to run. This eliminates the need to reread the registers in case of an update of the main registers during a read.

## Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. See Figure 4 for the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. Bit 7 of Register 0 is the clock halt (CH) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled. The clock can be halted whenever the timekeeping functions are not required, which decreases  $V_{BAT}$  current.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero. The countdown chain is reset whenever the seconds register is written. Write transfers occur on the

acknowledge from the DS1338. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

**Please note that the initial power-on state of all registers, unless otherwise specified, is not defined. Therefore, it is important to enable the oscillator (CH = 0) during initial configuration.**

The DS1338 runs in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit, with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours).

On a 2-wire START, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case of an update of the main registers during a read.

**Figure 4. RTC and RAM Address Map**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	CH	10 seconds				seconds				seconds 00–59
01H	0	10 minutes				minutes				minutes 00–59
02H	0	12/24	AM/PM	10 hour	hour				hours	1–12 +am/pm 00–23
			10 hour							
03H	0	0	0	0	0	day				day 1–7
04H	0	0	10 date		date				date	00–31
05H	0	0	0	10 mo	month				month	01–12
06H	10 year				year				year	00–99
07H	OUT	0	OSF	SQWE	0	0	RS1	RS0	control	
08H–3FH									RAM 56 x 8	00H–FFH

## Control Register (07h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	0	OSF	SQWE	0	0	RS1	RS0

The control register controls the operation of the SQW/OUT pin and provides oscillator status.

BIT	NAME	FUNCTION
7	OUT	Output Control. Controls the output level of the SQW/OUT pin when the square-wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if OUT = 1; it is 0 if OUT = 0.
5	OSF	<p>Oscillator Stop Flag. A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some time period and can be used to judge the validity of the clock and calendar data. This bit is edge triggered, and is set to logic 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that may cause the OSF bit to be set:</p> <ol style="list-style-type: none"> <li>1) The first time power is applied.</li> <li>2) The voltage present on V<sub>CC</sub> and V<sub>BAT</sub> are insufficient to support oscillation.</li> <li>3) The CH bit is set to 1, disabling the oscillator.</li> <li>4) External influences on the crystal (i.e., noise, leakage, etc.).</li> </ol> <p>This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.</p>
4	SQWE	Square-Wave Enable. When set to logic 1, this bit enables the oscillator output to operate with either V <sub>CC</sub> or V <sub>BAT</sub> applied. The frequency of the square-wave output depends upon the value of the RS0 and RS1 bits.
1, 0	RS	Rate Select. These bits control the frequency of the square-wave output when the square-wave output has been enabled. Table 1 lists the square-wave frequencies that can be selected with the RS bits.

**Table 1. Square-Wave Output Frequency**

RS1	RS0	SQW OUTPUT FREQUENCY
0	0	1Hz
0	1	4.096kHz
1	0	8.192kHz
1	1	32.768kHz

## 2-Wire Serial Data Bus

The DS1338 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device, which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1338 operates as a slave on the 2-wire bus. Within the bus specifications, a standard mode (100kHz cycle rate) and a fast mode (400kHz cycle rate) are defined. The DS1338 works in both modes.

Figures 5, 6, and 7 detail how data is transferred on the 2-wire bus.

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

**Bus not busy:** Both data and clock lines remain HIGH.

**Start data transfer:** A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

**Stop data transfer:** A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

**Data valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the 2-wire bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

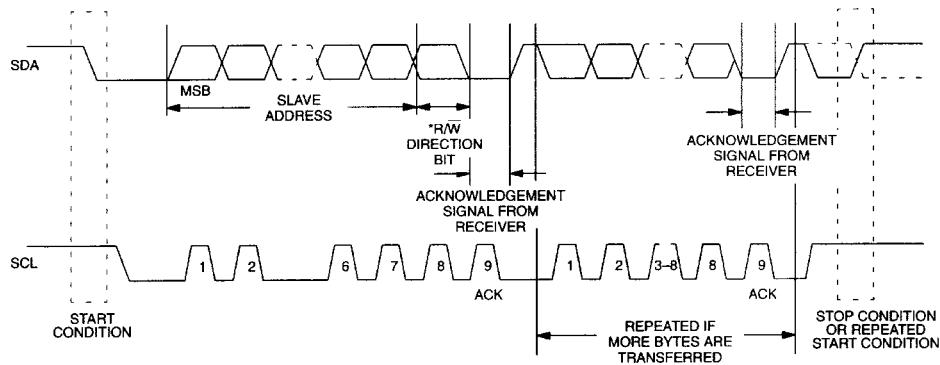
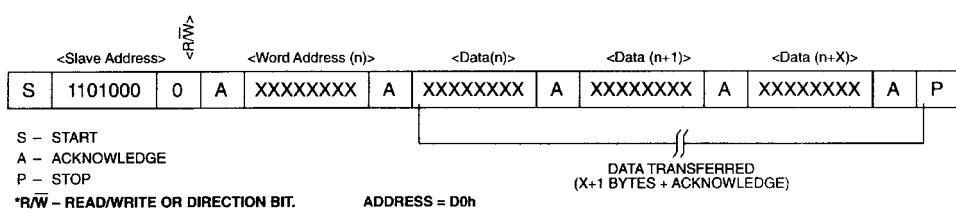
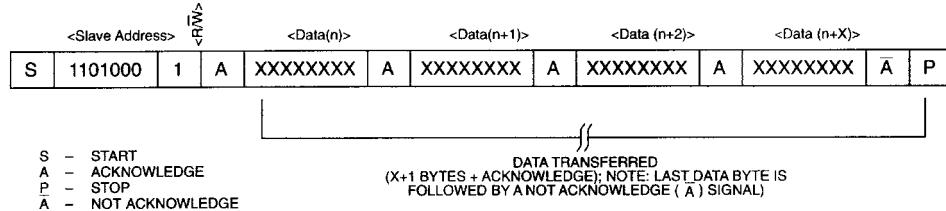
A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Depending upon the state of the R/W bit, two types of data transfer are possible:

- 1) **Data transfer from a master transmitter to a slave receiver.** The master transmits the first byte (the slave address). Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
- 2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, which is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The DS1338 can operate in the following two modes:

- 1) **Slave receiver mode (write mode):** Serial data and clock are received through SDA and SCL. An acknowledge bit is transmitted after each byte is received. START and STOP conditions are recognized as the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit (Figure 6). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1338 address—1101000—followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line. After the DS1338 acknowledges the slave address and write bit, the master transmits a word address to the DS1338. This sets the register pointer on the DS1338, with DS1338 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the DS1338 acknowledging each byte received. The register pointer increments after each byte is transferred. The master generates a STOP condition to terminate the data write.
- 2) **Slave transmitter mode (read mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. The DS1338 transmits serial data on SDA while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 7). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1338 address—1101000—followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line. The DS1338 then starts transmitting data using the register address pointed to by the register pointer. If the register pointer is not set before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The register pointer is incremented after each byte is transferred. The DS1338 must receive a “not acknowledge” to end a read.

**Figure 5. Data Transfer On 2-Wire Serial Bus****Figure 6. Data Write: Slave Receiver Mode****Figure 7. Data Read: Slave Transmitter Mode**

## Package Information

(For the latest package outline information, go to [www.maxim-ic.com/DallasPackInfo](http://www.maxim-ic.com/DallasPackInfo).)