CMOS 8-Bit Microcontroller

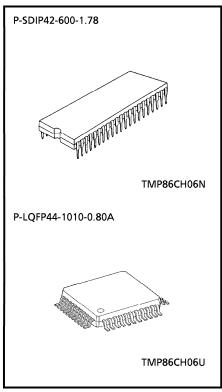
TMP86CH06N/TMP86CH06U

The TMP86CH06 is the 8-bit single chip microcomputer, which contains ROM, RAM, multi-function timer/counters, serial interface (UART/SIO) with high speed, high performance and low power consumption.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CH06N	16K × 8-bit	E120 hit	P-SDIP42-600-1.78	TMP86PH06N
TMP86CH06U	10K X 0-DIL	512 × 8-bit	P-LQFP44-1010-0.80A	TMP86PH06U

Features

- ♦ 8-bit single chip microcomputer TLCS-870/C Series
- Minimum Instruction execution time: $0.25 \mu s$ (at 16.0 MHz)
 - Power consumption is reducible by means of conversion of instruction execution time 0.25 μ s, 0.50 μ s, 1.0 μ s, 2.0 μ s, 4.0 μ s, 8.0 μ s, 122 μ s (at 16.0 MHz, 32.768 kHz operation)
- ◆ External Bus Interface
 - up to 64 Kbytes (for both Program and Data memory)
 - Multiplexed between Lower Address-bus and Data-bus
- ♦ 21 Interrupt factors (6 for External, 15 for Internal)
- ◆ Input/Output Ports: 35 pins
 - High-Current Output (Typ. 20 mA, LED direct drive): 8 pins
- ◆ 16-bit Timer/Counter: 1 channel
 - Timer, Event counter, Pulse Width measurement and External-triggered timer



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• For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

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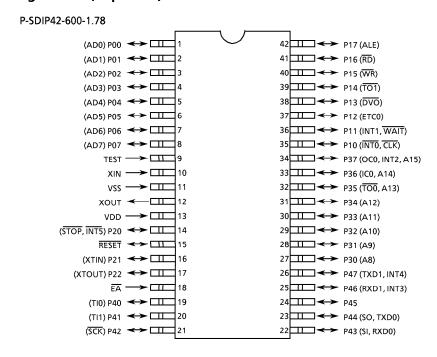
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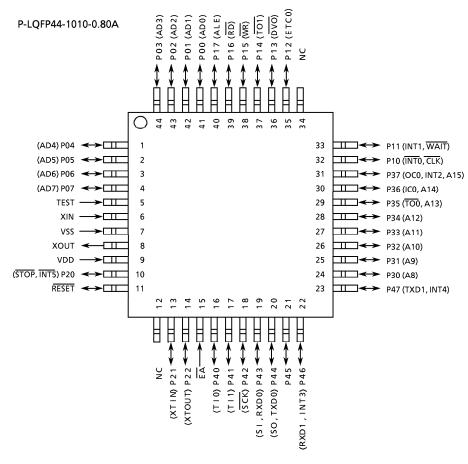
86CH06-1 2002-10-08

- ◆ 8-bit Timer/Counter: 2 channels
 - Available for 16-bit timer by cascade connection
 - Timer, Event counter, Pulse Width Modulation, Programmed Pulse Generator and Programmable Divider Output, Warming-up Counter
- ♦ Serial Interface
 - 8-bit UART: 2 channels
 - 8-bit SIO (synchronized): 1 channel
- ◆ Clock Oscillation circuit: 2 units
 - For Single or Dual clock mode
- ◆ Nine power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
 - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
 - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-
 - Timer. Release by falling edge of TBTCR < TBTCK > setting.
 - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by
 - interruputs.
 - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release
 - by interruputs.
 - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-
 - Timer. Release by falling edge of TBTCR < TBTCK > setting.
 - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by
 - interrupts.
 - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release
 - by interrupts.
- ◆ Operating Voltage: 4.5 to 5.5 V at 16.0 MHz/32.768 kHz, 2.7 to 5.5 V at 8 MHz/32.768 kHz,
 - 1.8 to 5.5 V at 4.2 MHz/32.768 kHz.

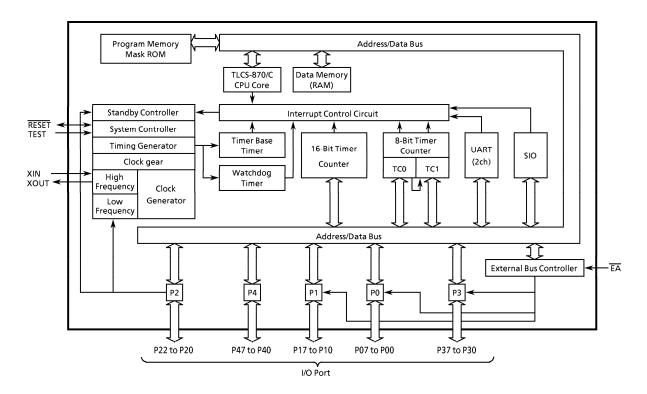
86CH06-2 2002-10-08

Pin Assignments (Top View)





Block Diagram



Pin Names And Functions (1/3)

Pin Name	No. of Pins	Input/Output	Functions
P00 to P07 AD0 to AD7	8	I/O 3-states	Port 0: 8-bit I/O port that allows selection of input/output on bit basis. Address/Data bus: Functions as 8-bit bidirectional address/data bus for external memory (TTL input).
P10 INTO CLK	1	I/O Input Output	Port 10: I/O port that allows selection of input/output on bit basis. External Interrupt Request 0 Clock: Clock output (Schmidt Input)
P11 INT1 WAIT	1	I/O Input Input	Port 11: I/O port that allows selection of input/output on bit basis. External Interrupt Request 1 Wait: Wait request from external Memory (Schmidt Input)
P12 ETC0	1	I/O Input	Port 12: I/O port that allows selection of input/output on bit basis. Extended Timer Input 0 (Schmidt Input)
P13	1	I/O Output	Port 13: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Divider Output
P14	1	1/0	Port 14: I/O port that allows selection of input/output on bit basis. (Schmidt Input)
P15	1	Output I/O	8-bit Timer 1 Output Port 15: I/O port that allows selection of input/output on bit basis. (Schmidt Input)
P16	1	Output I/O	Write: Generates strobe signal to write data on External Memory. Port 16: I/O port that allows selection of input/output on bit basis. (Schmidt Input)
RD P17		Output I/O	Read: Generates strobe signal to read data from External Memory. Port 17: I/O port that allows selection of input/output on bit basis.
ALE	1	Output	(Schmidt Input) Address Latch Enable: The negative edge of ALE supplies an address latch timing on AD0 to AD7 for External Memory.
P20 STOP	1	I/O Input	Port 20: I/O port that allows selection of input/output on bit basis. Open-Drain Output. STOP Releasing: The rising edge or High Level (Schmidt Input)
ĪNT5		Input	Releases STOP mode. External Interrupt Request 5
P21	1	I/O	Port 21: I/O port that allows selection of input/output on bit basis. Open-Drain Output. (Schmidt Input)
P22	1	Input I/O	Port 22: I/O port that allows selection of input/output on bit basis. Open-Drain Output. (Schmidt Input)
хтоит		Output	Low Frequency Clock Output
P30 to P34	5	1/0	Port 30 to 34: I/O port that allows selection of input/output on bit basis. (Schmidt Input)
A8 to A12		Output	Address Bus 8 to 12

Pin Names And Functions (2/3)

Pin Name	No. of Pins	Input/Output	Functions
P35		I/O	Port 35: I/O port that allows selection of input/output on bit basis. (Schmidt Input)
TO0 A13	1	Output Output	8-bit Timer Output 0 Address Bus 13
P36 IC0 A14	1	I/O Input Output	Port 36: I/O port that allows selection of input/output on bit basis. Capture Input 0 for Extended Timer Address Bus 14
P37		1/0	Port 37: I/O port that allows selection of input/output on bit basis. (Schmidt Input)
OC0 INT2 A15	1	Output Input Output	Output Compare 0 for Extended Timer External Interrupt Request 2 (Schmidt Input) Address Bus 15
P40	1	I/O	Port 40: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. 8-bit Timer Input 0 (Schmidt Input)
P41	1	I/O	Port 41: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. 8-bit Timer Input 1
P42	1	1/0	Port 42: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. Clock input/output for SIO (Schmidt Input)
P43 SI, RXD0	1	I/O Input	Port 43: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. Data Input for UART/SIO channel 0
P44	1	I/O	Port 44: I/O port that allows selection of input/output on bit basis. (Schmidt Input)
SO, TXD0 P45	1	Output I/O	Data Output for UART/SIO channel 0. Programmable Open-Drain Output. Port 45: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output.
P46 RXD1 INT3	1	I/O Input Input	Port 46: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. Data Input for UART channel 1 External Interrupt Request 3
P47 TXD1 INT4	1	I/O Output Input	Port 47: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Data Output for UART channel 1. Programmable Open-Drain Output. External Interrupt Request 4 (Schmidt Input)

Pin Names And Functions (3/3)

Pin Name	No. of Pins	Input/Output	Functions
ĒĀ	1	Input	External Access: Fix to HIGH level to utilize internal ROM. Fix to LOW level to utilize external memory.
TEST	1	Input	to be fixed to LOW level
RESET	1	I/O	RESET signal input or watchdog timer output/address trap output/system-clock-reset-output
XIN/XOUT	2	1/0	High-frequency resonator is to be connected.
VSS	1	Input	Ground
VDD	1	Input	Power Supply

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Maps

The TMP86CH06 memory consists of 3 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64K-byte address space. Figure 1-1 shows the TMP86CH06 memory address maps. The general-purpose register banks are not assigned to the RAM address space.

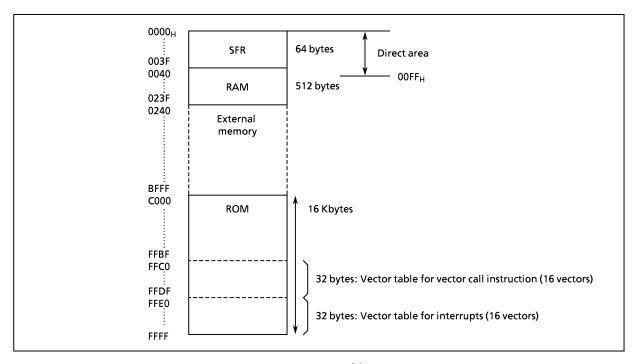


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86CH06 can address up to 64 Kbytes of external program memory space except the SFR area and the internal RAM. However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap). The TMP86CH06 contains a 16-Kbyte program memory (mask ROM) at addresses from $C000_{\rm H}$ to $FFFF_{\rm H}$.

1.3 Data Memory (RAM)

The TMP86CH06 is available up to 64 Kbytes of data memory area. Data memory consists of internal data memory (internal ROM or RAM) and external data memory (ROM or RAM). The TMP86CH06 has 512 bytes of internal RAM. The first 192 bytes ($0040_{\rm H}$ to $00FF_{\rm H}$) of the internal RAM are located in the direct area; instructions with shorten operations are available against such an area.

Electrical Characteristics

Absolute Maximum Rating (V_{ss} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	
Input Voltage	V_{IN}		– 0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT}		– 0.3 to V _{DD} + 0.3	
	I _{OUT1}	P1 to P4	3.2	
Output Current	I _{OUT3}	P0	30	mA
	Σ l _{OUT1}		80] ''"
Output Current	Σ I _{OUT3}		120	
2 2 4 4 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		TMP86CH06N	600	
Power Dissipation (Topr = 85°C)	PD	тмр86сн060	350	mW
Soldering Temperature (Time)	Tsld		260 (10 s)	
Storage Temperature	Tstg		– 55 to 125	°c
Operating Temperature	Topr		- 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins		Conditions	Min	Max	Unit
			fc = 16	NORMAL1, 2 mode			
			MHz	IDLE0, 1, 2 mode	4.5		
			fc = 8	NORMAL1, 2 mode			
			MHz	IDLE0, 1, 2 mode	2.7		
Supply Voltage	V_{DD}		fc = 4.2	NORMAL1, 2 mode		5.5	l _v l
	- 55		MHz	IDLE0, 1, 2 mode	1.8		
			fs = 32.768	SLOW1, 2 mode] "		
			kHz	SLEEP0, 1, 2 mode			
				STOP mode	1.8		
	V _{IH1}	Except hysteresis and TTL input	- V _{DD} ≧ 4.5 V		$V_{DD} \times 0.70$		
	V _{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
Input High Voltage	V _{IH3}	Except TTL input		V_{DD} < 4.5 V	$V_{DD} \times 0.90$	V_{DD}	V
	V_{IH4}	TTL input (Data bus)	V _{DD} = 5 V		2.2]	
	$V_{\text{IH}5}$			$V_{DD} = 1.8 V$	V _{DD} – 0.2		
	V_{IL1}	Except hysteresis and TTL input		$V_{DD} \ge 4.5 V$		$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input		V DD = 4.5 V		$V_{DD} \times 0.25$	
Input Low Voltage	V_{IL3}	Except TLL input		V _{DD} < 4.5 V	0	$V_{DD} \times 0.10$	V
	V_{IL4}	TTL input (Data bus)		$V_{DD} = 5 V$		0.8	
	V_{IL5}			V _{DD} = 1.8 V		0.2	
				$V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$		16	
Clock Frequency	fc	XIN, XOUT		V _{DD} = 2.7 V to 5.5 V		8	MHz
Clock Frequency			V _{DD} = 1.8 V to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock Frequency fc; The condition of supply voltage range is the value under NORMAL1/2 and IDLE0/1/2 mode.

Note 3: The minimum fc with clock gear is calculated as following formula with the ratio on divider n.

(Min fc) = (ratio on divider n) \times 1 [MHz]

DC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input		_	0.9	-	٧
	I _{IN1}	TEST, EA	V 55V				
Input Current	I _{IN2}	Sink Open Drain, Tri-state Port	$V_{DD} = 5.5 V$	_	_	± 2	μΑ
	I _{IN3}	RESET, STOP	$V_{IN} = 5.5 \text{ V/0 V}$				
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ
input Resistance	R _{IN3}	TEST		_	70	-	K22
OSC. Feedback	Rfx	XIN-XOUT		_	1.2	-	
Resistance	Rfxt	XTIN-XTOUT		_	6	-	ΜΩ
Output Leakage	I _{LO1}	Sink Open Drain Port	$V_{DD} = 5.5 \text{ V}, V_{OUT} = 5.5 \text{ V}$	_	-	2	
Current	I _{LO2}	Tri-state Port	$V_{DD} = 5.5 \text{ V}, \ V_{OUT} = 5.5 \text{ V}/0 \text{ V}$	_	-	± 2	μΑ
"H" Output Voltage	V _{OH2}	Tri-state Port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	-	-	V
"L" Output Voltage	V _{OL3}	Except P0 and XOUT	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	-	0.4	V
#U# Q :	I _{OL1}	Except P0 and XOUT	$V_{DD} = 4.5 \text{ V}, V_{OL} = 0.4 \text{ V}$	1.6	-	-	mA
"L" Output Current	I _{OL3}	P0	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$	- 20		_	IIIA
Supply Current under			V _{DD} = 5.5 V		5.5	7.0	
NORMAL1, 2 mode			V _{IN} = 5.3 V/0.2 V	_	3.5	7.0	
Supply Current under			fc = 16 MHz		2.8	3.5	mA
IDLE1, 2 mode			fs = 32.768 kHz	-	2.8	3.3	
Supply Current under			V _{DD} = 5.5 V		4.0	5.0	
NORMAL1, 2 mode			V _{IN} = 5.3 V/0.2 V	_	4.0	3.0	
Supply Current under			fc = 8 MHz		2.0	2.5	mA
IDLE1, 2 mode] ,		fs = 32.768 kHz	_	2.0	2.5	
Supply Current under	I _{DD}				14	25	_
SLOW1 mode			\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	_	14	25	μΑ
Supply Current under			$V_{DD} = 3.0 \text{ V}$		7.0	4.5	
SLEEP1 mode			$V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$ fs = 32.768 kHz		7.0	15	μΑ
Supply Current under]		15 = 32./08 KHZ		6.0	15	
SLEEP0 mode				-	6.0	15	μA
Supply Current under			V _{DD} = 5.5 V		۸.	10	
STOP mode			V _{IN} = 5.3 V/0.2 V	-	0.5	10	μA

Note 1: Typical values are shown under $T_{opr} = 25$ °C, $V_{DD} = 5$ V, while conditions are not stated. Note 2: Input current I_{IN1} , I_{IN3} : The current through pull-up or pull-down resistor is not included.

AC Characteristics

(1) $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

① CLOCK

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
		NORMAL1, 2 mode	0.25		4	
Machine Cycle Time	+0.4	IDLE0, 1, 2 mode	0.25	1	4	
Machine Cycle Time	tcy	SLOW1, 2 mode	117.6		122.2	μ S
		SLEEP0, 1, 2 mode	117.6	_	133.3	
High Level Clock Pulse Width	t _{WCH}	External clock operation (XIN input)	25			200
Low Level Clock Pulse Width	t _{WCL}	fc = 16 MHz	25	ı	1	ns
High Level Clock Pulse Width	t _{WSH}	External clock operation (XTIN input)	14.7			
Low Level Clock Pulse Width	t _{WSL}	fs = 32.768 kHz	14.7	-	_	μS

② External Memory Interface (Multiplexed Bus) at $V_{DD} = 4.5$ to 5.5

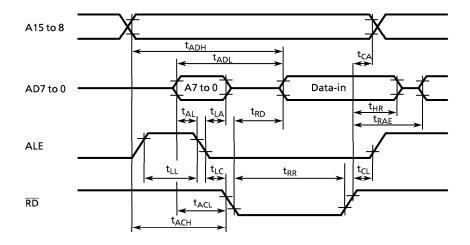
Na	Cumple of	Do no monto n	Vari	able	16 N	ЛHz	Unit
No.	Symbol	Parameter	Min	Max	Min	Max	Unit
1	t _{AL}	A7 to 0 effective → ALE	0.5t – 15		16		ns
2	t _{LA}	ALE fall → A7 to 0 hold	0.5t – 20		11		ns
3	t _{LL}	ALE pulse width	t – 40		22		ns
4	t _{LC}	ALE fall → RD, WR fall	0.5t – 25		6		ns
5	t _{CL}	RD, WR rise → ALE rise	0.5t – 20		11		ns
6	t _{ACL}	A7 to 0 effective $\rightarrow \overline{RD}$, \overline{WR} fall	A7 to 0 effective $\rightarrow \overline{RD}$, \overline{WR} fall $t-25$		37		ns
7	t _{ACH}	A15 to 8 effective $\rightarrow \overline{RD}$, \overline{WR} fall	1.5t – 25		68		ns
8	t _{CA}	\overline{RD} , \overline{WR} rise \rightarrow A15 to 8 hold	0.5t – 20		11		ns
9	t _{ADL}	A7 to 0 effective \rightarrow D7 to 0 input		3t – 55		132	ns
10	t _{ADH}	A15 to 8 effective \rightarrow D7 to 0 input		3.5t – 65		153	ns
11	t _{RD}	\overline{RD} fall \rightarrow D7 to 0 input		2t – 60		65	ns
12	t _{RR}	RD pulse width	2t – 40		85		ns
13	t _{HR}	\overline{RD} rise \rightarrow D7 to 0 hold	0		0		ns
14	t _{RAE}	\overline{RD} rise \rightarrow A7 to 0 effective	t – 15		47		ns
15	t _{WW}	WR pulse width	2t – 40		85		ns
16	t _{DW}	D7 to 0 effective → WR rise	2t – 40		85		ns
17	t _{WD}	$\overline{\text{WR}}$ rise \rightarrow D7 to 0 hold	0.5t – 15		16		ns

Note: t = tcy/4 (t = 62.5 ns at fcgck = 16 MHz)

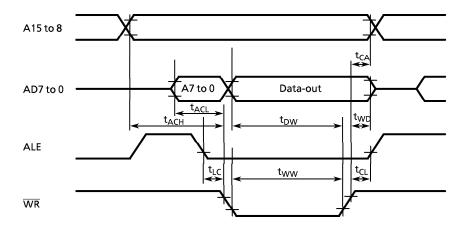
A.C.Measurement Condition

Output Level: High 2.2 V/Low 0.8 V, CL = 50 pFHigh 2.4 V/Low 0.4 V (D7 to D0)
High 0.8 VDD/Low 0.2 VDD (Except D7 to D0) Input Level:

Read Cycle



Write Cycle



Recommended Oscillating Conditions - 1

$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

Danamatan	0 ''' '	Oscillation			Recommended Constant		
Parameter	Oscillator	Frequency	Recom	mended Oscillator	C ₁	C ₂	
			MURATA	CSA16.00MXZ040	10 pF	10 pF	
Lieb francis		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF	
High-frequency Oscillation	Ceramic Resonator	8 IVITIZ		CST8.00MTW	30 pF (built-in)	30 pF (built-in)	
Oscillation		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF	
		4.19 WITZ		CST4.19MGW	30 pF (built-in)	30 pF (built-in)	
Low-frequency	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF	
Oscillation	Crystal Oscillator	32.700 KHZ	ווכ	V 1-200	o pr	o pi	

Recommended Oscillating Conditions - 2

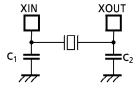
$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

Davamatas	0 111 /	Oscillation			Recommended Constant		
Parameter	Oscillator	Frequency	Recommended Oscillator		C ₁	C ₂	
	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF	
High-frequency		OIVITZ		CST8.00MTW	30 pF (built-in)	30 pF (built-in)	
Oscillation		4.40 8.411	MURATA	CSA4.19MG	30 pF	30 pF	
		4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)	

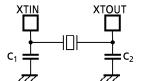
Recommended Oscillating Conditions - 3

$$(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$$

Donomoton	0 ''' 1	Oscillation	Recommended Oscillator		Recommend	ed Constant
Parameter	Oscillator	Frequency			C ₁	C ₂
High-frequency	Caramia Basanatar	4 10 1411-	MURATA	CSA4.19MG	30 pF	30 pF
Oscillation	Ceramic Resonator	4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;

http://www.murata.co.jp/search/index.html