

Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability
- PPAP Capable (Note 4)

Mechanical Data

- Case: SOT563
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.006 grams (Approximate)

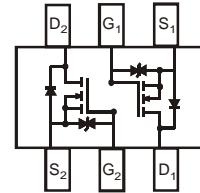


ESD Protected up to 2kV

SOT563



TOP VIEW


 TOP VIEW
 Internal Schematic

Ordering Information (Note 5)

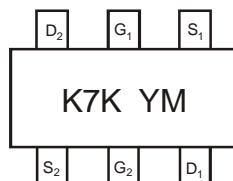
Part Number	Case	Packaging
DMN601VKQ-7	SOT563	3,000/Tape & Reel

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q101 qualified and are PPAP capable. Refer to http://www.diodes.com/product_compliance_definitions.html.
5. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information

SOT563



K7K = Marking Code
 YM = Date Code Marking
 Y = Year (ex: D = 2016)
 M = Month (ex: 9 = September)

Date Code Key

Month	2005	...	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Code	S	...	C	D	E	F	G	H	I	J	K	L
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V_{DSS}	60	V	
Gate-Source Voltage	V_{GSS}	± 20	V	
Drain Current (Note 6)	Continuous Pulsed (Note 7)	I_D	305 800	mA

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

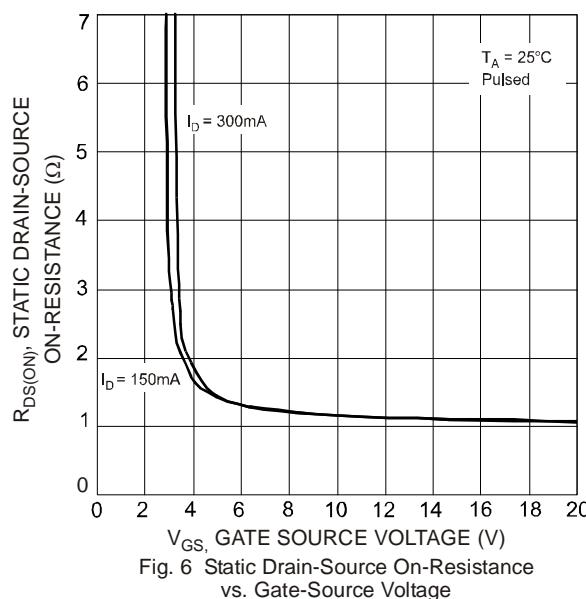
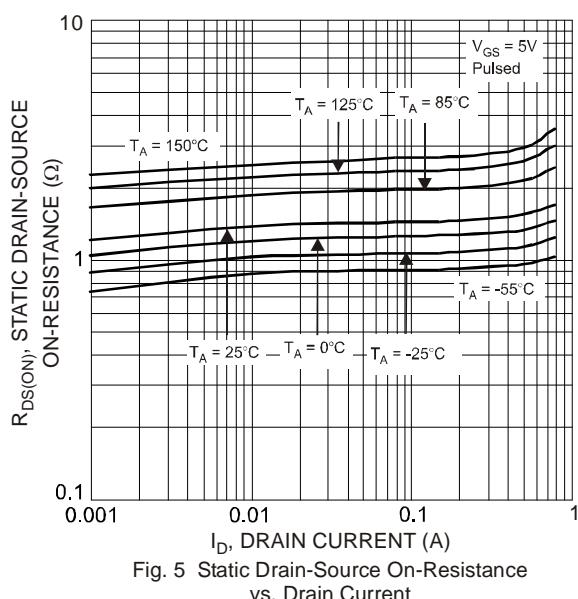
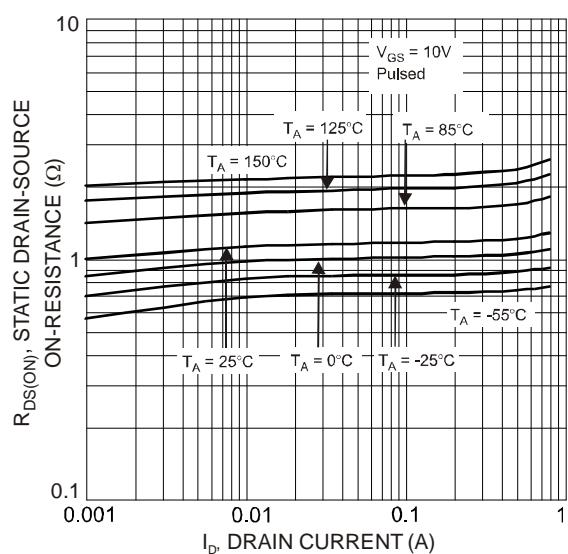
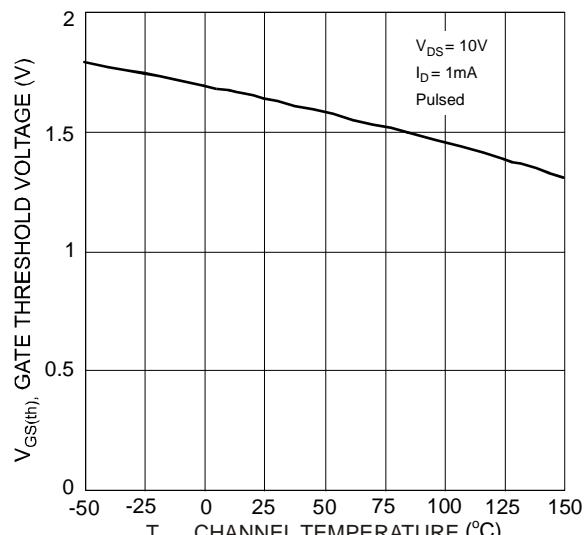
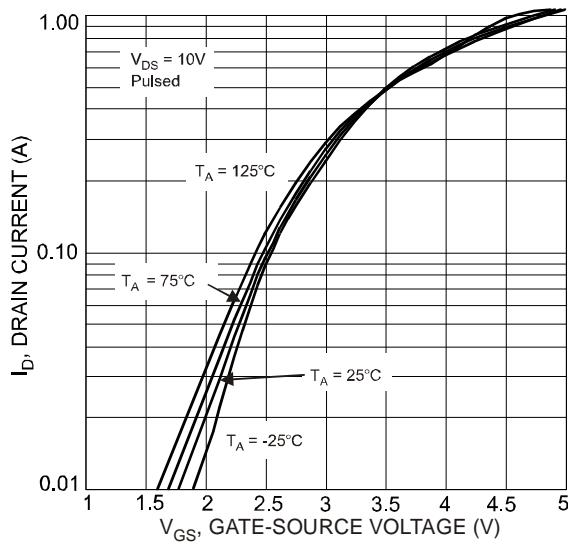
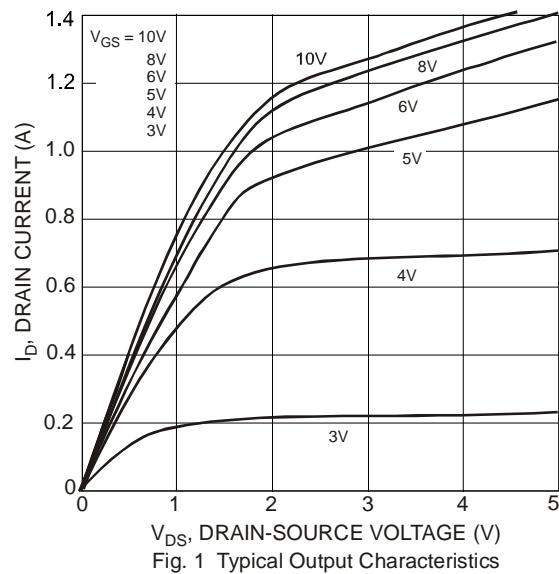
Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P_D	250	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	500	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to +150	°C

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$ unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 10\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	250	nA	$V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 500	nA	$V_{GS} = \pm 10\text{V}$, $V_{DS} = 0\text{V}$
		—	—	± 100	nA	$V_{GS} = \pm 5\text{V}$, $V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.6	2.5	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	—	2.0	Ω	$V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$
		—	—	3.0	Ω	$V_{GS} = 4.5\text{V}$, $I_D = 200\text{mA}$
Forward Transfer Admittance	$ Y_{fs} $	—	284	—	ms	$V_{DS} = 10\text{V}$, $I_D = 0.2\text{A}$
Diode Forward Voltage (Note 8)	V_{SD}	0.5	—	1.4	V	$V_{GS} = 0\text{V}$, $I_S = 115\text{mA}$
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	—	50	pF	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	5.0	pF	

Notes:

6. Device mounted on FR-4 PCB.
7. Pulse width $\leq 10\mu\text{s}$, Duty Cycle $\leq 1\%$.
8. Short duration pulse test used to minimize self-heating effect.



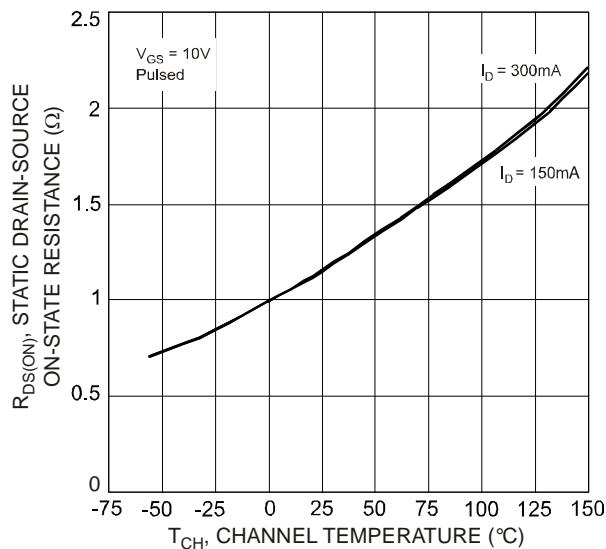


Fig. 7 Static Drain-Source On-State Resistance vs. Channel Temperature

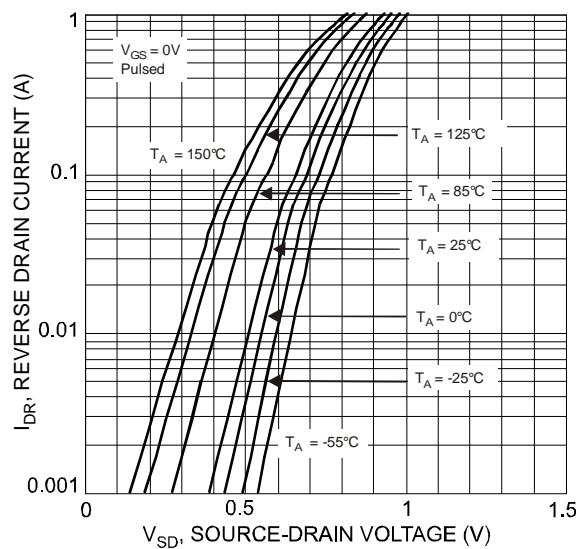


Fig. 8 Reverse Drain Current vs. Source-Drain Voltage

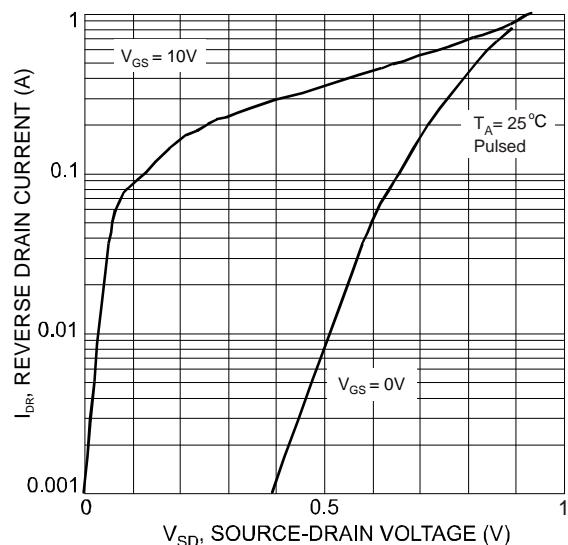


Fig. 9 Reverse Drain Current vs. Source-Drain Voltage

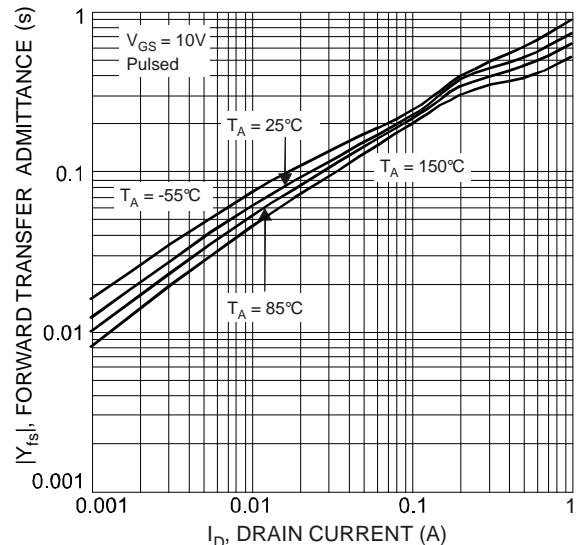
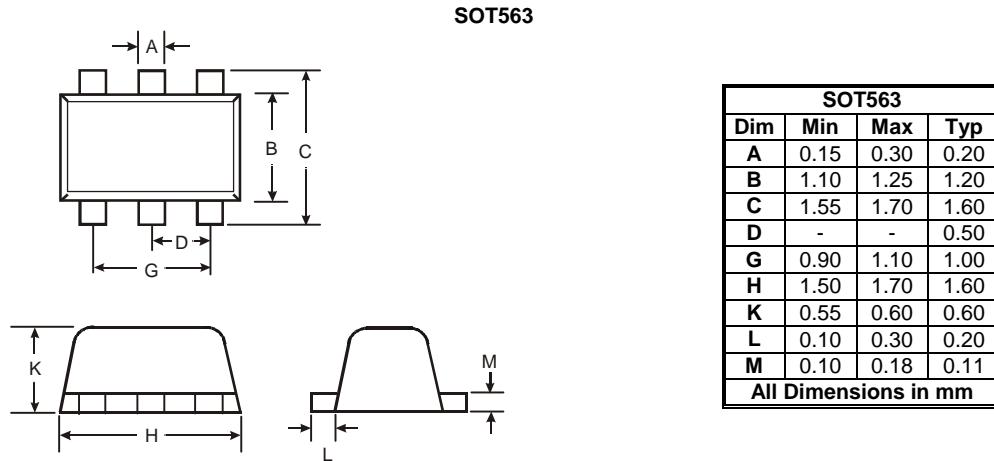


Fig. 10 Forward Transfer Admittance vs. Drain Current

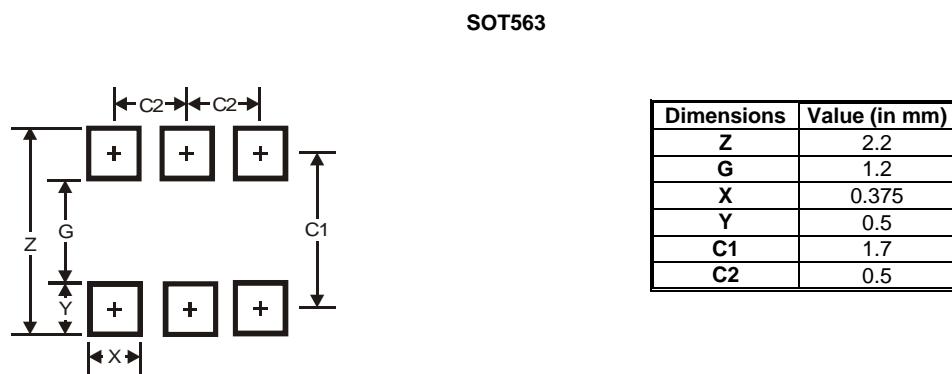
Package Outline Dimensions

Please see AP02001 at http://www.diodes.com/_files/datasheets/ap02001.pdf for the latest version.



Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/_files/datasheets/ap02001.pdf for the latest version.



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