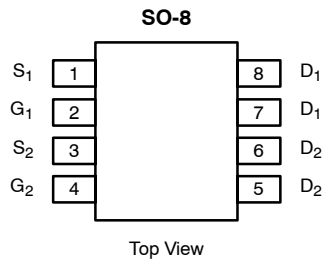


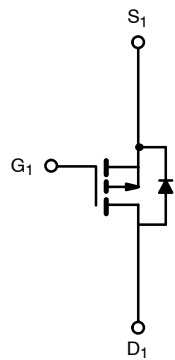


Dual P-Channel 60-V (D-S) 175° MOSFET

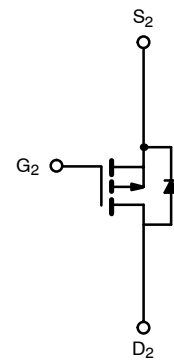
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-60	0.120 @ $V_{GS} = -10$ V	-3.1
	0.150 @ $V_{GS} = -4.5$ V	-2.8



Ordering Information: Si4948BEY—E3 (Lead Free)
Si4948BEY-T1—E3 (Lead Free with Tape and Reel)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	10 secs	Steady State
Drain-Source Voltage		V_{DS}	-60	
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	-3.1	-2.4
	$T_A = 70^\circ\text{C}$		-2.6	-2.0
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	-25	
Continuous Source Current (Diode Conduction) ^a		I_S	-2	-1.1
Avalanche Current		I_{AS}	15	
Single Pulse Avalanche Energy		E_{AS}	11	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.4	1.4
	$T_A = 70^\circ\text{C}$		1.7	0.95
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Typical	Maximum
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	53	62.5
	Steady State		85	110
Maximum Junction-to-Foot	Steady State	R_{thJF}	30	37

Notes

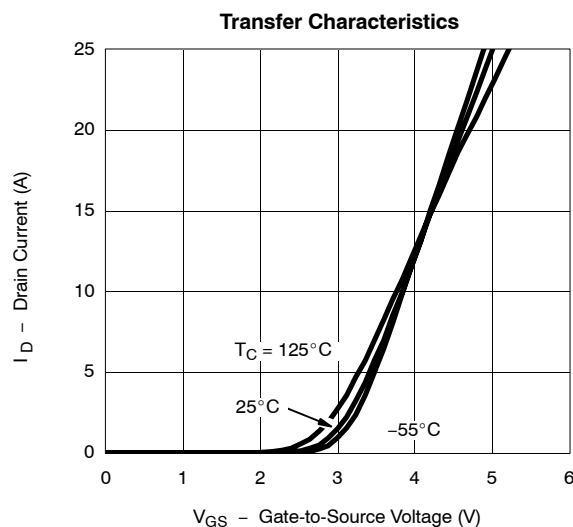
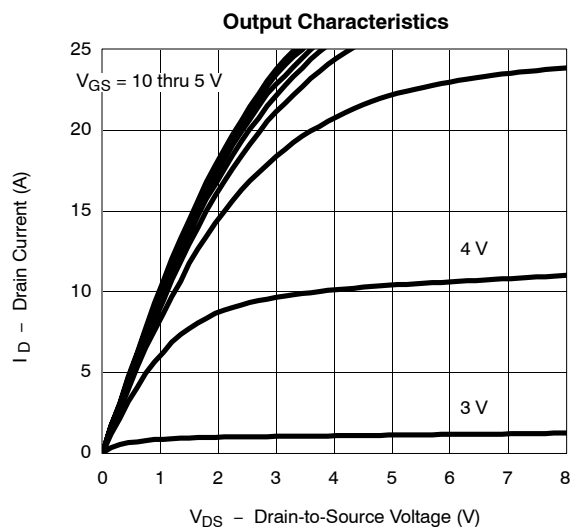
a. Surface Mounted on 1" x 1" FR4 Board.

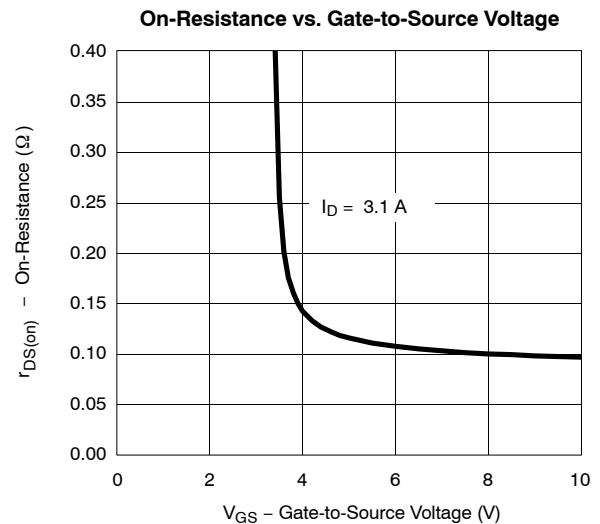
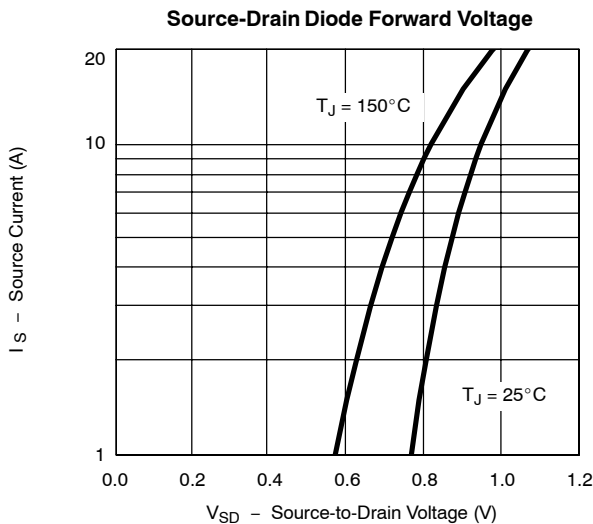
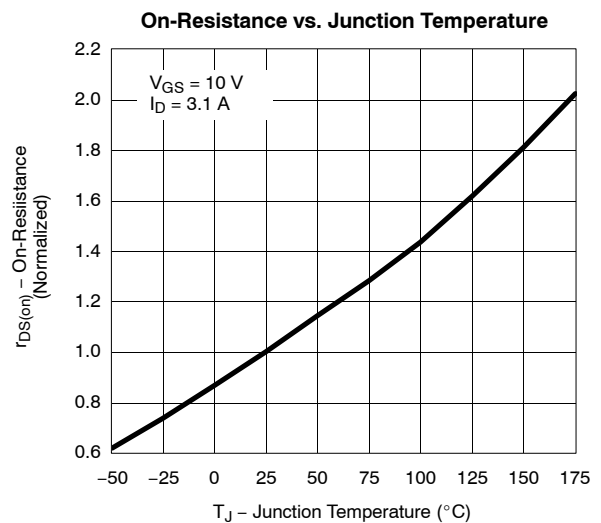
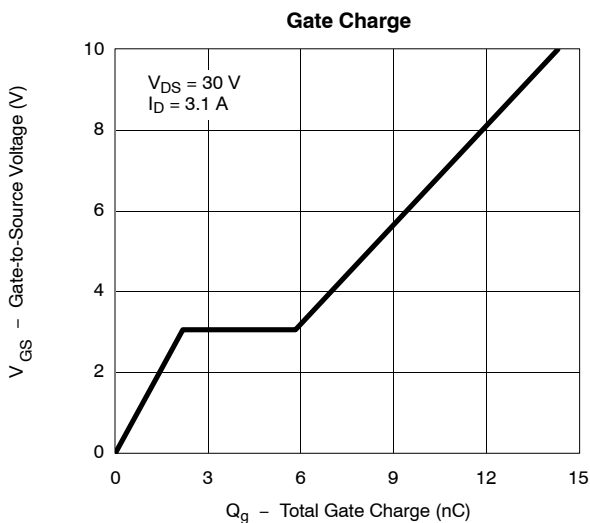
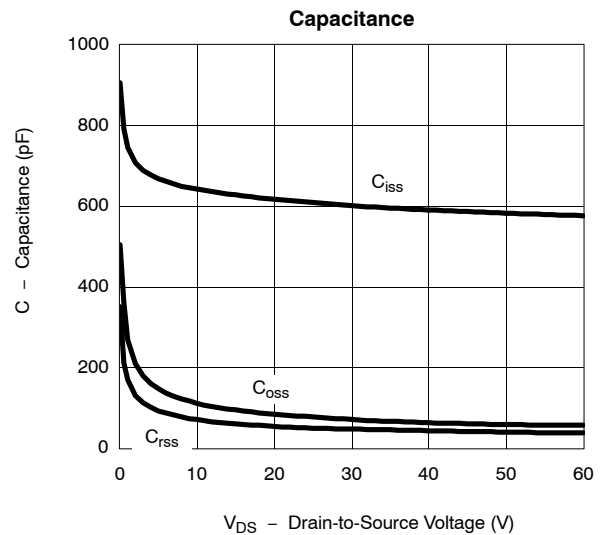
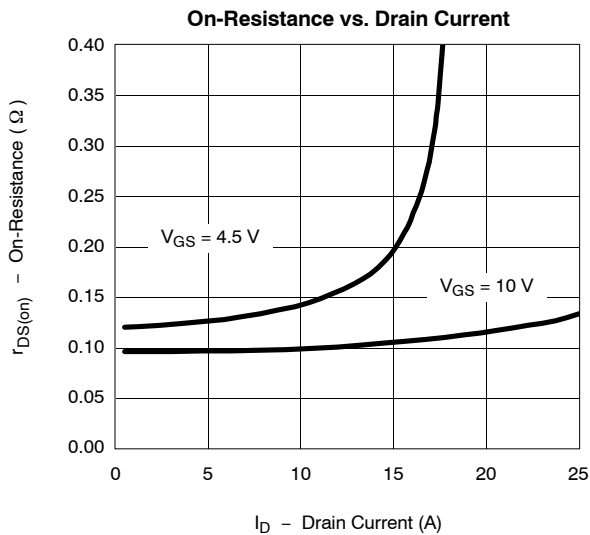
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

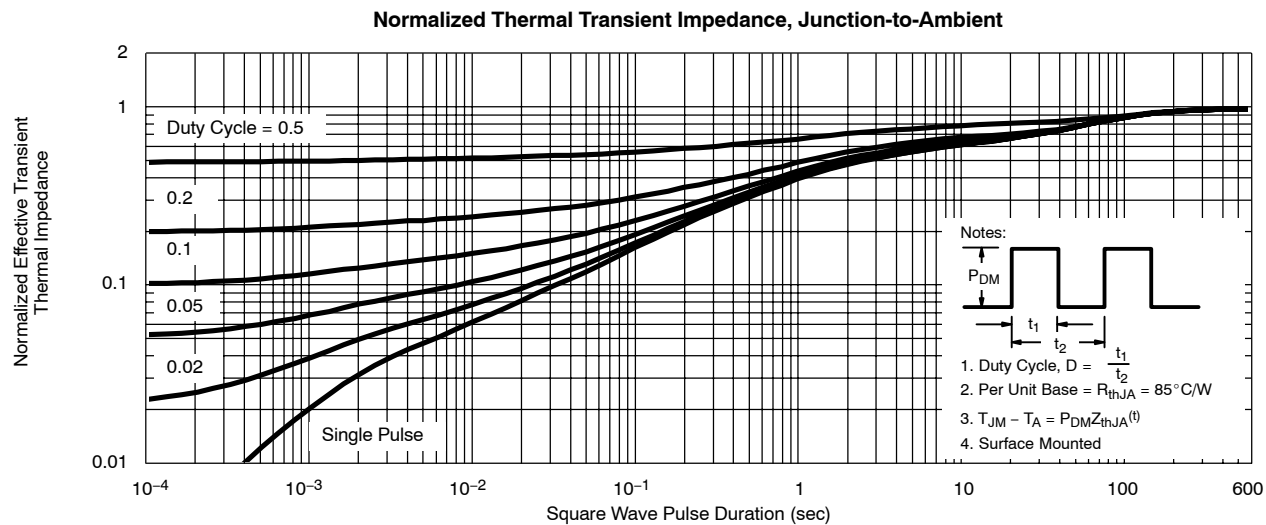
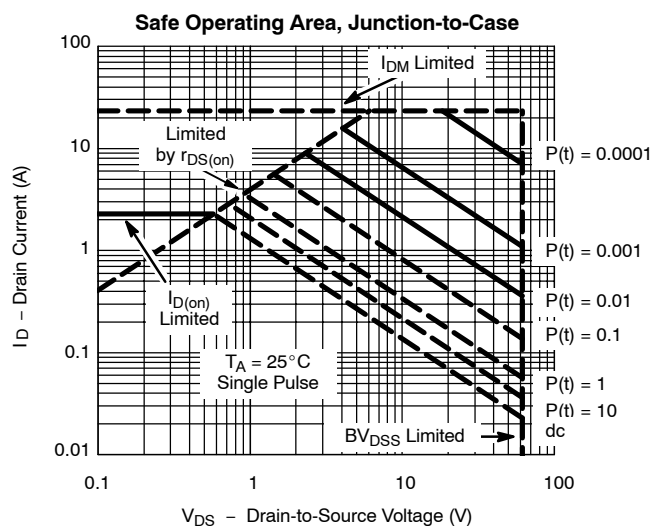
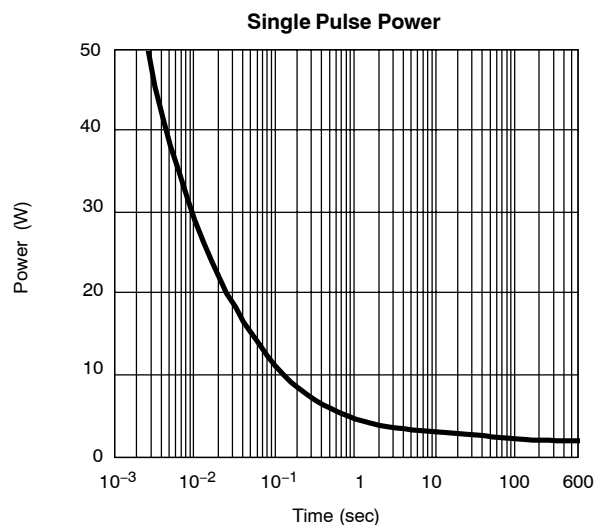
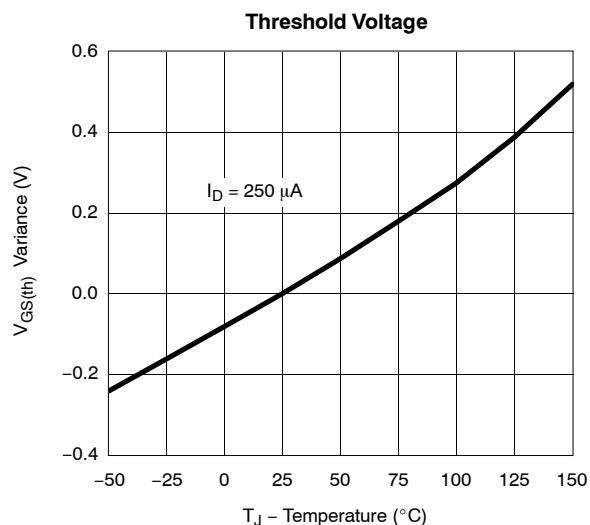
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-1		-3	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -60\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}$, $V_{GS} = -10\ \text{V}$	-25			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}$, $I_D = -3.1\ \text{A}$		0.100	0.120	Ω
		$V_{GS} = -4.5\ \text{V}$, $I_D = -0.2\ \text{A}$		0.126	0.150	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}$, $I_D = -3.1\ \text{A}$		8.5		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -30\ \text{V}$, $V_{GS} = -10\ \text{V}$, $I_D = -3.1\ \text{A}$		14.5	22	nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			3.7		
Gate Resistance	R_g	$f = 1\ \text{MHz}$		14		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30\ \text{V}$, $R_L = 30\ \Omega$ $I_D \cong -1\ \text{A}$, $V_{GEN} = -10\ \text{V}$, $R_g = 6\ \Omega$		10	15	ns
Rise Time	t_r			15	22	
Turn-Off Delay Time	$t_{d(off)}$			50	75	
Fall Time	t_f			35	55	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		30	50	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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