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FAIRCHILD

August 2010

FSEZ2037 — Low-Power Green-Mode EZ-PSR without Secondary Feedback (CC)

Features

- Linearly Decreasing PWM Frequency
- Green Mode Under Light-load and Zero-load Conditions
- Constant Current (CC) without Secondary-Feedback Circuitry
- Low Startup Current: 8µA
- Low Operating Current: 3.6mA
- Leading-Edge Blanking
- Constant Power Limit
- Universal AC Input Range
- Synchronized Slope Compensation
- 140°C OTP Sensor with Hysteresis
- V_{DD} Over-Voltage Protection (Auto Restart)
- Cycle-by-Cycle Current Limiting
- Under-Voltage Lockout (UVLO)
- Fixed PWM Frequency with Hopping
- Gate Output Maximum Voltage Clamped at 17V

Applications

General-purpose switching-mode power supplies (SMPS) and flyback power converters, such as:

- Battery Chargers for Cellular Phones, Cordless Phones, PDAs, Digital Cameras, Power Tools
- Power Adapters for Ink Jet Printers, Video Game Consoles, Portable Audio Players
- Open-Frame SMPS for TV/DVD Standby and Auxiliary Supplies, Home Appliances, Consumer Electronics
- Replacement for Linear Transformers and RCC SMPS
- PC 5V Standby Power

Description

This highly integrated PWM controller provides several features to enhance the performance of low-power flyback converters. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load and zero-load conditions. This green mode enables the power supply to meet international power conservation requirements. Another advantage is typical startup current of only 8µA, while the typical operating current can be as low as 3.6mA. A large startup resistance can be used to achieve even higher power conversion efficiency.

FSEZ2037 integrates a frequency-hopping function internally to reduce EMI emissions with minimum line filters. Built-in synchronized slope compensation maintains the stability of peak current-mode control. Proprietary internal compensation ensures constant output power limiting over a universal range of AC input voltages, from $90V_{AC}$ to $264V_{AC}$.

The FSEZ2037 provides many protection functions. Pulse-by-pulse current limiting ensures constant output current, even if a short circuit occurs. The internal protection circuit disables PWM output if V_{DD} exceeds 24.5V. The gate output is clamped at 17V to protect the power MOS from over-voltage damage. The built-in over-temperature protection (OTP) function shuts down the controller at 140°C with a 30°C hysteresis.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FSEZ2037NY	-40°C to +105°C	8-Lead, Dual-Outline Package (DIP-8)	Tube

Application Diagram

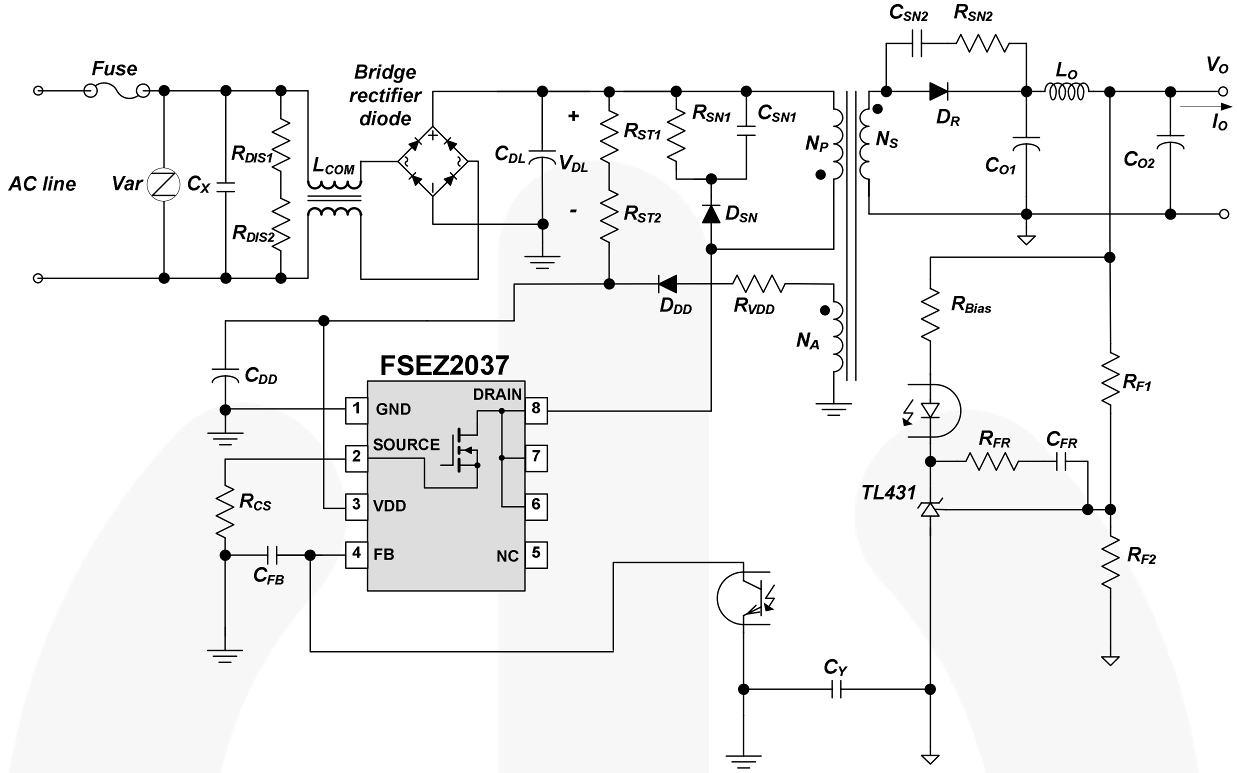


Figure 1. Typical Application

Internal Block Diagram

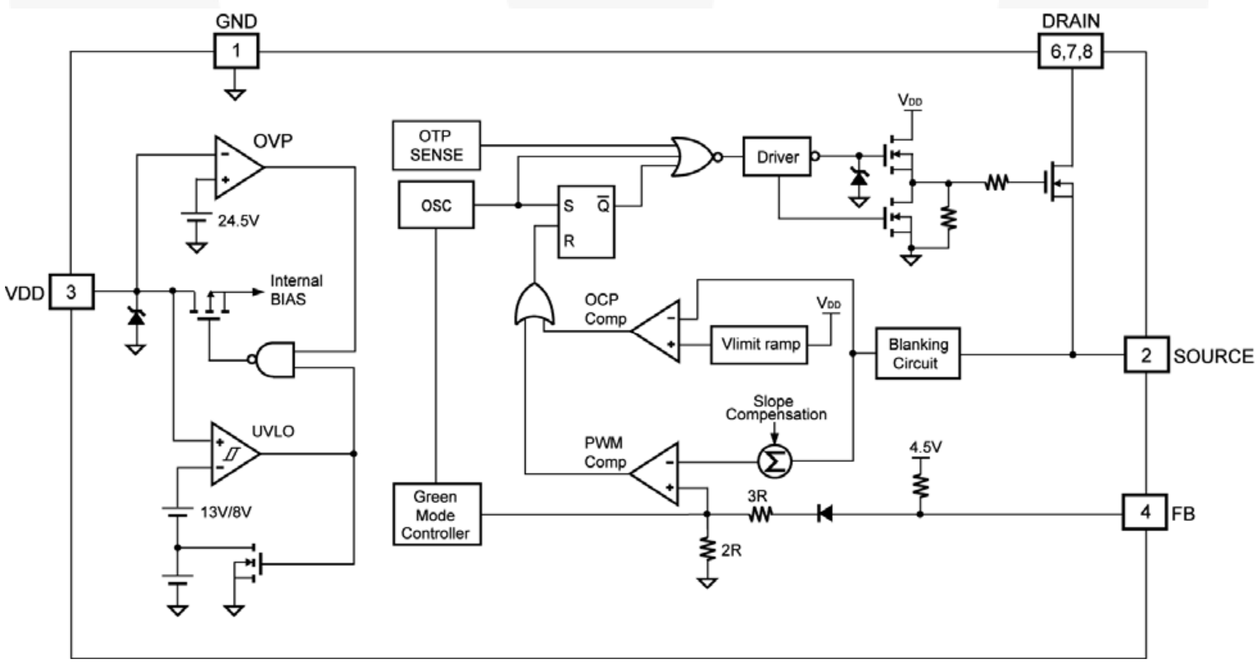
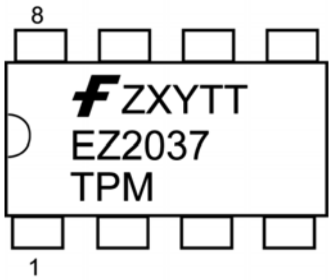


Figure 2. Functional Block Diagram

Marking Information



F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 1-Digit Week Code
TT – 2-Digit Die-Run Code
T – Package Type (N: DIP)
P – Y: Green Package
M – Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

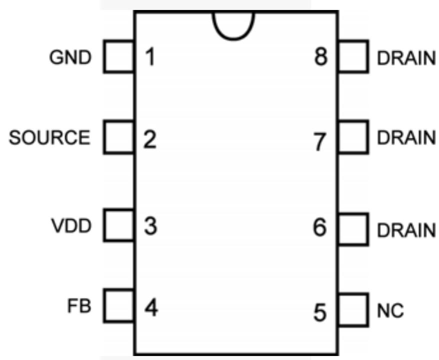


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	Ground
2	SOURCE	Power MOSFET source. This is the high-voltage power MOSFET source.
3	VDD	Power supply
4	FB	The FB pin provides feedback information to the internal PWM comparator. This feedback is used to control the duty cycle. When no feedback is provided, this pin is left open.
5	NC	No connection
6,7,8	DRAIN	Power MOSFET drain. This is the high-voltage power MOSFET drain.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage[1,2]			30	V
V_{FB}	Input Voltage to FB Pin		-0.3	7.0	V
V_{SENSE}	Input Voltage to Sense Pin		-0.3	7.0	V
P_D	Power Dissipation (T_A=25°C)			1.2	W
θ_{JA}	Thermal Resistance (Junction-to-Air)			80	°C/W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin	Human Body Model (JEDEC:JESD22_A114)		3.5	KV
		Charged Device Model (JEDEC:JESD22_C101)		1.0	

Notes:
1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Electrical Characteristics

Unless otherwise noted, V_{DD}=15V and T_A=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-OP}	Continuously Operation Voltage				23.5	V
V_{DD-ON}	Turn-on Threshold Voltage		12	13	14	V
V_{DD-OFF}	Turn-off Threshold Voltage		7.5	8.0	8.5	V
I_{DD-ST}	Startup Current	V_{DD}=V_{DD-ON} – 0.1V		8	20	μA
I_{DD-OP}	Operating Supply Current	C_L=1nF		3.6	4.6	mA
$V_{DD-G\ OFF}$	V_{DD} Low-threshold Voltage to Exit Green-off Mode			V_{DD-OFF} +1.25		V
V_{DD-OVP}	V_{DD} Over-voltage Protection		23.5	24.5	25.5	V
$t_{D-VDDOVP}$	V_{DD} Over-voltage Protection Debounce Time		70	135	200	μs
Feedback Input Section						
A_V	Input-Voltage to Current-Sense Attenuation			0.35		V/V
Z_{FB}	Input Impedance	I_{FB}=0.1mA to 0.2mA		4.6		kΩ
$V_{FB-OPEN}$	Open-Loop Voltage		4.5			V
Current-Sense Section						
t_{PD}	Propagation Delay			100	150	ns
V_{STHVA}	Current Limit Valley Threshold Voltage	V_{DD}=18V		0.81		V
		V_{DD}=15V		0.73		V
		V_{DD}=10V		0.58		V
V_{STHFL}	Current Limit Flat Threshold Voltage	V_{DD}=18V		1.10		V
		V_{DD}=15V		1.01		V
		V_{DD}=10V		0.81		V
t_{LEB}	Leading-Edge Blanking Time		260	330	400	ns

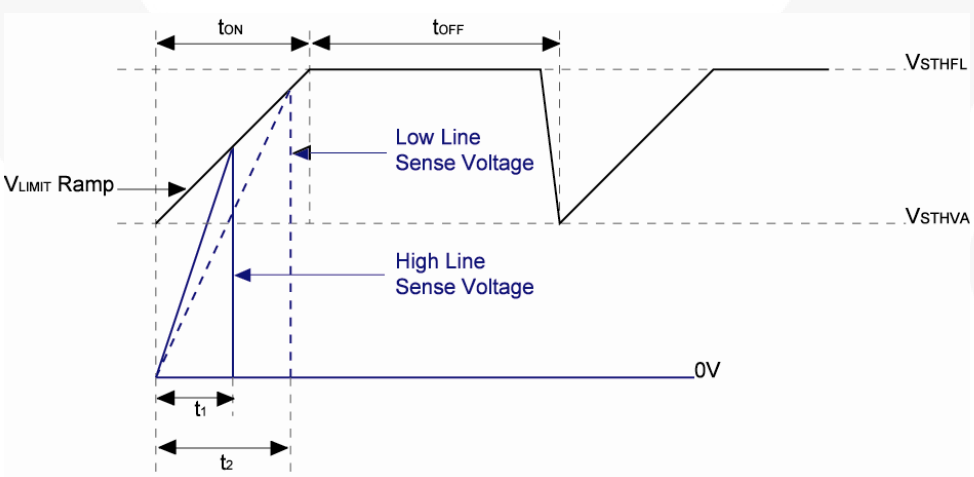


Figure 5. Saw Limit

Electrical Characteristics (Continued)

Unless otherwise noted, V_{DD}=15V and T_A=25°C.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
Oscillator Section							
f_{OSC}	Frequency	Center Frequency		60	65	70	kHz
		Hopping Range		±4.0	±4.6	±5.2	
t_{HOP}	Hopping Period				4		ms
f_{OSC-G}	Green Mode Frequency				17.0		KHz
V_{FB-N}	Green Mode Entry FB Voltage				2.6		V
V_{FB-G}	Green Mode Ending FB Voltage				V_{FB-N} -0.75		V
V_{FB-Z}	Zero Duty Cycle FB Voltage				1.35		V
S_G	Green Mode Modulation Slope			40	70	100	Hz/mV
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD}=10 to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A=-20 to 85°C		1.5	5.0	%
Internal MOSFET Section(3)							
DCY_{MAX}	Maximum Duty Cycle			70	75	80	%
BV_{DSS}	Drain- Source Breakdown Voltage		V_{DS} = 700V, V_{GS} = 0V	700			V
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 700V, V_{GS} = 0V		0.5	50.0	µA
			V_{DS} = 560V, V_{GS} = 0V, T_C = 125°C		1	200	
$R_{DS(ON)}$	Drain-Source On-State Resistance(4)		V_{GS} = 10V, I_D = 0.5A		4.00	4.75	Ω
C_{ISS}	Input Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		315	410	pF
C_{OSS}	Output Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		47	61	pF
C_{RSS}	Reverse Transfer Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		9	14	pF
$t_{d(on)}$	Turn-On Delay Time		V_{DS} = 350V, I_D = 1.0A		11.2	33.0	ns
t_r	Rise Time		V_{DS} = 350V, I_D = 1.0A		34	78	ns
$t_{d(off)}$	Turn-Off Delay Time		V_{DS} = 350V, I_D = 1.0A		28.2	67.0	ns
t_f	Fall Time		V_{DS} = 350V, I_D = 1.0A		32	74	ns
Over Temperature Protection (OTP)							
T_{OTP}	Protection Junction Temperature				140		°C
$T_{OTP-RESTART}$	Restart Junction Temperature				110		°C

Notes:
3. These parameters, although guaranteed, are not 100% tested in production.
4. Pulse test: Pulse width ≤ 300µs, duty ≤ 2%.

Typical Characteristics

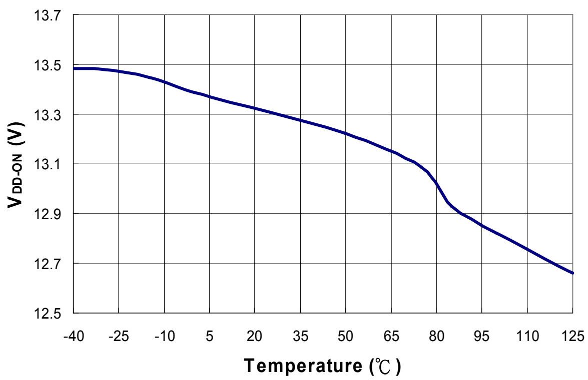


Figure 6. $V_{DD\text{-}ON}$ vs. Temperature

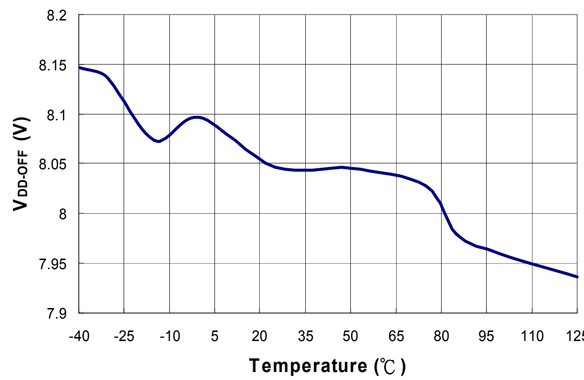


Figure 7. $V_{DD\text{-}OFF}$ vs. Temperature

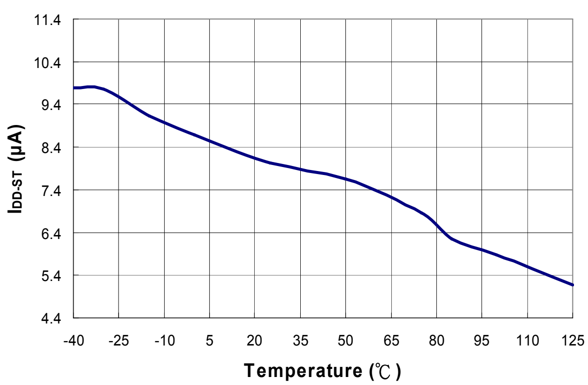


Figure 8. $I_{DD\text{-}ST}$ vs. Temperature

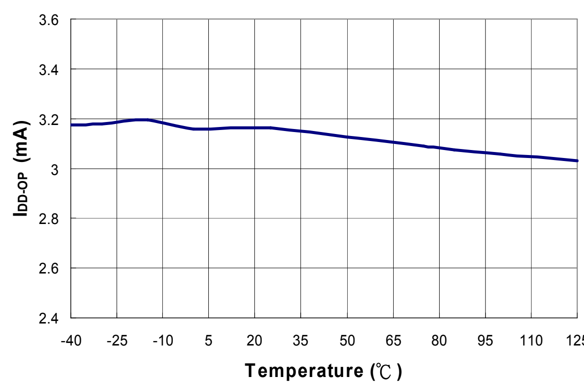


Figure 9. $I_{DD\text{-}OP}$ vs. Temperature

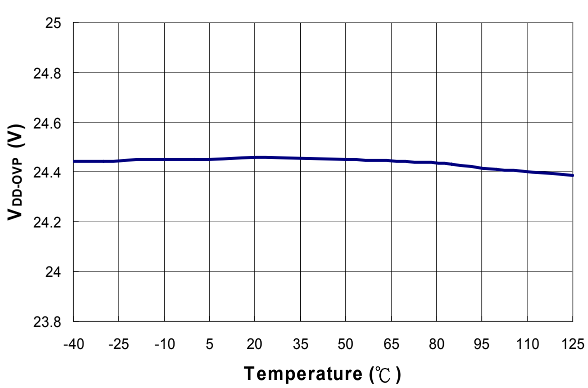


Figure 10. $V_{DD\text{-}OVP}$ vs. Temperature

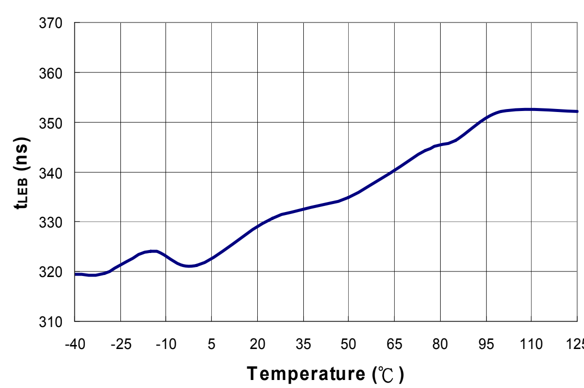


Figure 11. t_{LEB} vs. Temperature

Typical Characteristics

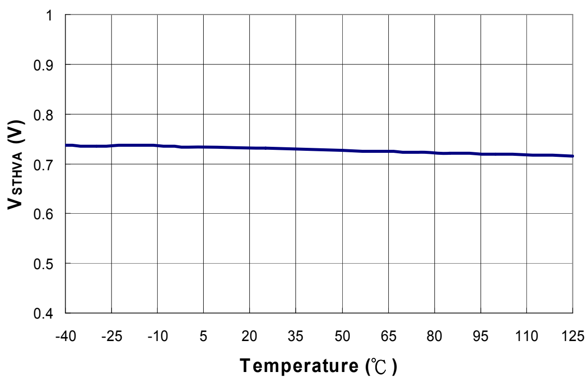


Figure 12. V_{STHVA} vs. Temperature

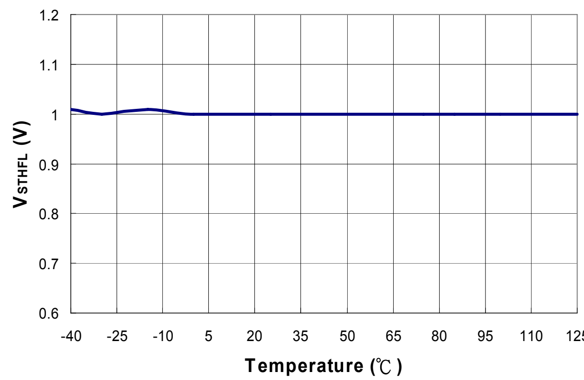


Figure 13. V_{STHFL} vs. Temperature

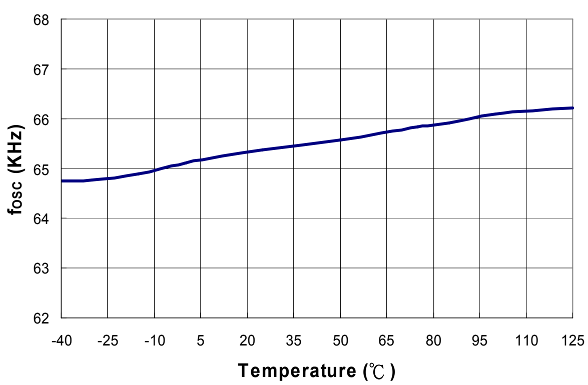


Figure 14. f_{OSC} vs. Temperature

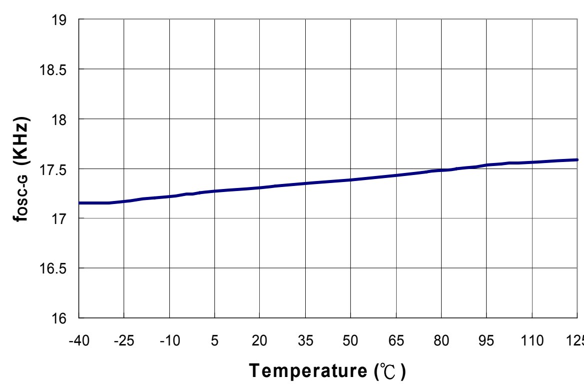


Figure 15. f_{OSC-G} vs. Temperature

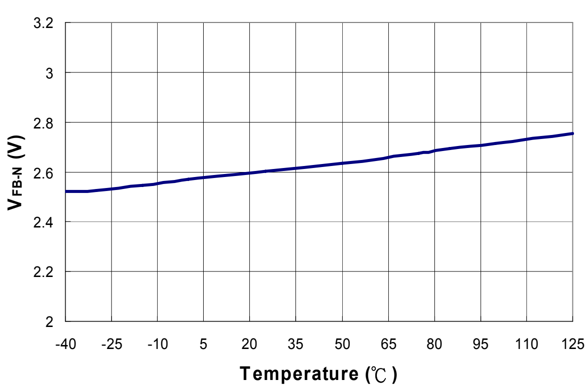


Figure 16. V_{FB-N} vs. Temperature

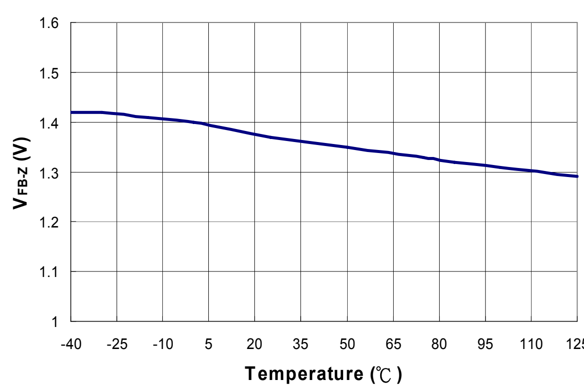


Figure 17. V_{FB-Z} vs. Temperature

Operation Description

FSEZ2037 integrates many useful functions for low-power switch-mode power supplies. The following descriptions highlight the key features.

Startup Current

The required startup current is only 8μA. This allows a high-resistance, low-wattage startup resistor to supply the controller's startup power. A 1.5MΩ/0.25W startup resistor can be used over a wide input range (90V-264V_{AC}) with very little power loss.

Operating Current

The operating current is normally 3.6mA, which results in higher efficiency and reduces the required V_{DD} hold-up capacitance. A 10μF/25V V_{DD} hold-up capacitor can be used over a wide input range (90V-264V_{AC}) with very little power loss.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load and zero-load conditions. The on-time is limited to provide better protection against brownouts and other abnormal conditions. Power supplies using the FSEZ2037 can meet international restrictions regarding standby power-consumption.

Current (CC) without Feedback

The FSEZ2037 can provide over-current protection without requiring secondary-side feedback signals. For improved CV and CC accuracy, the transformer leakage inductance should be reduced as much as possible.

Over-Temperature Protection (OTP)

The FSEZ2037 has a built-in temperature sensing circuit to shut down PWM output if the junction temperature exceeds 140°C. While PWM output is shut down, the V_{DD} voltage gradually drops to the UVLO voltage. Some of the internal circuits are shut down and V_{DD} gradually starts increasing again. When V_{DD} reaches 13V, all the internal circuits, including the temperature sensing circuit, operate normally. If the junction temperature is still higher than 140°C, the PWM controller shuts down immediately. This situation continues until the temperature drops below 110°C. The PWM output is then turned back on. The temperature hysteresis window for the OTP circuit is 30°C.

V_{DD} Over-Voltage Clamping

V_{DD} over-voltage clamping prevents damage from over-voltage conditions. When V_{DD} exceeds 24.5V, PWM output is shut down. Over-voltage conditions may be caused by an open photo-coupler loop or a short circuit in the output.

Oscillator Operation

The oscillation frequency is fixed at 65KHz.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense-resistor. To avoid premature termination of the switching pulse, a 330ns leading-edge blanking time is built in. Conventional RC filtering is not necessary. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate drive.

Constant Output Power Limit

When the SENSE voltage across sense resistor R_S reaches the threshold voltage (around 1.0V), the output GATE drive is turned off following a small propagation delay, t_{PD}. This propagation delay introduces an additional current proportional to $t_{PD} \bullet V_{IN}/L_P$. The propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltages result in larger additional currents. Under high input-line voltages the output power limit is higher than under low input-line voltages. Over a wide range of AC input voltages, the variation can be significant. To compensate for this, the threshold voltage is adjusted by adding a positive ramp (V_{limit_ramp}). This ramp signal can vary from 0.73V to 1.01V and flattens out at 1.01V. A smaller threshold voltage forces the output GATE drive to terminate earlier, reducing total PWM turn-on time and making the output power equal to that of the low line input. This proprietary internal compensation feature ensures a constant output power limit over a wide range of AC input voltages (90V-264V_{AC}).

Under-Voltage Lockout (UVLO)

The turn-on/turn-off thresholds are fixed internally at 13V and 8V. To enable the FSEZ2037 during startup, the hold-up capacitor must first be charged to 13V through the startup resistor. The hold-up capacitor continues to supply V_{DD} before energy can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 8V during this startup process. This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply V_{DD} during startup.

Slope Compensation

The sensed voltage across the current sense resistor is used for current mode control and pulse-by-pulse current limiting. The built-in slope compensation improves power supply stability and prevents sub-harmonic oscillations that normally would occur because of peak-current-mode control. A positively sloped, synchronized ramp is activated with every switching cycle. The slope of the ramp is:

$$\frac{0.33 \times \text{Duty}}{\text{Duty(max.)}} \qquad (1)$$

Noise Immunity

Noise from the current sense or the control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoid long PCB traces and component leads. Compensation and filter components should be located near the FSEZ2037. Increasing the power-MOS gate resistance is advised.

Typical Application Circuit

Application	Fairchild Devices	Input Voltage Range	Output
Cell Phone Charger	FSEZ2037	90~264V_{AC}	12V/1A (12W); without cable

Features

- High efficiency (>77.76% at full load) meeting EPS regulation with enough margin
- Standby power <0.3W at no-load condition
- Output regulation (CV:±0.84%, CC:±6.65%)

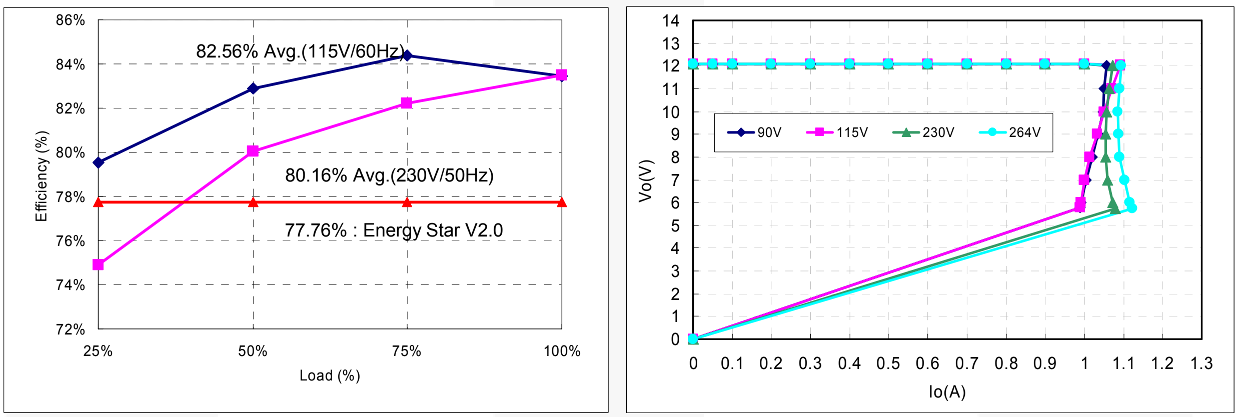


Figure 18. Measured Efficiency and Output Regulation

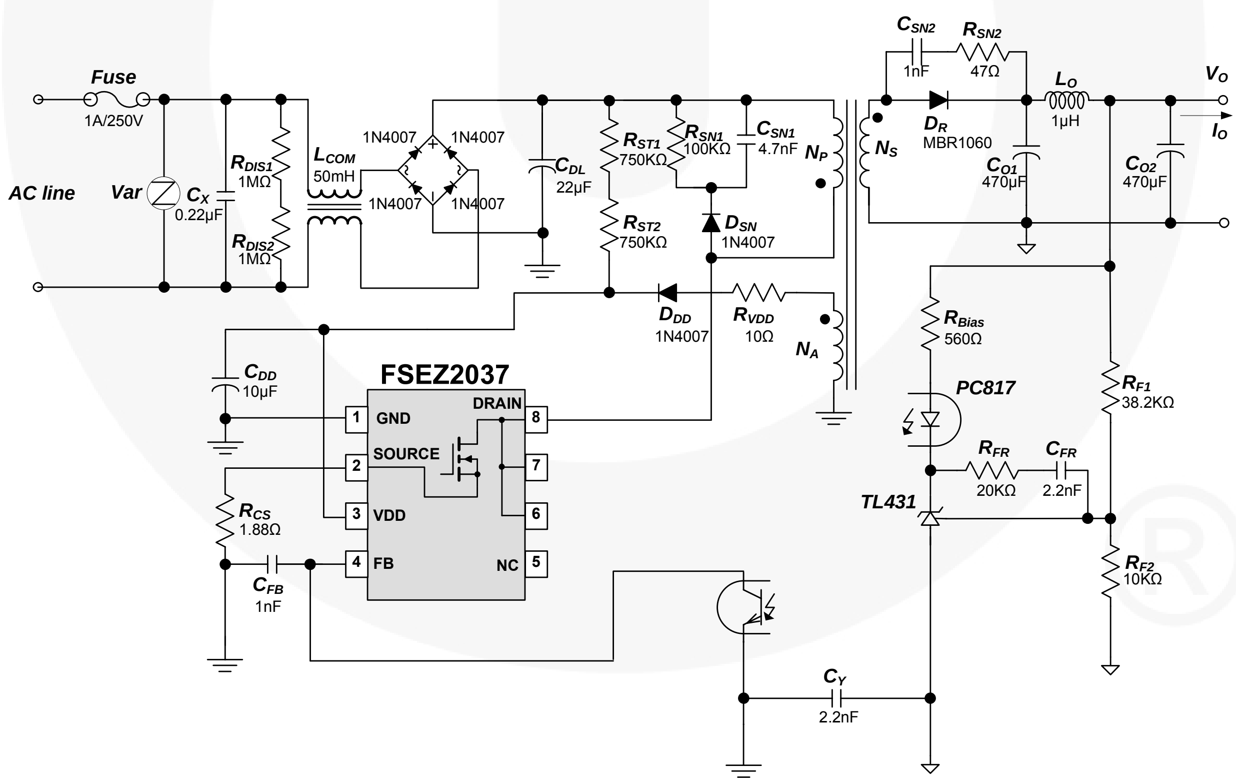


Figure 19. Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

- Core: EF20
- Bobbin: EF20

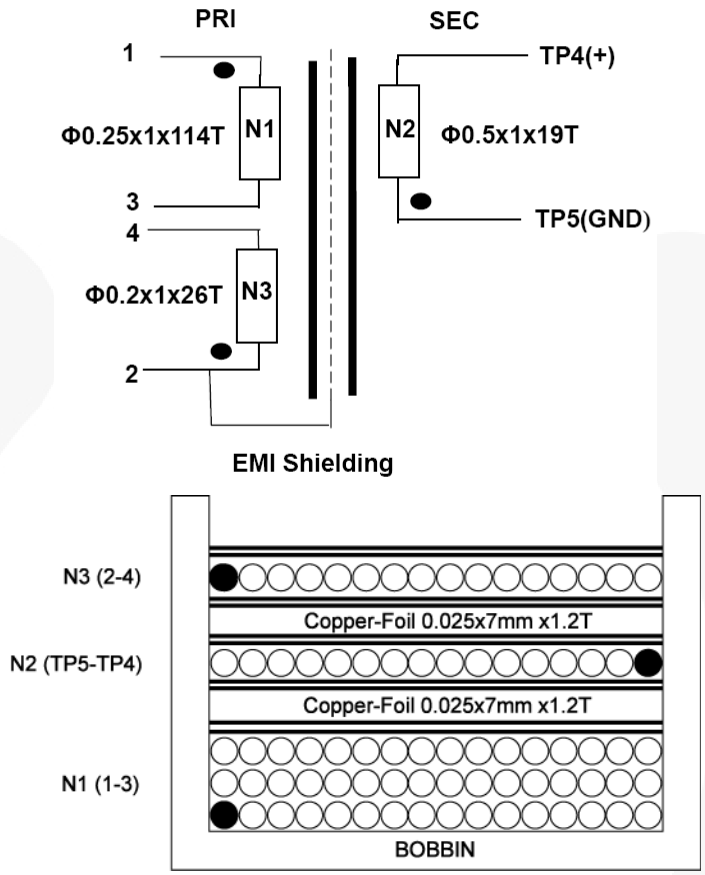


Figure 20. Transformer Diagram

	Pin	Specification	Remark
Primary-Side Inductance	1 – 3	1.5mH ± 5%	100kHz, 1V
Primary-Side Effective Leakage	1 – 3	40μH ± 5%	Short one of the secondary windings

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