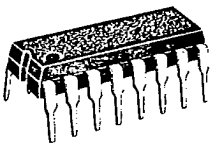
MN4020B / MN4020BS

14-Stage Binary Counters

■ Description

The MN4020B/S are binary counters in which an input-shaping circuit and 14-Stage flip-flops are built in.
Count is performed on the negative going edge of clock input.
The MN4020B/S are equivalent to MOTOROLA MC14020B and RCA CD4020B.

P- 3



16-Pin • Plastic DIL Package

P- 4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

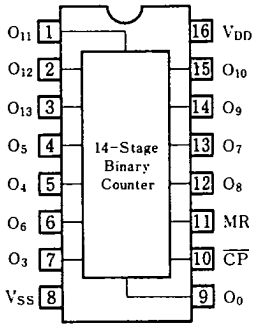
$\overline{CP}$	MR	Mode
⌐‾	L	No Change
‾⌐	L	Counter Advance
×	H	$O_0 \sim O_{13}$ = All "L"

Note) × : don't care

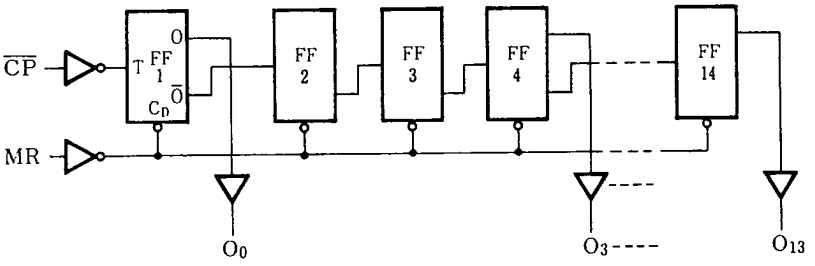
Pin Explanation

$\overline{CP}$: Negative clock input
MR : Reset input
$O_0, O_3 \sim O_{13}$: Parallel output

Pin Configuration



■ Logic Diagram



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

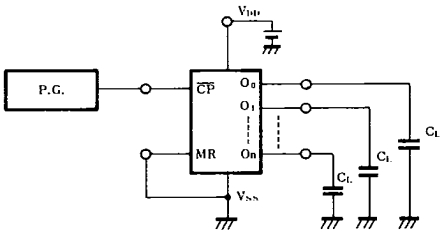
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

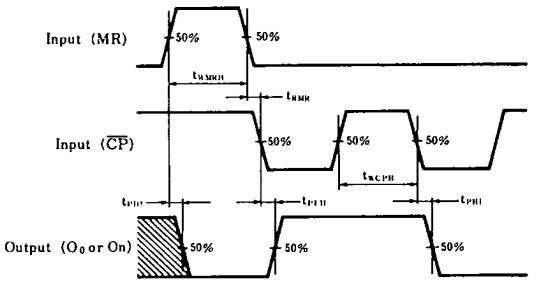
■ **Switching Characteristics** ($Ta = 25℃$, $V_{SS} = 0V$, $C_L = 50pF$)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{CP} \rightarrow O_0$ (H→L)	5	t_{PHL}	—	105	315	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time $\overline{CP} \rightarrow O_0$ (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $On \rightarrow On_{-1}$ (H→L)	5	t_{PHL}	—	80	270	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $On \rightarrow On_{-1}$ (L→H)	5	t_{PLH}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	180	540	ns
	10		—	90	270	
	15		—	70	210	
Minimum Clock Pulse Width	5	t_{WCPH}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Minimum MR Pulse Width	5	t_{WMRH}	—	65	195	ns
	10		—	50	150	
	15		—	45	135	
Reset Recovery Time	5	t_{RMR}	—	60	180	ns
	10		—	35	105	
	15		—	25	75	
Maximum Clock Frequency	5	fmax	5	10	—	MHz
	10		13	25	—	
	15		18	35	—	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths

■ Timing Diagram