/883 Version Obsolete
Replace with Equivalent SMD Device
(See "Ordering Information" Table Below)

HA-5221/883

October 1999

Low Noise, Wideband, Precision Operational Amplifier

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Gain Bandwidth Product . . . . . 100MHz (Min)**
- **Unity Gain Bandwidth . . . . . 30MHz (Min) 40MHz (Typ)**
- **High Slew Rate . . . . . 25V/µs (Min) 37V/µs (Typ)**
- **Low Offset Voltage . . . . . 0.75mV (Max) 0.30mV (Typ)**
- **High Open Loop Gain . . . . . 106dB (Min) 128dB (Typ)**
- **Low Voltage Noise (at 1kHz) . . . . . 5.8nV/√Hz (Max) 3.6nV/√Hz (Typ)**
- **Low Current Noise (at 1kHz) . . . . . 2.0pA/√Hz (Max) 1.4pA/√Hz (Typ)**
- **High Output Current . . . . . ±30mA (Min) ±56mA (Typ)**
- **Low Supply Current . . . . . 10mA (Max) 8mA (Typ)**

Applications

- **Precision Test Systems**
- **Active Filtering**
- **Small Signal Video**
- **Accurate Signal Processing**
- **RF Signal Conditioning**

Description

The HA-5221/883 is a high performance, dielectrically isolated, monolithic op amp, featuring precision DC characteristics while providing excellent AC characteristics. Designed for audio, video, and other demanding applications, noise (3.6nV/√Hz at 1kHz typ), total harmonic distortion (<0.005% typ), and DC errors are kept to a minimum.

The precision performance is shown by low offset voltage (0.3mV typ), low bias currents (40nA typ), low offset currents (15nA typ), and high open loop gain (128dB typ). The combination of these excellent DC characteristics with fast settling time (0.4µs typ) make the HA-5221/883 ideally suited for precision signal conditioning.

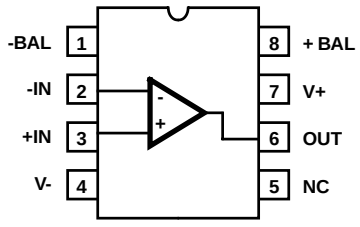
The unique design of the HA-5221/883 gives this device outstanding AC characteristics, including high unity gain bandwidth (40MHz typ) and high slew rate (37V/µs typ), not normally associated with precision op amps. Other key specifications include high CMRR (95dB typ) and high PSRR (100dB typ). The combination of these specifications will allow the HA-5221/883 to be used in RF signal conditioning as well as video amplifiers.

Ordering Information

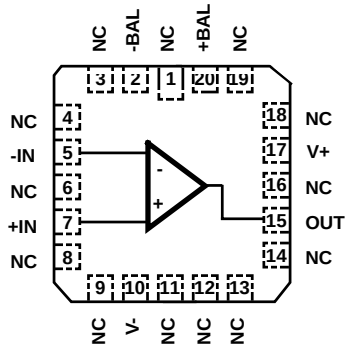
OBSOLETE PART NUMBER	SMD NO.	TEMP RANGE (^oC)	PACKAGE
HA4-5221/883	5962-9163401M2A	-55 to 125	20 Ld CLCC
HA7-5221/883	5962-9163401MPA	-55 to 125	8 Ld CERDIP

Pinouts

HA-5221/883
(CERDIP)
TOP VIEW



HA-5221/883
(CLCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
Differential Input Voltage. 5V
Voltage at Either Input Terminal . . . . . V+ to V-
Peak Output Current (Pulsed at 1ms, 10% Duty Cycle) 100mA
Continuous Output Current. . . . . Short Circuit Protected
Junction Temperature . . . . . +175^{o}C
Storage Temperature Range . . . . . -65^{o}C to +150^{o}C
ESD Rating. . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . +300^{o}C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	110^{o}C/W	27^{o}C/W
Ceramic LCC Package	64^{o}C/W	13^{o}C/W
Metal Can Package	148^{o}C/W	67^{o}C/W

Package Power Dissipation Limit at +75^{o}C
CerDIP Package 0.91W
Ceramic LCC Package 1.56W
Metal Can Package 0.68W
Package Power Dissipation Derating Factor Above +75^{o}C
CerDIP Package . . . . . 9.1mW/^{o}C
Ceramic LCC Package . . . . . 15.6mW/^{o}C
Metal Can Package . . . . . 6.8mW/^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -55^{o}C to +125^{o}C
Operating Supply Voltage . . . . . ±10V to ±15V

$V_{INCM} \leq 1/2\ (V+ - V-)$
$R_L \geq 1k\Omega$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_{SUPPLY} = \pm15V$, $R_{LOAD} = 1k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25^{o}C	-0.75	0.75	mV
			2, 3	+125^{o}C, -55^{o}C	-1.5	1.5	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$, $+R_S = 100.1k\Omega$, $-R_S = 100\Omega$	1	+25^{o}C	-80	80	nA
			2, 3	+125^{o}C, -55^{o}C	-200	200	nA
	$-I_B$	$V_{CM} = 0V$, $+R_S = 100\Omega$, $-R_S = 100.1k\Omega$	1	+25^{o}C	-80	80	nA
			2, 3	+125^{o}C, -55^{o}C	-200	200	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$, $+R_S = 100.1k\Omega$, $-R_S = 100.1k\Omega$	1	+25^{o}C	-50	50	nA
			2, 3	+125^{o}C, -55^{o}C	-150	150	nA
Common Mode Range	+CMR	V+ = +3V, V- = -27V	1	+25^{o}C	12	-	V
			2, 3	+125^{o}C, -55^{o}C	12	-	V
	-CMR	V+ = +27V, V- = -3V	1	+25^{o}C	-	-12	V
			2, 3	+125^{o}C, -55^{o}C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and +10V	4	+25^{o}C	106	-	dB
			5, 6	+125^{o}C, -55^{o}C	100	-	dB
	$-A_{VOL}$	$V_{OUT} = 0V$ and -10V	4	+25^{o}C	106	-	dB
			5, 6	+125^{o}C, -55^{o}C	100	-	dB
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +10V$, V+ = +5V, V- = -25V, $V_{OUT} = -10V$	1	+25^{o}C	88	-	dB
			2, 3	+125^{o}C, -55^{o}C	86	-	dB
	-CMRR	$\Delta V_{CM} = -10V$, V+ = +25V, V- = -5V, $V_{OUT} = +10V$	1	+25^{o}C	88	-	dB
			2, 3	+125^{o}C, -55^{o}C	86	-	dB
Output Voltage Swing	$+V_{OUT}$	$R_L = 1k\Omega$	4	+25^{o}C	12.0	-	V
			5, 6	+125^{o}C, -55^{o}C	11.5	-	V
	$-V_{OUT}$	$R_L = 1k\Omega$	4	+25^{o}C	-	-12.0	V
			5, 6	+125^{o}C, -55^{o}C	-	-11.5	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±15V, R_{LOAD} = 1kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current	$+I_{OUT}$	V_{OUT} = +10V, R_L = 1kΩ	4	+25°C	30	-	mA
			5, 6	+125°C, -55°C	30	-	mA
	$-I_{OUT}$	V_{OUT} = -10V, R_L = 1kΩ	4	+25°C	-	-30	mA
			5, 6	+125°C, -55°C	-	-30	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	10	mA
			2, 3	+125°C, -55°C	-	11	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-10	-	mA
			2, 3	+125°C, -55°C	-11	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V, V+ = +20V, V- = -15V, V+ = +10V, V- = -15V	1	+25°C	90	-	dB
			2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV_{SUP} = 10V, V+ = +15V, V- = -20V, V+ = +15V, V- = -10V	1	+25°C	90	-	dB
			2, 3	+125°C, -55°C	86	-	dB
Offset Voltage Adjustment	$+V_{IO}$Adj	Note 1	1	+25°C	V_{IO}-1	-	mV
			2, 3	+125°C, -55°C	V_{IO}-1	-	mV
	$-V_{IO}$Adj	Note 1	1	+25°C	V_{IO}+1	-	mV
			2, 3	+125°C, -55°C	V_{IO}+1	-	mV

NOTE:

1. Offset adjustment range is [V_{IO} (Measured ±1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See AC specifications in Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_{SUPPLY} = ±15V, R_{LOAD} = 1kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Noise Voltage Density	E_N	R_S = 0Ω, f_O = 10Hz	1, 5	+25°C	-	24.0	nV/√Hz
		R_S = 0Ω, f_O = 100Hz	1, 5	+25°C	-	8.0	nV/√Hz
		R_S = 0Ω, f_O = 1kHz	1, 5	+25°C	-	5.8	nV/√Hz
Input Noise Current Density	I_N	R_S = 500kΩ, f_O = 10Hz	1, 5	+25°C	-	11.5	pA/√Hz
		R_S = 500kΩ, f_O = 100Hz	1, 5	+25°C	-	6.0	pA/√Hz
		R_S = 500kΩ, f_O = 1kHz	1, 5	+25°C	-	2.0	pA/√Hz
Gain Bandwidth Product	GBWP	V_{OUT} = 200mV_{P-P}, f_O = 100kHz	1	+25°C	100	-	MHz
				-55°C to +125°C	90	-	MHz
Unity Gain Bandwidth	UGBW	V_{OUT} = 200mV	1	+25°C	30	-	MHz
				-55°C to +125°C	25	-	MHz
Slew Rate	±SR	V_{OUT} = ±2.5V, C_L = 50pF	1	-55°C to +125°C	25	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: V_{SUPPLY} = ±15V, R_{LOAD} = 1kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	-55°C to +125°C	398	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 1kΩ, C_L = 50pF	1	-55°C to +125°C	1	-	V/V
Rise and Fall Time	t_R, t_F	V_{OUT} = ±100mV	1, 4	+25°C	-	20	ns
Overshoot	±OS	V_{OUT} = ±100mV	1	+25°C	-	25	%
				-55°C to +125°C	-	30	%
Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	660	mW

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.).
4. Measured between 10% and 90% points.
5. Input Noise Voltage Density and Input Noise Current Density limits are based on characterization data.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
72 x 94 x 19 mils ± 1 mils
1840 x 2400 x 483µm ± 25.4µm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride (Si3N4) over Silox (SIO2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:
$4.2 \times 10^4 A/cm^2$

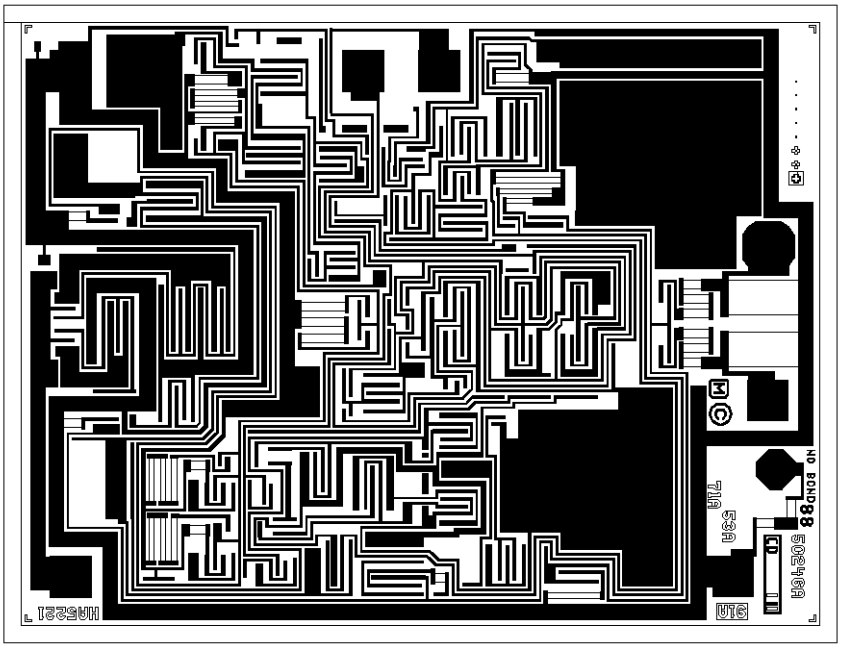
SUBSTRATE POTENTIAL (Powered Up): V-

TRANSISTOR COUNT: 62

PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5221/883



DESIGN INFORMATION (Continued)

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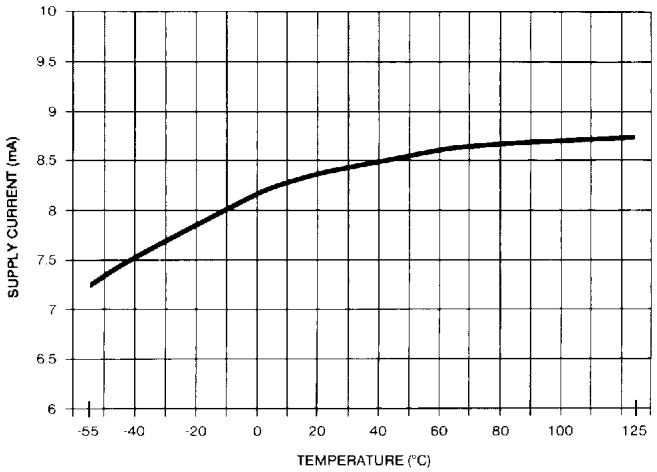
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

SUPPLY CURRENT vs TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, C_L = 50pF, Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Input Offset Voltage	See Table 1	+25°C	0.3	mV
		Full	0.35	mV
Average Offset Voltage Drift	See Table 1	Full	0.5	µV/°C
Input Bias Current	See Table 1	+25°C	40	nA
		Full	70	nA
Input Offset Current	See Table 1	+25°C	15	nA
		Full	30	nA
Differential Input Resistance	See Table 1	+25°C	70	kΩ
Input Noise Voltage	f_O = 0.1Hz to 10Hz	+25°C	0.25	μV_{P-P}
Input Noise Voltage Density	f_O = 10Hz	+25°C	10	nV/√Hz
	f_O = 100Hz	+25°C	5	nV/√Hz
	f_O = 1kHz	+25°C	3.6	nV/√Hz
Input Noise Current Density	f_O = 10Hz	+25°C	7	pA/√Hz
	f_O = 100Hz	+25°C	3	pA/√Hz
	f_O = 1kHz	+25°C	1.4	pA/√Hz
THD & N	See Note 1	+25°C	0.005	%
Large Signal Voltage Gain	V_{OUT} = 0V to ±10V	+25°C	128	dB
		Full	120	dB

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: Supply Voltage = ±15V, R_L = 1kΩ, C_L = 50pF, Unless Otherwise Specified

PARAMETERS	CONDITIONS		TEMPERATURE	TYPICAL	UNITS
Common Mode Rejection Ratio	ΔV_{CM} = ±10V		Full	95	dB
Unity Gain Bandwidth	(-3dB)		+25°C	40	MHz
			+125°C	33	MHz
			-55°C	45	MHz
Gain Bandwidth Product	1kHz to 400kHz		+25°C	130	MHz
			+125°C	110	MHz
			-55°C	150	MHz
Minimum Gain Stability			Full	1	V/V
Output Voltage Swing	R_L = 333Ω		Full	±10	V
	R_L = 1K		+25°C	±12.5	V
			Full	±12.1	V
Output Current	V_{OUT} = ±10V		Full	±56	mA
Output Resistance			+25°C	10	W
Full Power Bandwidth	FPBW = SR/2πV_{PEAK}, V_{PEAK} = 10V		+25°C	398	kHz
Slew Rate	V_{OUT} = ±2.5V		+25°C	37	V/µs
			+125°C	37	V/µs
			-55°C	34	V/µs
Rise Time	V_{OUT} = ±100mV		+25°C	13	ns
			+125°C	13	ns
			-55°C	15	ns
Overshoot	V_{OUT} = ±100mV		+25°C	13	%
			+125°C	13	%
			-55°C	11	%
Settling Time	$10V_{STEP}$, AV = -1	0.1%	+25°C	0.4	µs
		0.01%	+25°C	1.5	µs
Power Supply Rejection Ratio	ΔV_S = ±10V to ±20V		Full	100	dB
Supply Current			Full	8	mA
Minimum Supply Voltage	Functional Operation Only. Other Parameters May Vary.		+25°C	±5	V

NOTE:

1. A_{VCL} = 10, f_O = 1kHz, V_{OUT} = 5Vrms, R_L = 600Ω, 10Hz to 100Hz, Minimum resolution of test equipment is 0.005%.

DESIGN INFORMATION (Continued)

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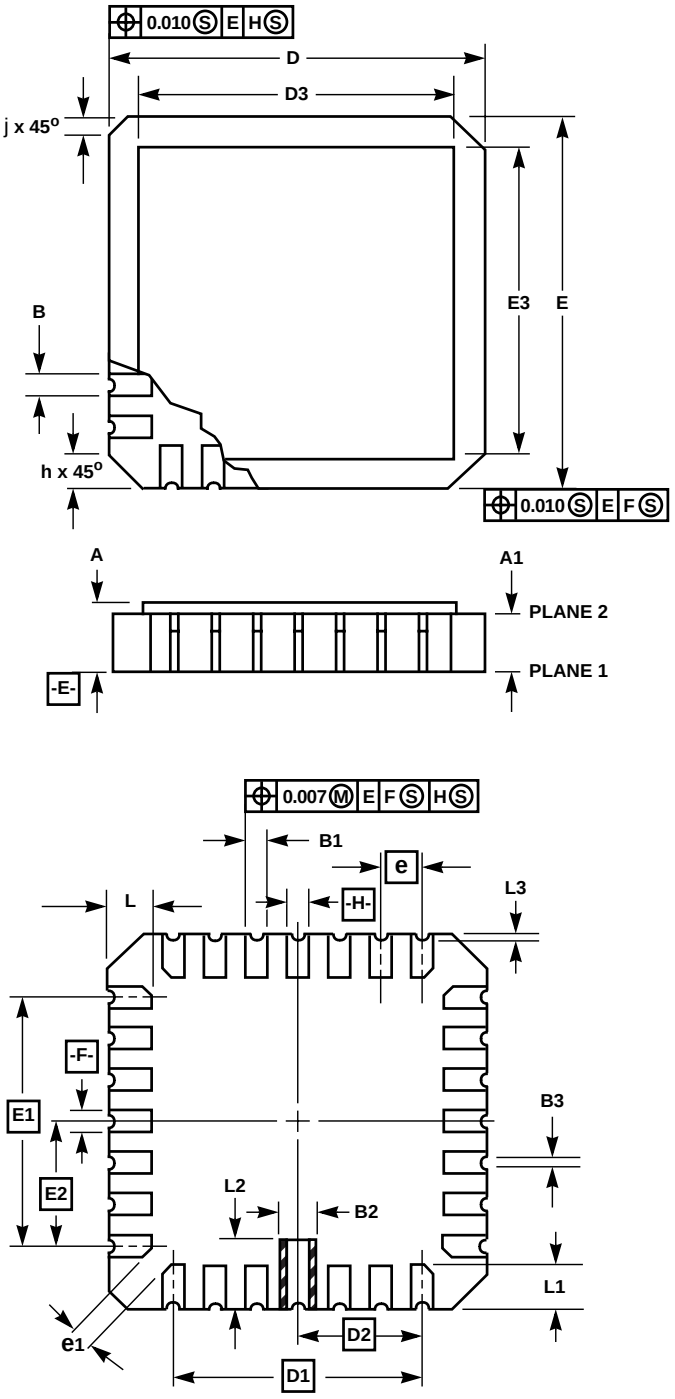
PARAMETERS	CONDI-TIONS	TEMPERATURE	TYPICAL	UNITS
Input Noise Current Density	fO = 10Hz	+25oC	7	pA/qHz
	fO = 100Hz	+25oC	3	pA/qHz
	fO = 1kHz	+25oC	1.4	pA/qHz
THD & N	See Note 1	+25oC	0.005	%
Large Signal Voltage Gain	VOUT = 0 to 110V	+25oC	128	dB
		Full	120	dB
Common Mode Rejection Ratio	Delta VCM = 110V	Full	95	dB
Unity Gain Bandwidth	(-3)			

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A **MIL-STD-1835 CQCC1-N20 (C-2)**
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

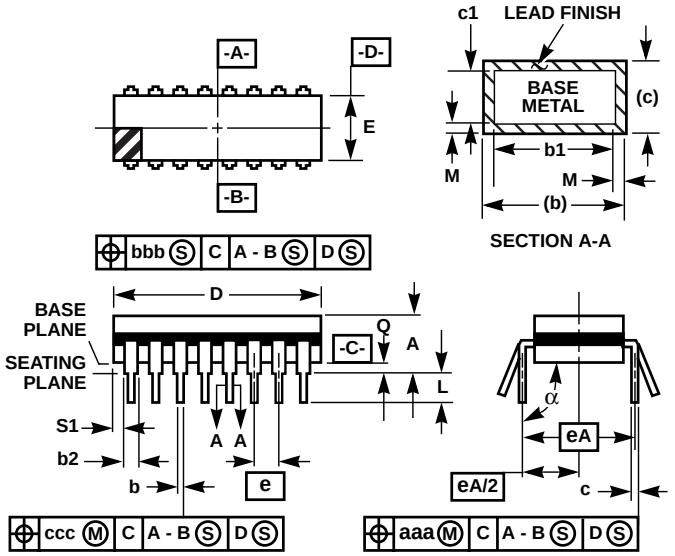
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

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