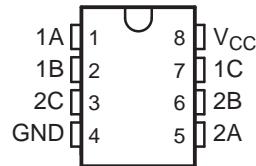


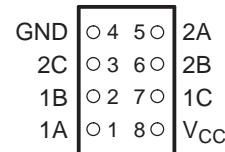
FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Operates at 0.8 V to 2.7 V
- Sub-1-V Operable
- Max t_{pd} of 0.5 ns at 1.8 V
- Low Power Consumption, 10 μ A at 2.7 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DCT OR DCU PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



DESCRIPTION/ORDERING INFORMATION

This dual analog switch is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.1-V to 2.7-V V_{CC} operation.

The SN74AUC2G66 can handle both analog and digital signals. It permits signals with amplitudes of up to 2.7-V (peak) to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
-40°C to 85°C	NanoFree™ – W CSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G66YZPR _ _ _ U6 _
	SSOP – DCT	Reel of 3000	SN74AUC2G66DCTR U66_ _ _
	VSSOP – DCU	Reel of 3000	SN74AUC2G66DCUR U66_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

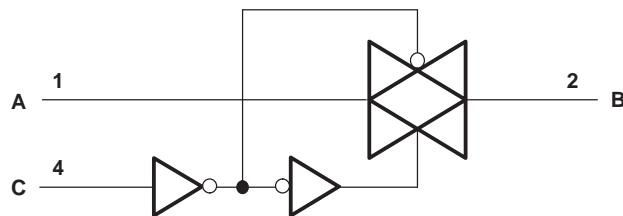
CONTROL INPUT (C)	SWITCH
L	OFF
H	ON



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range ⁽²⁾	-0.5	3.6	V
V_I	Input voltage range ⁽²⁾⁽³⁾	-0.5	3.6	V
$V_{I/O}$	Switch I/O voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Control input clamp current	$V_I < 0$	-50	mA
I_{IOK}	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$	± 50	mA
I_T	On-state switch current	$V_{I/O} = 0$ to V_{CC}	± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DCT package	220	°C/W
		DCU package	227	
		YZP package	102	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC} Supply voltage			0.8	2.7	V
V _{IH} High-level input voltage	V _{CC} = 0.8 V		V _{CC}		V
	V _{CC} = 1.1 V to 1.95 V		0.65 × V _{CC}		
	V _{CC} = 2.3 V to 2.7 V		1.7		
V _{IL} Low-level input voltage	V _{CC} = 0.8 V		0		V
	V _{CC} = 1.1 V to 1.95 V		0.35 × V _{CC}		
	V _{CC} = 2.3 V to 2.7 V		0.7		
V _{I/O} I/O port voltage			0	V _{CC}	V
V _I Control input voltage			0	3.6	V
Δt/Δv Input transition rise or fall rate	V _{CC} = 0.8 V to 1.65 V ⁽²⁾		20		ns/V
	V _{CC} = 1.65 V to 2.3 V ⁽³⁾		20		
	V _{CC} = 2.3 V to 2.7 V ⁽³⁾		20		
T _A Operating free-air temperature			-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) The data was taken at C_L = 15 pF, R_L = 2 kΩ (see [Figure 1](#)).

(3) The data was taken at C_L = 30 pF, R_L = 500 Ω (see [Figure 1](#)).

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
r _{on} On-state switch resistance	V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 1 and Figure 2)	I _S = 4 mA	1.1 V	17	40	Ω
			1.65 V	7	20	
		I _S = 8 mA	2.3 V	4	15	
r _{on(p)} Peak on resistance	V _I = V _{CC} to GND, V _C = V _{IH} (see Figure 1 and Figure 2)	I _S = 4 mA	1.1 V	131	180	Ω
			1.65 V	32	80	
		I _S = 8 mA	2.3 V	15	20	
Δr _{on} Difference of on-state resistance between switches	V _I = V _{CC} to GND, V _C = V _{IH} (see Figure 1 and Figure 2)	I _S = 4 mA	1.1 V		3	Ω
			1.65 V		1	
		I _S = 8 mA	2.3 V		1	
I _{S(off)} Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see Figure 3)		2.7 V		±1	μA
					±0.1 ⁽²⁾	
I _{S(on)} On-state switch leakage current	V _I = V _{CC} or GND, V _C = V _{IH} , V _O = Open (see Figure 4)		2.7 V		±1	μA
					±0.1 ⁽²⁾	
I _I Control input current	V _I = V _{CC} or GND		0 to 2.7 V		±5	μA
I _{CC} Supply current	V _I = V _{CC} or GND, I _O = 0		0.8 V to 2.7 V		10	μA
C _{ic} Control input capacitance			2.5 V		2.5	pF
C _{io(off)} Switch input/output capacitance			2.5 V		3	pF
C _{io(on)} Switch input/output capacitance			2.5 V		7	pF

(1) t_a = 25°C

(2) The data was taken at C_L = 15 pF, R_L = 2 kΩ (see [Figure 1](#)).

SN74AUC2G66

DUAL BILATERAL ANALOG SWITCH

SCES507A–NOVEMBER 2003–REVISED JANUARY 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see [Figure 5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	UNIT
			TYP	MIN	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A	1	0.6		0.5	0.5	0.4
t_{en}	C	A or B	5	0.5	3	0.5	2.1	0.5
t_{dis}	C	A or B	5.3	0.5	4	0.5	3	0.5
						0.5	2.6	3.3
						0.5	2.7	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see [Figure 5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	UNIT			
			MIN	TYP	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A		0.7		0.7	0.7	ns
t_{en}	C	A or B	0.5	1.6	2.7	0.5	2.3	ns
t_{dis}	C	A or B	0.5	2.7	3.4	0.5	2	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

Analog Switch Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (switch ON)	A or B	B or A	$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, f_{in} = sine wave (see Figure 6)	0.8 V	101	MHz
				1.1 V	150	
				1.4 V	175	
				1.65 V	250	
				2.3 V	400	
			$C_L = 5 \text{ pF}$, $R_L = 50 \Omega$, f_{in} = sine wave (see Figure 6)	0.8 V	450	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	
Crosstalk (between switches)	A or B	B or A	$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, $f_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 7)	0.8 V	-60	dB
				1.1 V	-60	
				1.4 V	-60	
				1.65 V	-60	
				2.3 V	-60	
			$C_L = 5 \text{ pF}$, $R_L = 50 \Omega$, $f_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 7)	0.8 V	-65	
				1.1 V	-65	
				1.4 V	-65	
				1.65 V	-65	
				2.3 V	-65	

Analog Switch Characteristics (continued)

TA = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	TYP	UNIT
Crosstalk (control input to signal output)	C	A or B	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 8)	0.8 V	9	mV
				1.1 V	14	
				1.4 V	15	
				1.65 V	16	
				2.3 V	20	
Feedthrough attenuation (switch OFF)	A or B	B or A	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	-50	dB
				1.1 V	-50	
				1.4 V	-50	
				1.65 V	-50	
				2.3 V	-50	
		B or A	C _L = 5 pF, R _L = 50 Ω, f _{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	-60	
				1.1 V	-60	
				1.4 V	-60	
				1.65 V	-60	
				2.3 V	-60	
Sine-wave distortion	A or B	B or A	C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 10)	0.8 V	7	%
				1.1 V	0.256	
				1.4 V	0.04	
				1.65 V	0.03	
				2.3 V	0.01	
	A or B	B or A	C _L = 50 pF, R _L = 10 kΩ, f _{in} = 10 kHz (sine wave) (see Figure 10)	0.8 V	3.7	
				1.1 V	0.4	
				1.4 V	0.04	
				1.65 V	0.02	
				2.3 V	0.02	

Operating Characteristics

TA = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
		TYP	TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance f = 10 MHz	2.5	2.5	2.5	2.5	2.5	pF

PARAMETER MEASUREMENT INFORMATION

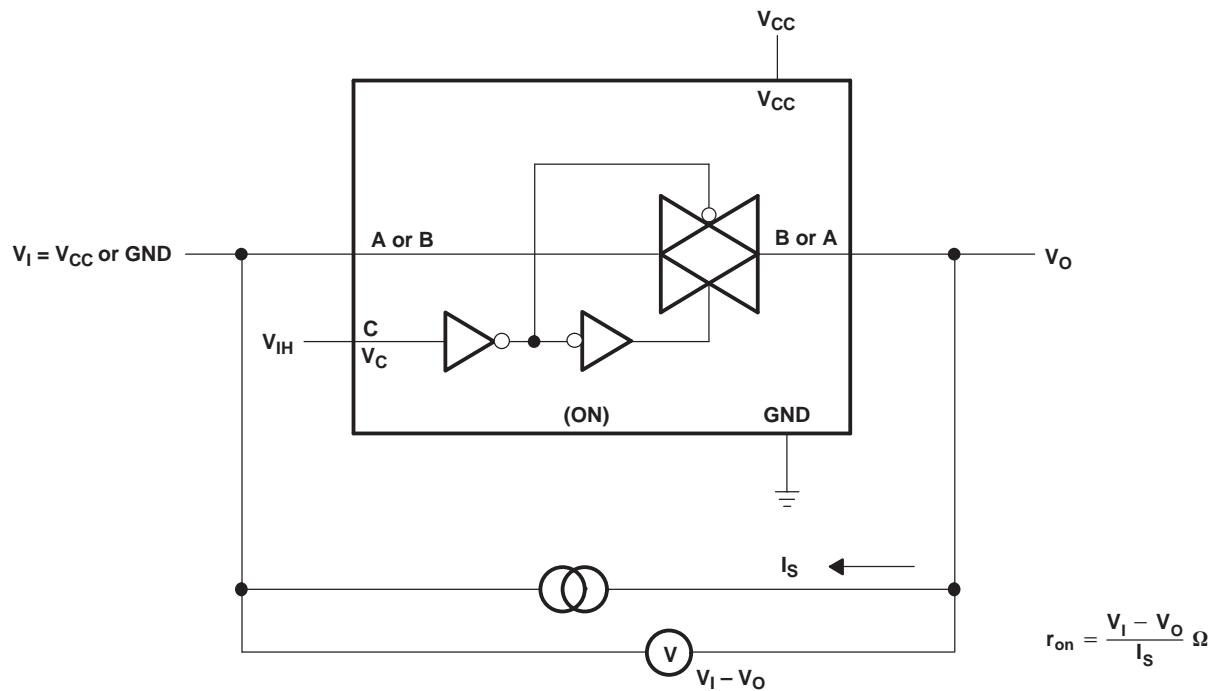


Figure 1. On-State Resistance Test Circuit

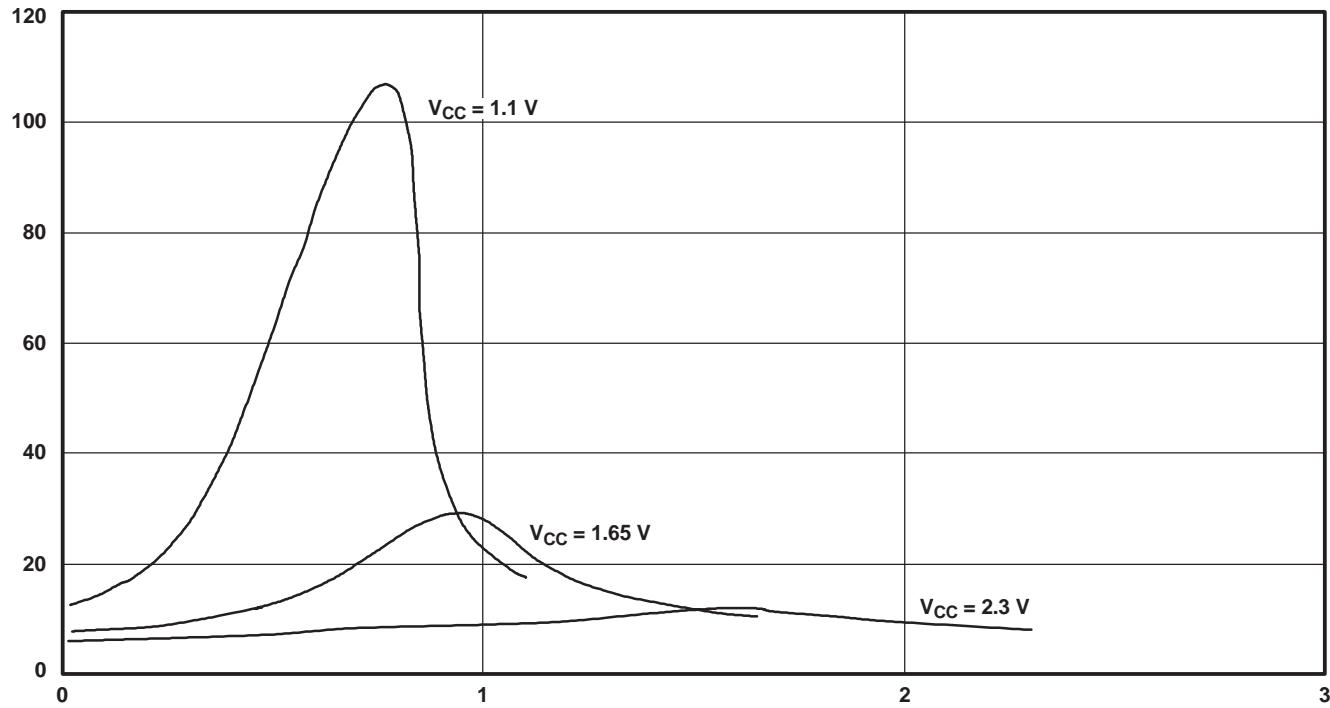


Figure 2. Typical r_{on} as a Function of Voltage (V_I) for $V_I = 0$ to V_{CC}

PARAMETER MEASUREMENT INFORMATION

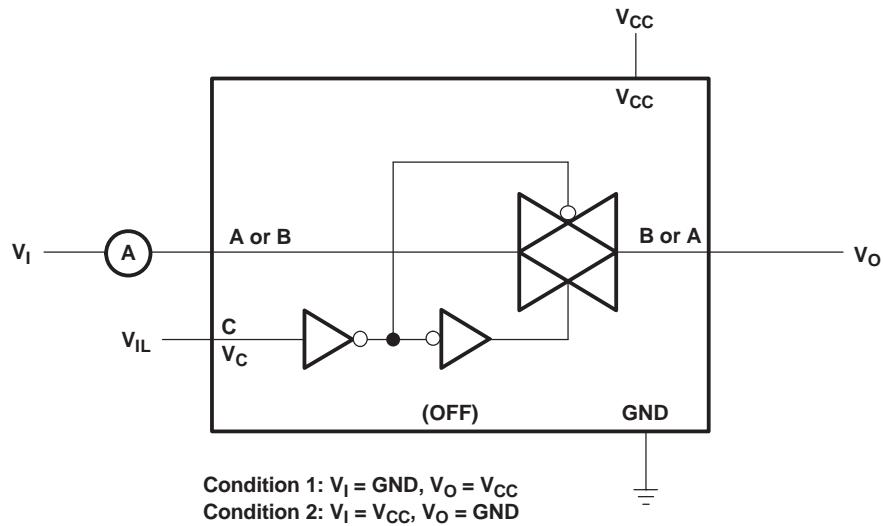


Figure 3. Off-State Switch Leakage-Current Test Circuit

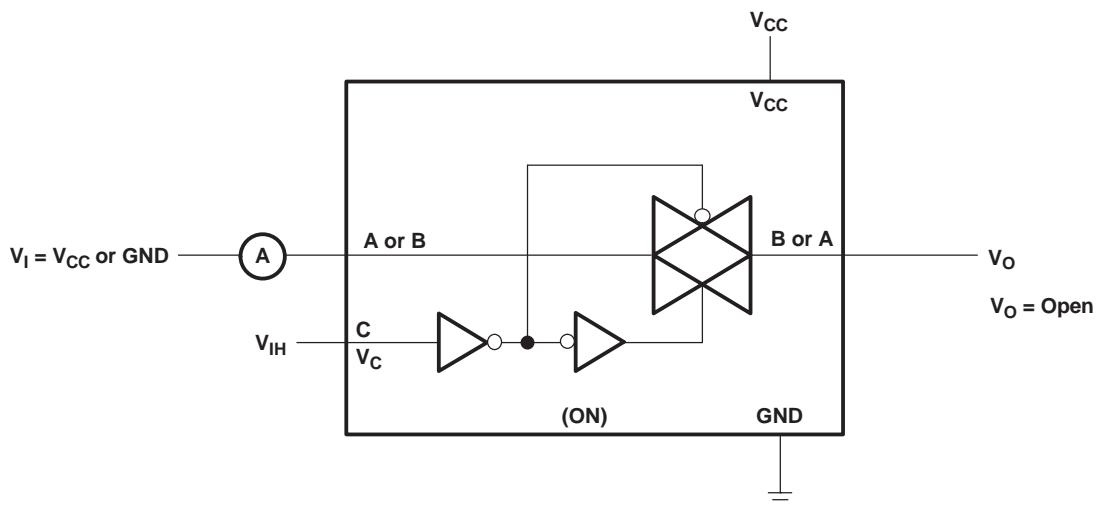
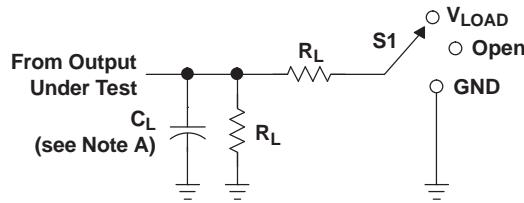


Figure 4. On-State Leakage-Current Test Circuit

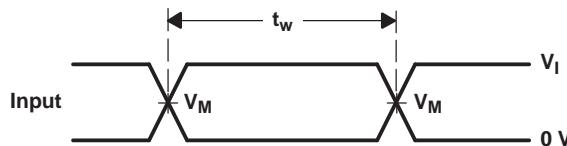
PARAMETER MEASUREMENT INFORMATION



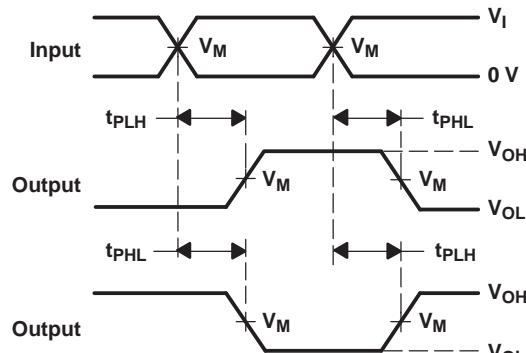
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

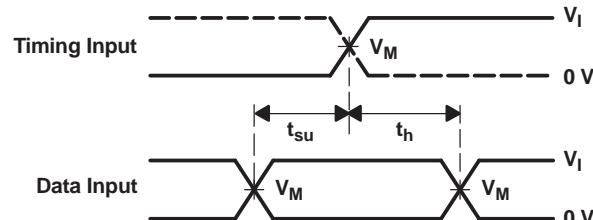
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.2 \text{ V} \pm 0.1 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.5 \text{ V} \pm 0.1 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.15 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V



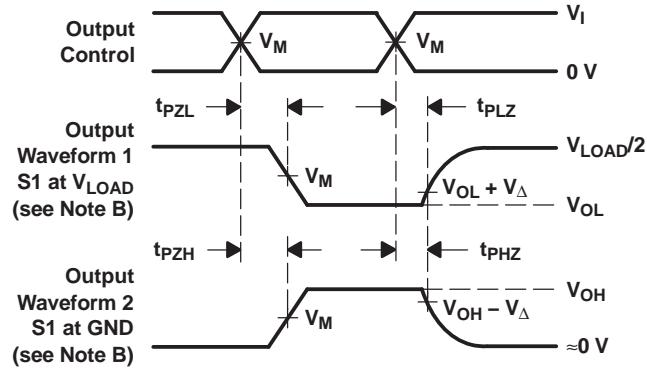
**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, slew rate ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

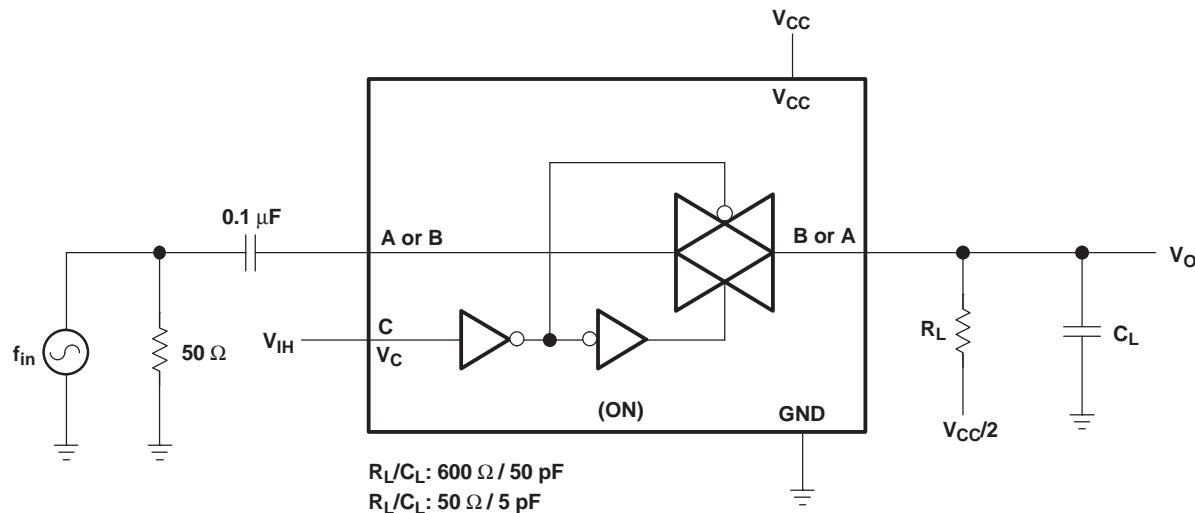


Figure 6. Frequency Response (Switch ON)

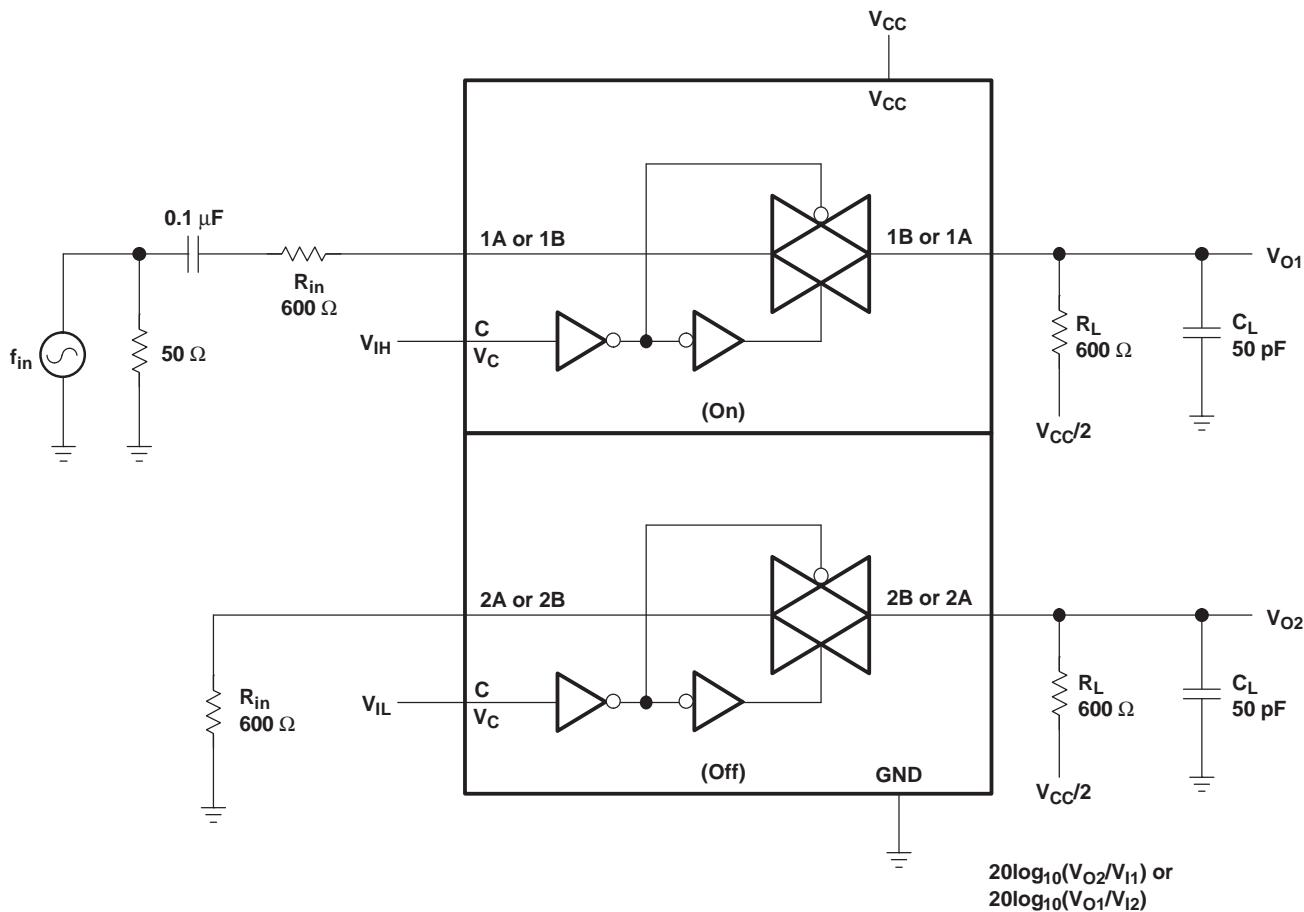


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

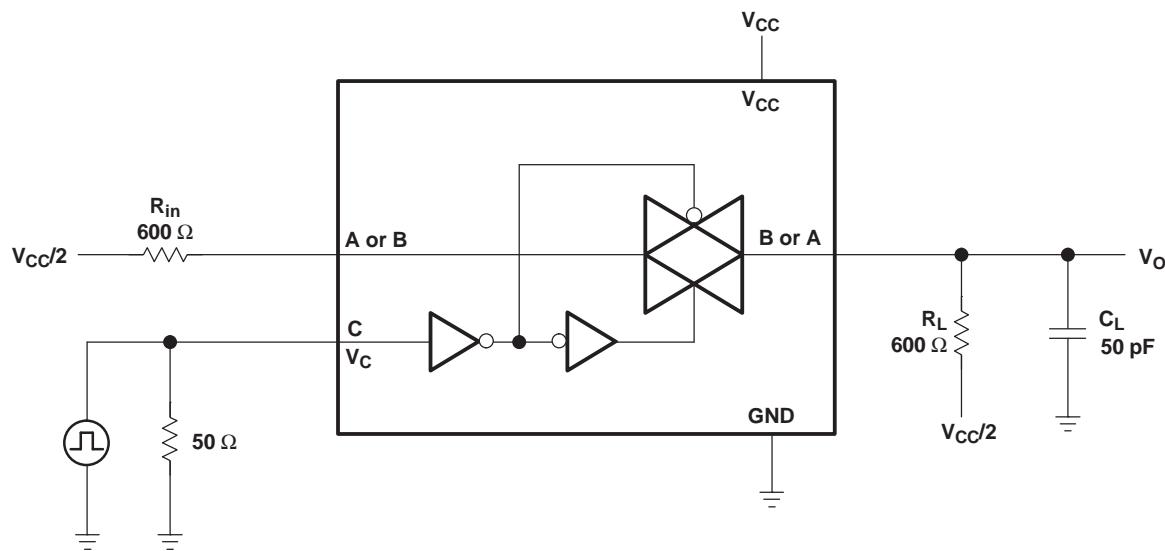


Figure 8. Crosstalk (Control Input – Switch Output)

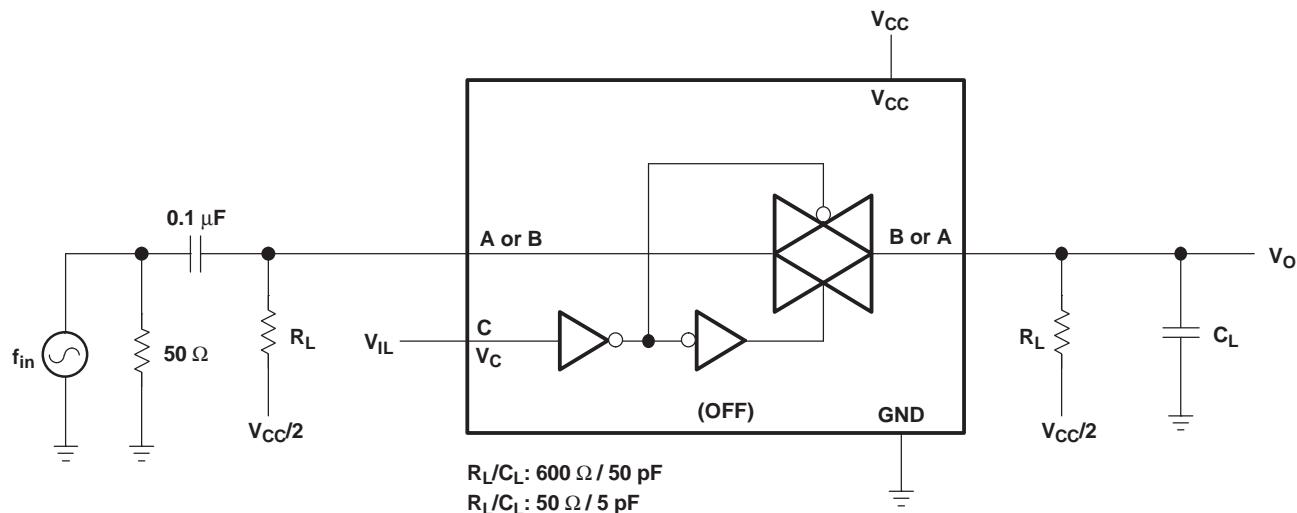


Figure 9. Feedthrough, Switch Off

PARAMETER MEASUREMENT INFORMATION

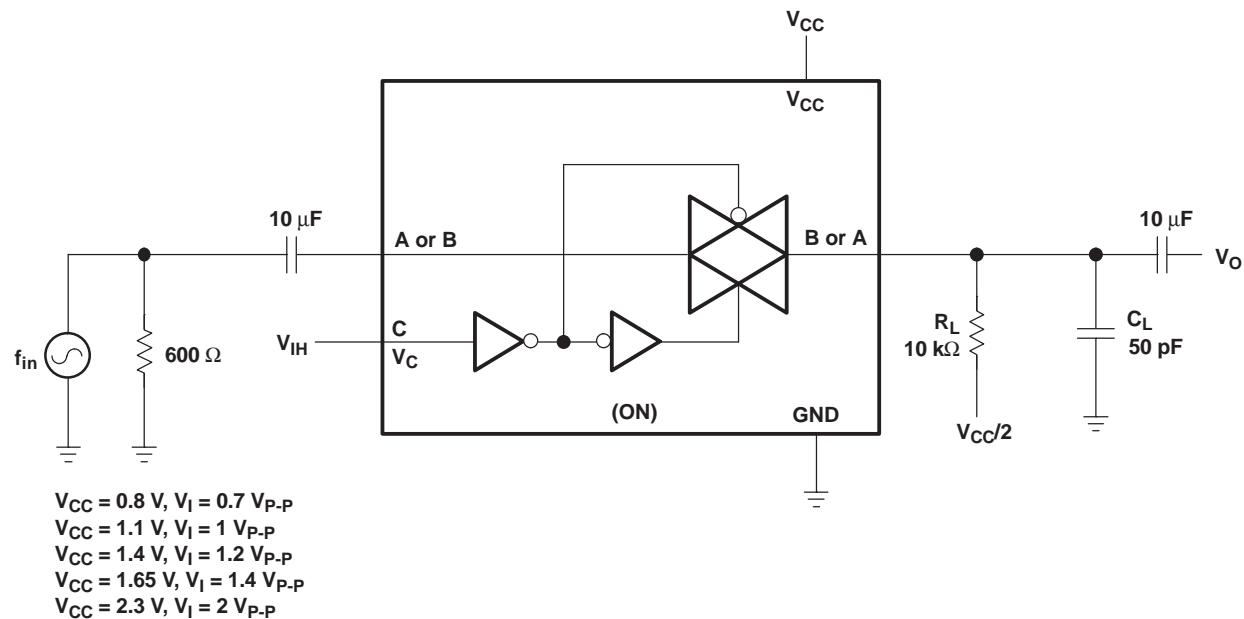


Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC2G66DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	U66Z	Samples
SN74AUC2G66DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	(66 ~ U66Q ~ U66R) (UR ~ UZ)	Samples
SN74AUC2G66DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	U66R	Samples
SN74AUC2G66DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	U66R	Samples
SN74AUC2G66YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U67	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

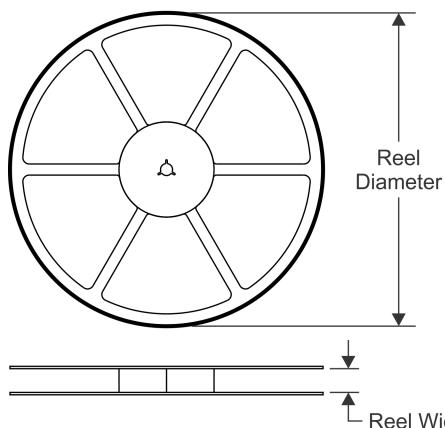
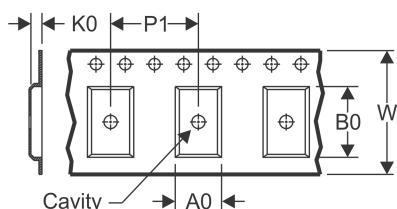
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

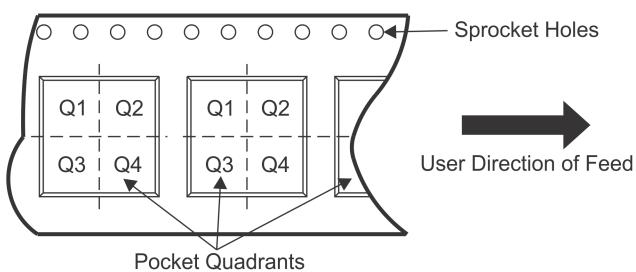
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G66DCUR	US8	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
SN74AUC2G66DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G66DCURG4	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G66YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

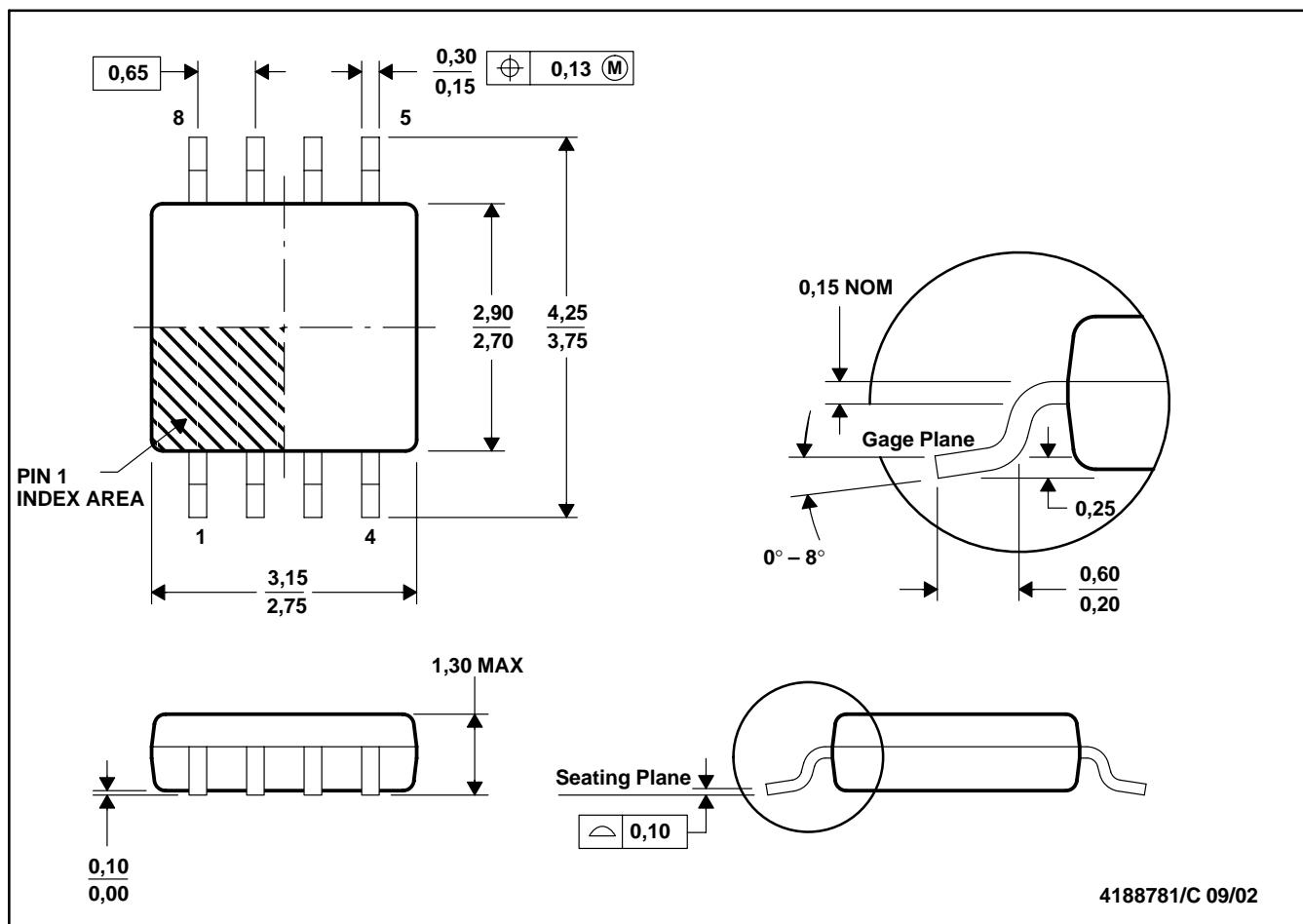
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G66DCUR	US8	DCU	8	3000	182.0	182.0	20.0
SN74AUC2G66DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G66DCURG4	US8	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G66YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

DCT (R-PDSO-G8)

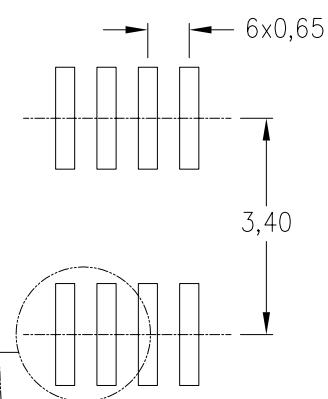
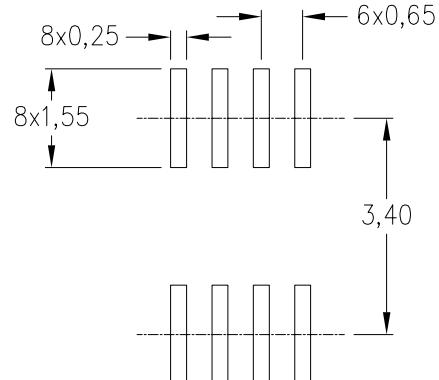
PLASTIC SMALL-OUTLINE PACKAGE



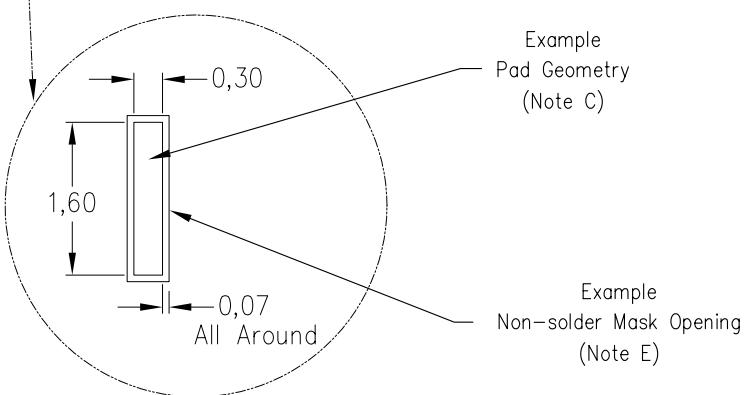
NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion
 D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C,E)Example Stencil Design
(Note D)

Non Solder Mask Defined Pad

Example
Pad Geometry
(Note C)Example
Non-solder Mask Opening
(Note E)

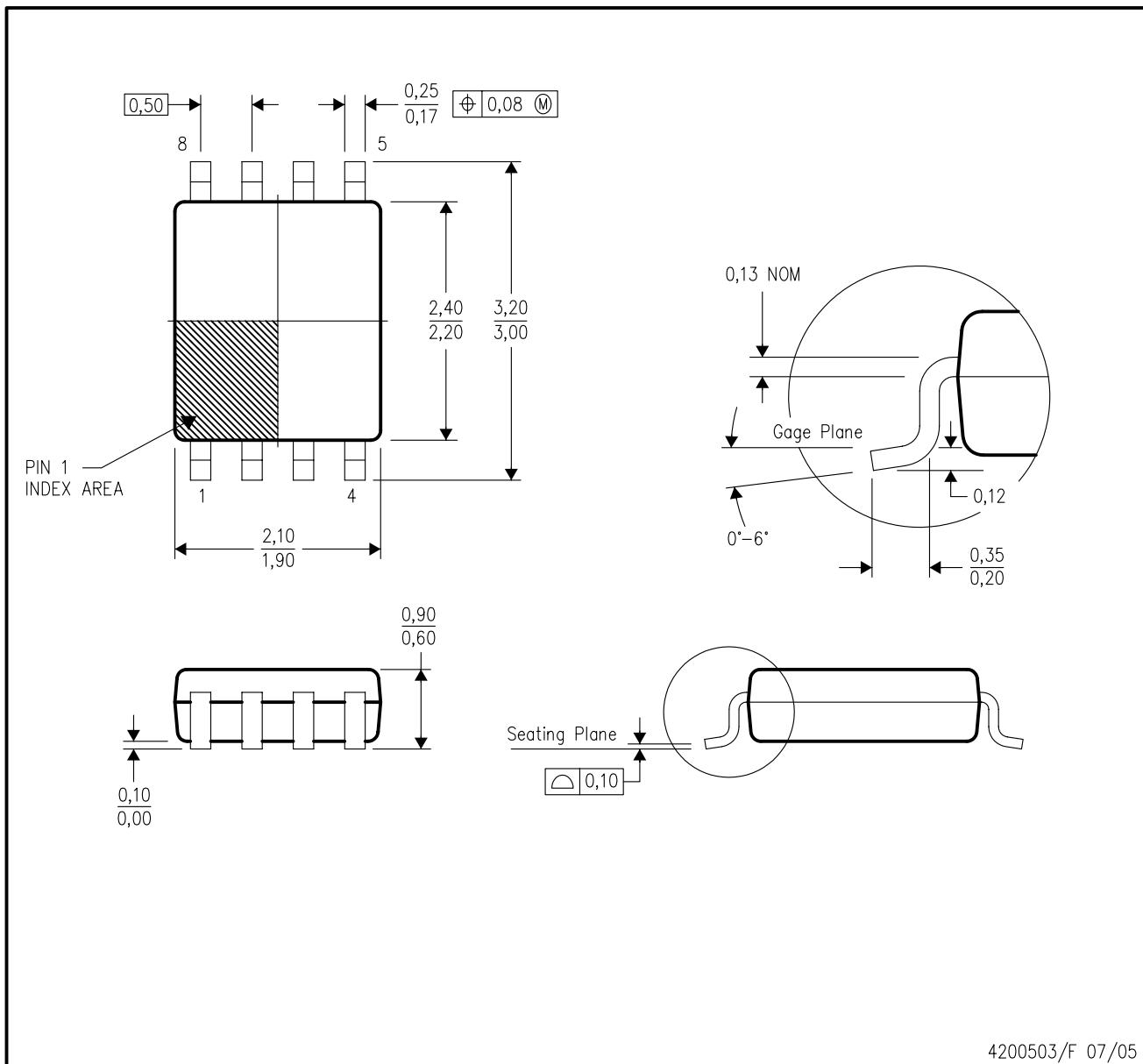
4212201/A 10/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



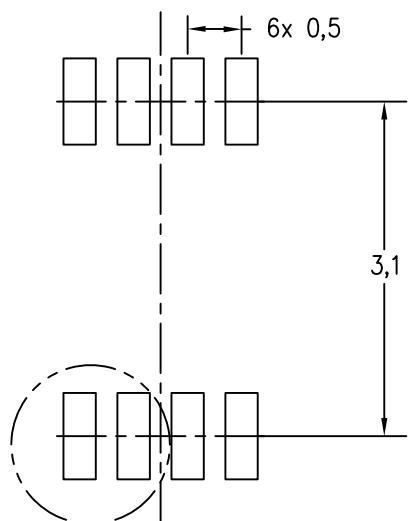
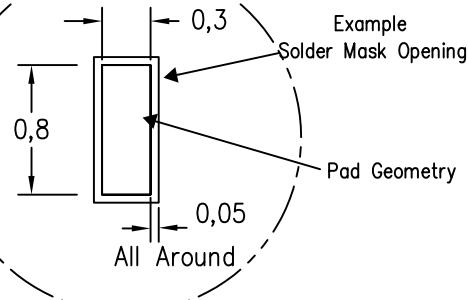
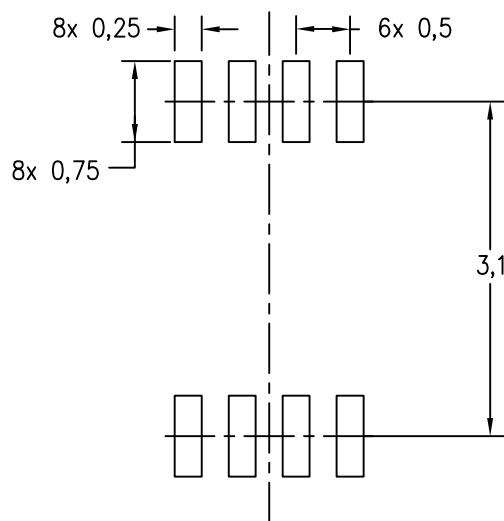
4200503/F 07/05

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

Example Board Layout
(Note C,E)Example Stencil Design
(Note D)

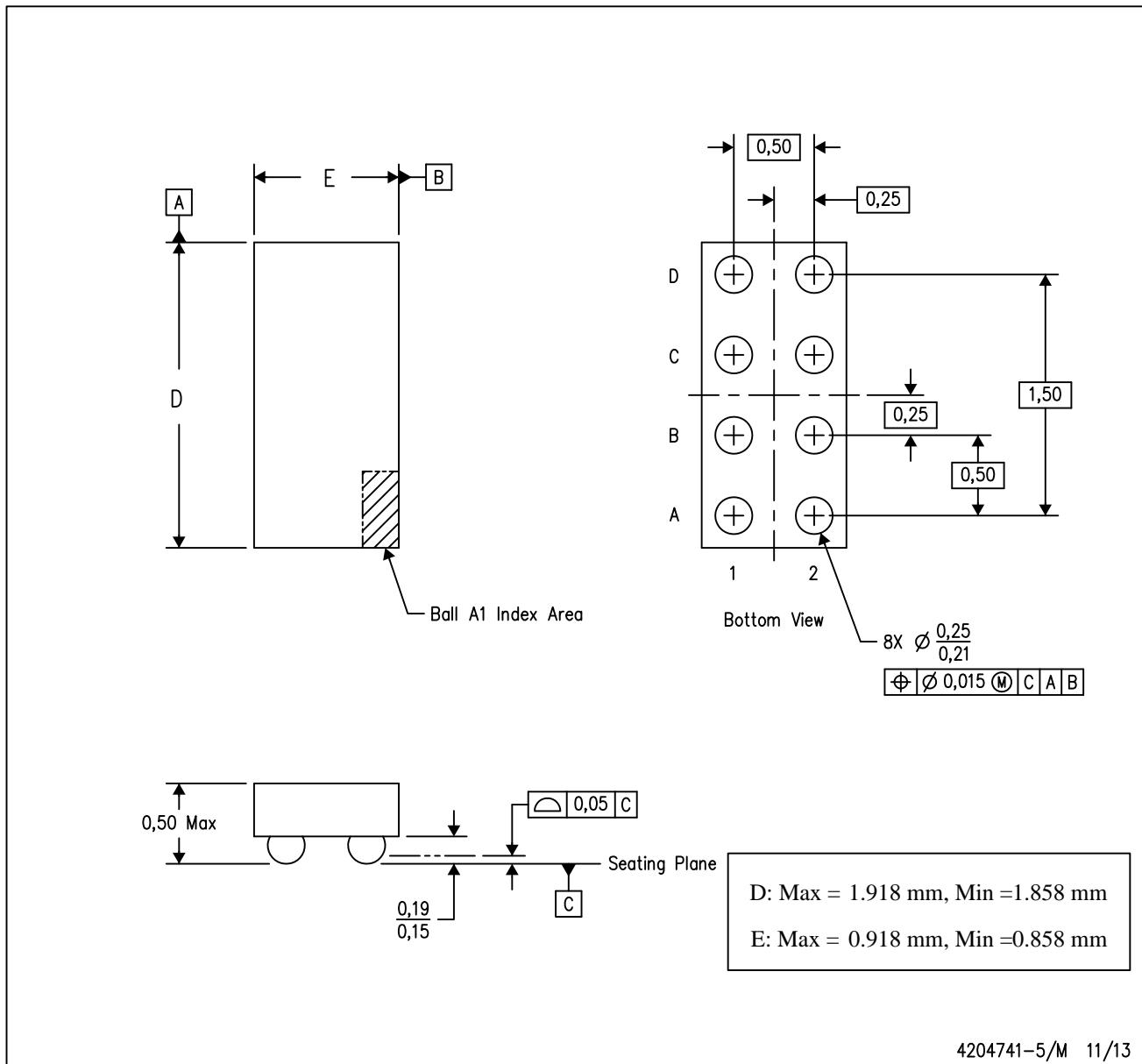
4210064/C 04/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



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